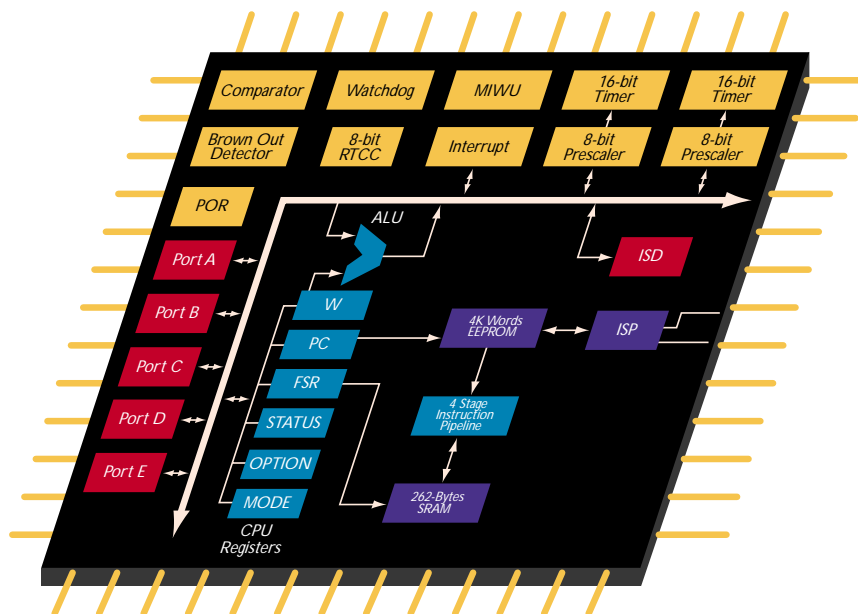


SX48/52 are members of the powerful family of SX configurable communications controllers fabricated in an advanced CMOS process technology. The advanced process, combined with a RISC-based architecture, allows high-speed computation, flexible I/O control, and efficient data manipulation. In addition, the SX architecture is deterministic and totally reprogrammable.



50 MIPS PERFORMANCE

- DC - 50 MHz operation
- 1 instruction per clock (branches 3)
- 20 ns instruction cycle, 60 ns internal interrupt response at 50 MHz

EE/FLASH PROGRAM MEMORY

- In-system programming via oscillator pins
- Access time of <10 ns provides single cycle access
- EE/Flash rated for 10,000 rewrite cycles

FAST AND DETERMINISTIC INTERRUPT

- Hardware context save/restore of PC, W, STATUS, and FSR within the 3-cycle interrupt response time
- Jitter-free 3-cycle internal interrupt response
- External wakeup/interrupt capability on Port B (8 pins)

FLEXIBLE I/O

- All pins individually programmable as I/O
- Inputs are TTL or CMOS level selectable
- All pins have selectable internal pull-ups
- Selectable Schmitt Trigger inputs on Ports B, C, D, and E
- All outputs capable of sinking/sourcing 30 mA
- Port A outputs have symmetrical drive
- Analog comparator on Port B (RB0 out, RB1 in-, RB2 in+)
- I/O operation synchronous to the oscillator clock

COMPONENT REDUCTION

- On-board brown-out detector
- Power-on-reset
- Multi-input wakeup
- Watchdog Timer

FAST TIME TO PRODUCTION

- On-chip in-system programming
- On-chip in-system debug
- Library of Virtual Peripheral™ modules
- Eval Kits for communication intensive applications

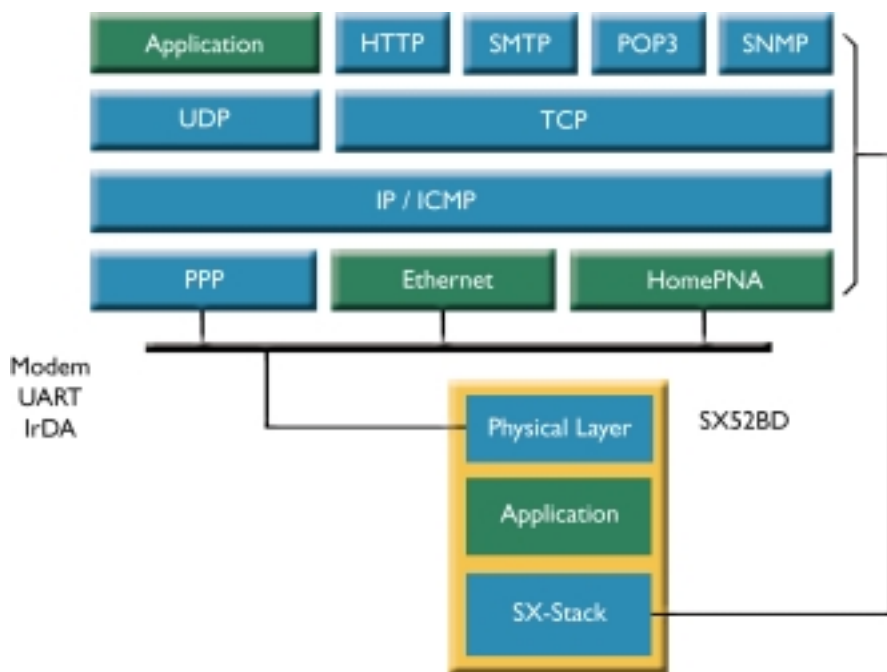
GENERAL

- 4096 words of EE/Flash program memory
- 262 bytes of SRAM
- Two 16-bit multi-function timers with 8-bit prescalers
- One 8-bit Real Time Clock/Counter (RTCC) with programmable 8-bit prescaler
- Operating voltage—2.2V to 5.5V
- Fast table lookup capability through run-time readable code
- User selectable clock modes
- TQFP-48, PQFP-52
- Complete third party development tools support

EXAMPLES OF VIRTUAL PERIPHERAL MODULES

	Virtual Peripheral	Program Memory Words	Data Memory Bytes
SX-Stack	UDP/IP/PPP	1700	61
	HTTP/TCP/IP/PPP	3200	100
	SMTP/TCP/IP/PPP	3000	90
	POP3/TCP/IP/PPP	2800	127
Physical Layer	DTMF Detection	295	52
	DTMF Generation	89	15
	FSK Detection	42	6
	FSK Generation	47	8
	Caller ID	369	70
	Ring Detect	19	3
	UART	51	10

Virtual Peripheral™ concept enables the “software system on a chip” approach. Virtual Peripheral, the software that replaces traditional hardware peripherals, takes advantage of the Ubicom architecture’s high clock speeds and deterministic nature to produce same results as hardware peripheral, with much greater flexibility.



With 50 MIPS performance and deterministic architecture, the SX52BD device allows implementation of the entire TCP/IP protocols, physical interface, and other relevant communication interfaces as Virtual Peripheral modules.



1330 Charleston Road
Mountain View, CA 94043

tel 650 210 1500
fax 650 210 8715

E-mail: sales@ubicom.com
Web site: www.ubicom.com