SX18/20/28AC and SX18/20/28AC75 are members of the powerful family of SX configurable communications controllers fabricated in an advanced CMOS process technology. The advanced process, combined with a RISC-based architecture, allows high-speed computation, flexible I/O control, and efficient data manipulation. In addition, the SX architecture is deterministic and totally reprogrammable.
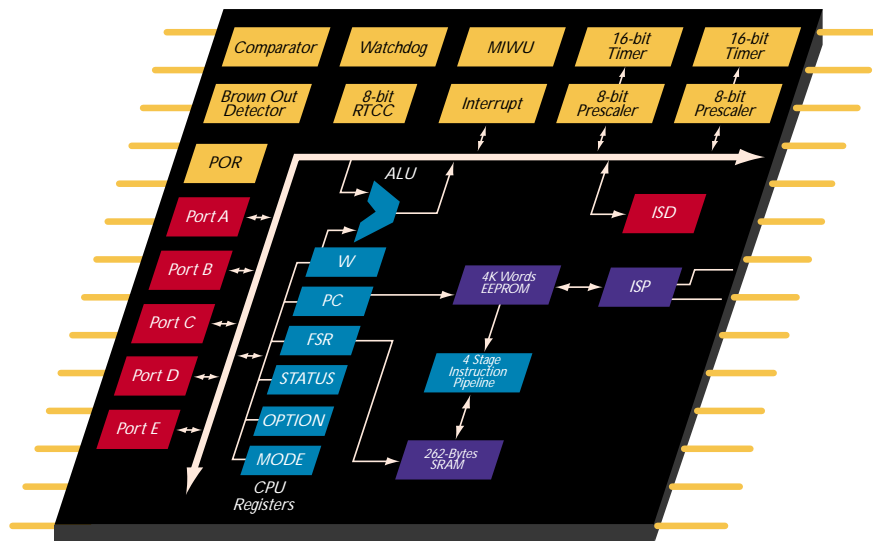
50/75 MIPS PERFORMANCE
- DC—50/75 MHz operation
- 1 instruction per clock (branches 3)
- 20 ns instruction cycle, 60 ns internal interrupt response at 50 MHz

EE/FLASH PROGRAM MEMORY
- In-system programming via oscillator pins
- Access time of <10 ns provides single cycle access
- EE/Flash rated for 10,000 rewrite cycles

FAST AND DETERMINISTIC INTERRUPT
- Hardware context save/restore of PC, W, STATUS, and FSR within the 3-cycle interrupt response time
- Jitter-free 3-cycle internal interrupt response
- External wakeup/interrupt capability on Port B (8 pins)

FLEXIBLE I/O
- All pins individually programmable as I/O
- Inputs are TTL or CMOS level selectable
- All pins have selectable internal pull-ups
- Selectable Schmitt Trigger inputs on Ports B and C
- All outputs capable of sinking/sourcing 30 mA
- Port A outputs have symmetrical drive
- Analog comparator on Port B (RB0 out, RB1 in-, RB2 in+)
- I/O operation synchronous to the oscillator clock

COMPONENT REDUCTION
- On-board brown-out detector
- Power-on-reset
- Multi-input wakeup

FAST TIME TO PRODUCTION
- On-chip in-system programming
- On-chip in-system debug
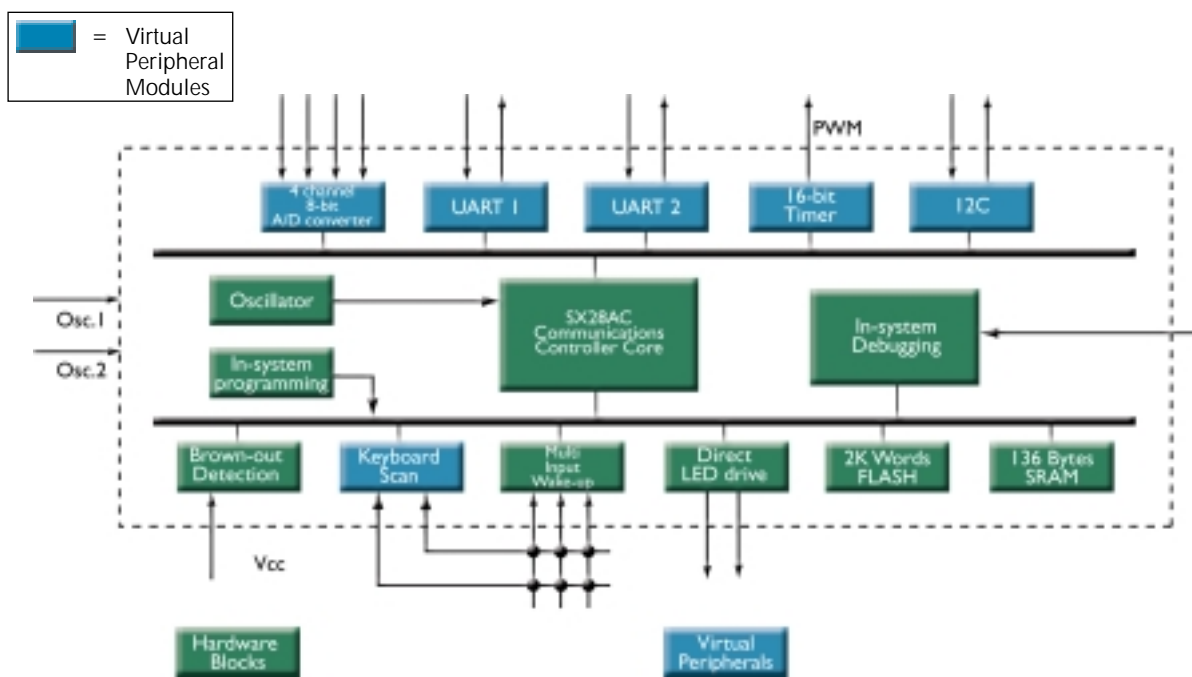- Library of Virtual Peripheral™ modules

GENERAL
- 2048 words of EE/Flash program memory
- 136 bytes of SRAM
- Two 16-bit multi-function timers with 8-bit prescalers
- Operating voltage—2.7V to 5.5V
- Fast table lookup capability through run-time readable code
- User selectable clock modes
- DIP-18/28, SSOP-20, SOIC-18/28
- Complete third party development tools support

EXAMPLES OF VIRTUAL PERIPHERAL MODULES

Peripheral Function	EEPROM Words	SRAM Bytes
UART @ 2400 Baud	51	10
16-Bit Timer	10	5
Real-Time Clock	39	9
2-Ch 8-bit ADC	25	7
FSK Generation	47	8
FSK Detection	42	6
DTMF Receive	295	52

Virtual Peripheral™ concept enables the "software system on a chip" approach. Virtual Peripheral, the software that replaces traditional hardware peripherals, takes advantage of the Ubicom architecture's high performance and deterministic nature to produce same results as hardware peripheral, with much greater flexibility.

With up to 75 MIPs performance, the SX device provides efficient implementation of software functions from a library of Virtual Peripheral modules to replace on-chip hardware functions.

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