MITSUBISHI 8-BIT SINGLE-CHIP MICROCOMPUTER
740 FAMILY / 740 SERIES

7531 Group

User's Manual

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REVISION DESCRIPTION LIST	7531 GROUP USER'S MANUAL

Rev. No.	Revision Description	Rev. date
1.0	First Edition	980801
2.0	The contents of revision are mainly as follows; CHAPTER 1 HARDWARE 3.1 Electrical characteristics 3.2 Typical characteristics 3.6 Mask ROM confirmation form 3.7 Mark specification form	990924
2.1	Updated as follows: Page1-2; Power dissipation to 25 mW Page 1-14, Fig.13; Start address of Interrupt vector area to $FFEC_{16}$ Pages 3-6, 3-14, 3-22; Parameter to Linearity error from former Absolute accuracy	991109
2.2	Page 1-3: Operating temperature range; **Note** deleted Page 1-9: Fig. 8 "Under development" revised Page 1-29: Fig. 31 Note revised Page 1-32: Description revised; $\overline{RESET}$ "L" pulse width 2 µs → 15 µs Page 1-36: Fig. 42 Rd resistor connected to X_{OUT} pin eliminated Page 2-42: Fig. 2.3.20 Note added Page 2-58: Fig. 2.5.2 revised Page 3-7: Table 3.1.6 tw($\overline{RESET}$) revised; 2 µs → 15 µs Table 3.1.7 tw($\overline{RESET}$) revised; 2 µs → 45 µs at V_{CC} = 2.2 to 5.5 V, 35 µs at V_{CC} = 2.4 to 5.5 V Page 3-15: Table 3.1.15 tw($\overline{RESET}$) revised; 2 µs → 15 µs Table 3.1.16 tw($\overline{RESET}$) revised; 2 µs → 35 µs Page 3-23: Table 3.1.24 tw($\overline{RESET}$) revised; 2 µs → 15 µs Table 3.1.25 tw($\overline{RESET}$) revised; 2 µs → 35 µs Page 3-34: Description revised; Non-linearity error → Linearity error Fig. 3.2.19 revised; Non-linearity error → Linearity error Page 3-35: Fig. 3.2.20 revised; Non-linearity error → Linearity error Page 3-36: Fig. 3.2.21 revised; Non-linearity error → Linearity error	000614
2.3	Pages 1-32, 1-36, 2-42, 3-34: Character fonts errors revised	000905

Preface

This user's manual describes Mitsubishi's CMOS 8-bit microcomputers 7531 Group.
After reading this manual, the user should have a through knowledge of the functions and features of the 7531 Group, and should be able to fully utilize the product. The manual starts with specifications and ends with application examples.

For details of software, refer to the "740 FAMILY SOFTWARE MANUAL."
For details of development support tools, refer to the "Mitsubishi Microcomputer Development Support Tools" Hompage (http://www.tool-spt.mesc.co.jp/index_e.htm).

BEFORE USING THIS MANUAL

This user's manual consists of the following three chapters. Refer to the chapter appropriate to your conditions, such as hardware design or software development. Chapter 3 also includes necessary information for systems development. You must refer to that chapter.

1. Organization

- **CHAPTER 1 HARDWARE**
  This chapter describes features of the microcomputer and operation of each peripheral function.

- **CHAPTER 2 APPLICATION**
  This chapter describes usage and application examples of peripheral functions, based mainly on setting examples of relevant registers.

- **CHAPTER 3 APPENDIX**
  This chapter includes necessary information for systems development using the microcomputer, such as the electrical characteristics, the list of registers, the Mask ROM confirmation form (for mask ROM version), the ROM programming confirmation form (for One Time PROM version), and the Mark specification form which are to be submitted when ordering.

2. Structure of register

The figure of each register structure describes its functions, contents at reset, and attributes as follows :

Bits

(Note 2) **Bit attributes**

(Note 1) **Contents immediately after reset release**

b7	b6	b5	b4	b3	b2	b1	b0
		0					

CPU mode register (CPUM) [Address : 3B $_{16}$]

B	Name	Function	At reset	R	W
0	Processor mode bits	b1 b0 0 0 : Single-chip mode 0 1 : 1 0 : } Not available 1 1 :	0	○	○
1			0	○	○
2	Stack page selection bit	0 : 0 page 1 : 1 page	0	○	○
3	Nothing arranged for these bits. These are write disabled bits. When these bits are read out, the contents are "0."		0	○	×
4			0	○	×
5	Fix this bit to "0."		1	○	○
6	Main clock (X_{IN}-X_{OUT}) stop bit	0 : Operating 1 : Stopped	✻	○	○
7	Internal system clock selection bit	0 : X_{IN}-X_{OUT} selected 1 : X_{CIN}-X_{COUT} selected	✻	○	○

■ : Bit in which nothing is arranged　　░ : Bit that is not used for control of the corresponding function

Note 1:. Contents immediately after reset release
0....... "0" at reset release
1....... "1" at reset release
?....... Undefined at reset release
✻.......Contents determined by option at reset release

Note 2: Bit attributes......... The attributes of control register bits are classified into 3 bytes : read-only, write-only and read and write. In the figure, these attributes are represented as follows :

R.......Read
○...... Read enabled
×.......Read disabled

W......Write
○ ..... Write enabled
×...... Write disabled
✻......."0" write

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CHAPTER 1
HARDWARE

DESCRIPTION/FEATURES/APPLICATION/PIN CONFIGURATION

DESCRIPTION

The 7531 Group is the 8-bit microcomputer based on the 740 family core technology.

The 7531 Group has a serial I/O, 8-bit timers, and an A-D converter, and is useful for control of home electric appliances and office automation equipment.

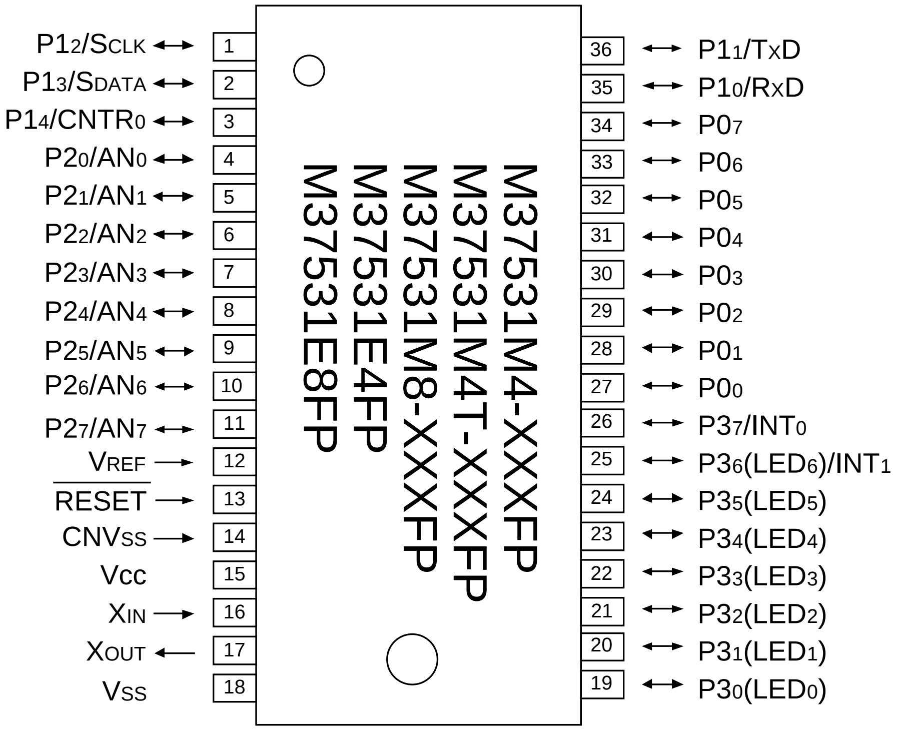
FEATURES

- Basic machine-language instructions 69
- The minimum instruction execution time .... 0.50 µs
  (at 8 MHz oscillation frequency for the shortest instruction, in high-speed mode)
- Memory size ROM .... 8K to 16K bytes
  RAM ....256 to 384 bytes
- Programmable I/O ports 29
  (25 in 32-pin version)
- Interrupts .... 12 sources, 8 vectors
  (11 sources, 8 vectors for 32-pin version)
- Timers .... 8-bit ✕ 3
- Serial I/O1 .... 8-bit ✕ 1
  (UART)
- Serial I/O2 .... 8-bit ✕ 1
  (Clock-synchronized)
- A-D converter .... 10-bit ✕ 8 channels
  (6 channels for 32-pin version)
- Clock generating circuit .... Built-in type
  (connect to external ceramic resonator or quartz-crystal oscillator permitting RC oscillation)
- Watchdog timer .... 16-bit ✕ 1
- Power source voltage
  At 8 MHz X_{IN} oscillation frequency at ceramic oscillation
  .... 4.0 to 5.5 V
  At 4 MHz X_{IN} oscillation frequency at ceramic oscillation
  .... 2.4 to 5.5 V
  At 2 MHz X_{IN} oscillation frequency at ceramic oscillation
  .... 2.2 to 5.5 V
  At 4 MHz X_{IN} oscillation frequency at RC oscillation
  .... 4.0 to 5.5 V
  At 2 MHz X_{IN} oscillation frequency at RC oscillation
  .... 2.4 to 5.5 V
  At 1 MHz X_{IN} oscillation frequency at RC oscillation
  .... 2.2 to 5.5 V
- Power dissipation .... 25 mW (standard)
- Operating temperature range .... –20 to 85 °C
  (–40 to 85 °C or –40 to 125 °C for extended operating temperature version)

APPLICATION

Office automation equipment, factory automation equipment, home electric appliances, consumer electronics, car, etc.

PIN CONFIGURATION (TOP VIEW)



Package type: 36P2R-A

Fig. 1 Pin configuration (36P2R package type)

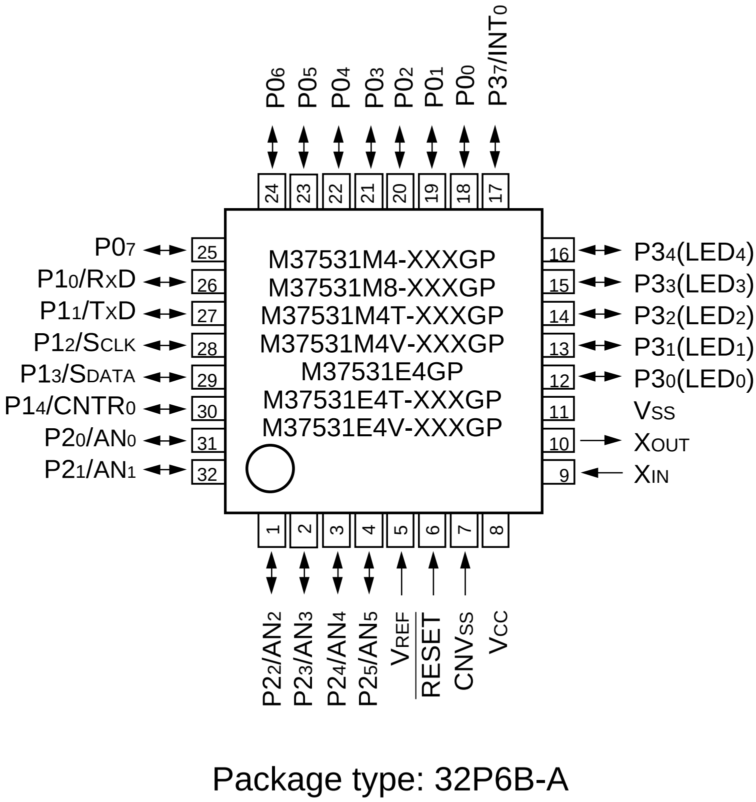


Fig. 2 Pin configuration (32P6B package type)

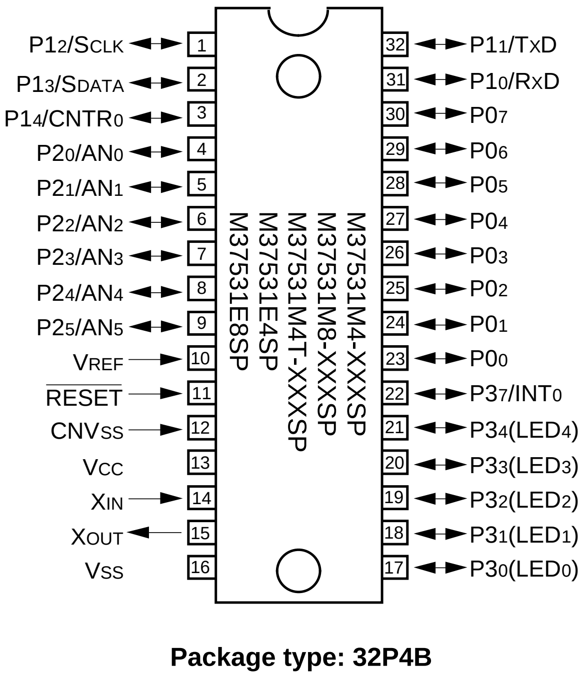


Fig. 3 Pin configuration (32P4B package type)

PIN CONFIGURATION

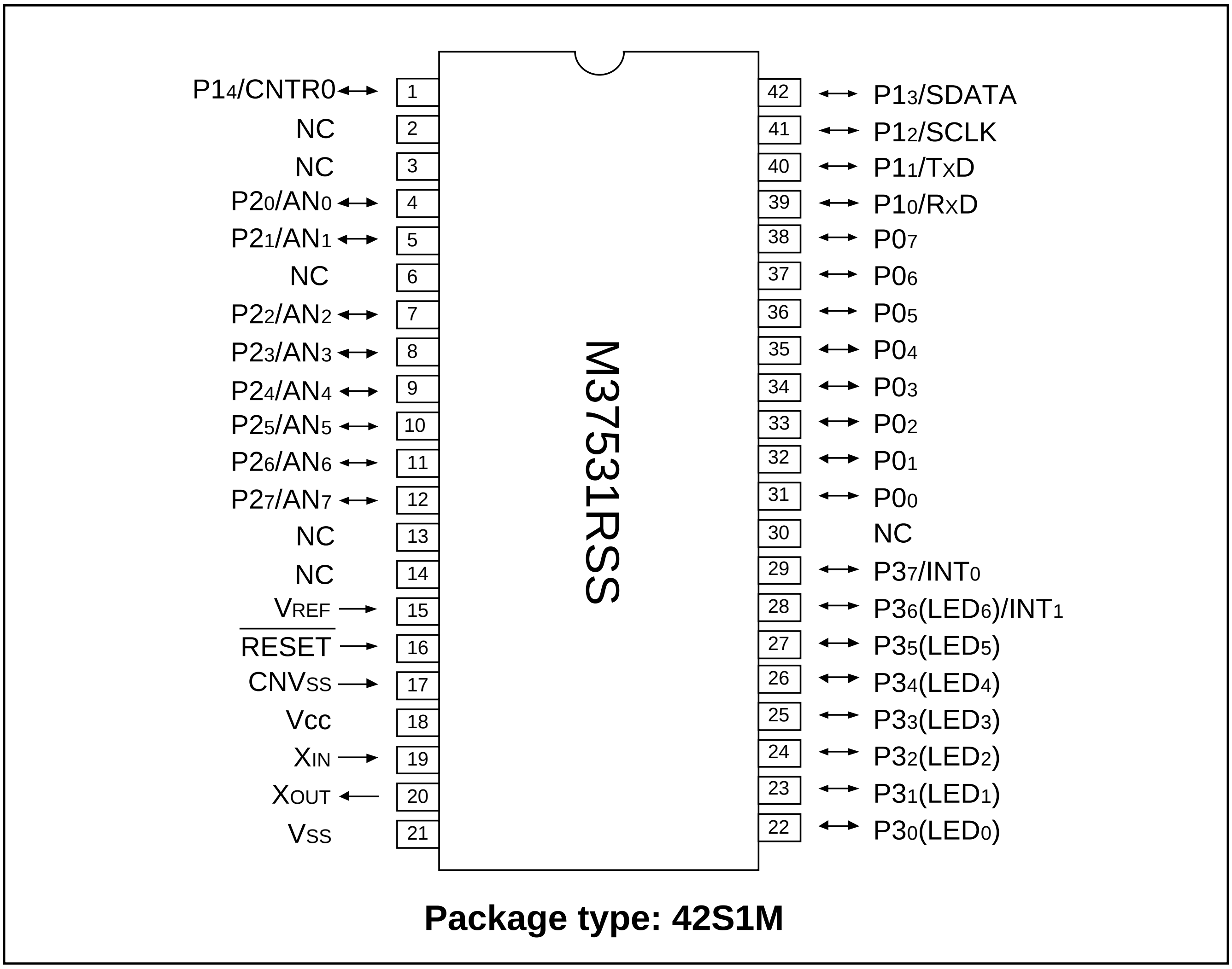


Fig. 4 Pin configuration (42S1M package type)

FUNCTIONAL BLOCK

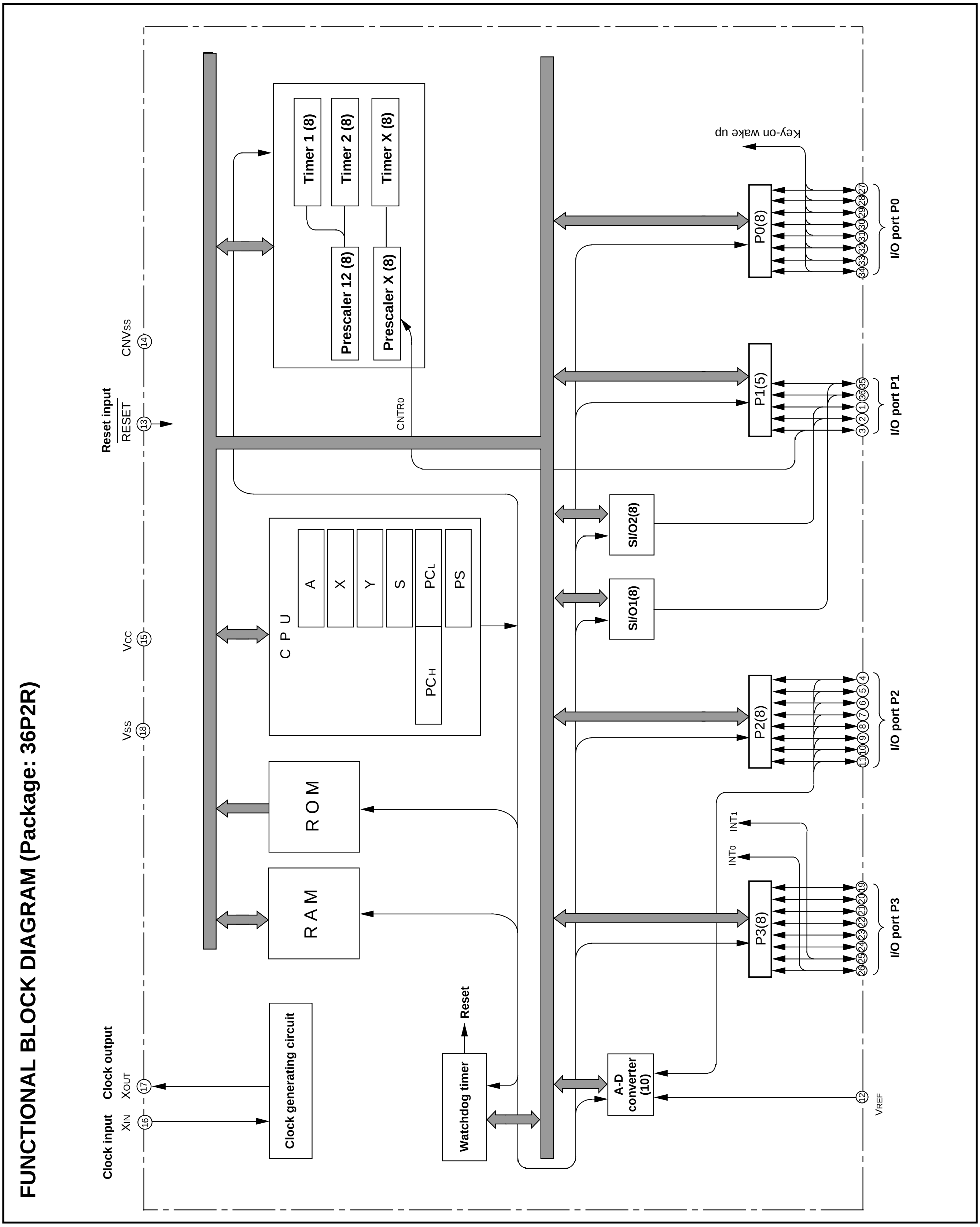


Fig. 5 Functional block diagram (36P2R package)

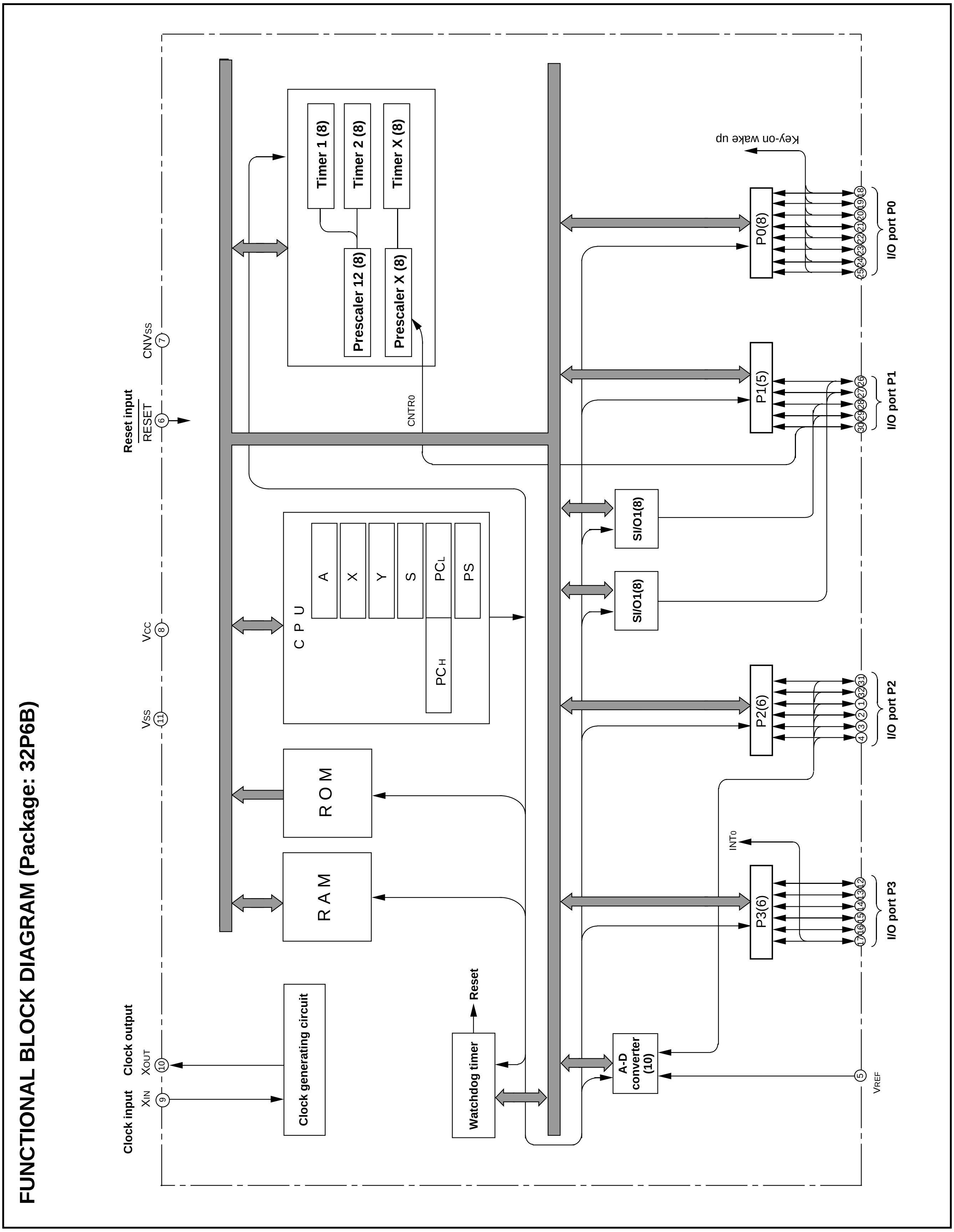


Fig. 6 Functional block diagram (32P6B package)

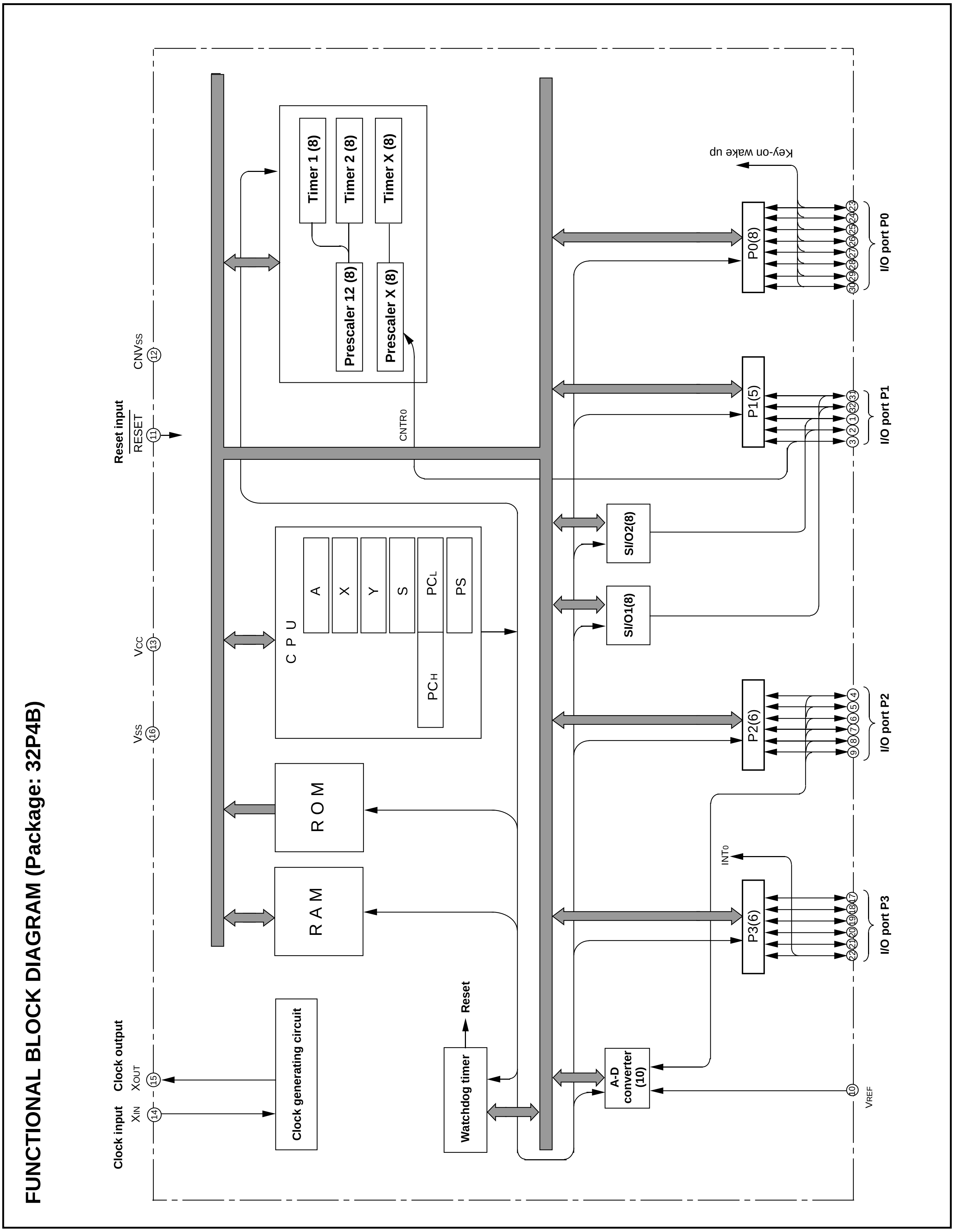


Fig. 7 Functional block diagram (32P4B package)

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	Function expect a port function
Vcc, Vss	Power source (Note 1)	•Apply voltage of 2.2–5.5 V to Vcc, and 0 V to Vss.	
V_{REF}	Analog reference voltage	•Reference voltage input pin for A-D converter	
CNVss	CNVss	•Chip operating mode control pin, which is always connected to Vss.	
$\overline{RESET}$	Reset input	•Reset input pin for active “L”	
X_{IN}	Clock input	•Input and output pins for main clock generating circuit •Connect a ceramic resonator or quartz crystal oscillator between the X_{IN} and X_{OUT} pins. •For using RC oscillator, short between the X_{IN} and X_{OUT} pins, and connect the capacitor and resistor. •If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
$P0_0$–$P0_7$	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •Whether a built-in pull-up resistor is to be used or not can be determined by program.	•Key-input (key-on wake up interrupt input) pins
$P1_0$/RxD $P1_1$/TxD	I/O port P1	•5-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •CMOS/TTL level can be switched for $P1_0$, $P1_2$ and $P1_3$	•Serial I/O1 function pin
$P1_2$/S_{CLK} $P1_3$/S_{DATA}			•Serial I/O2 function pin
$P1_4$/$CNTR_0$			•Timer X function pin
$P2_0$/AN_0– $P2_7$/AN_7	I/O port P2 (Note 2)	•8-bit I/O port having almost the same function as P0 •CMOS compatible input level •CMOS 3-state output structure	•Input pins for A-D converter
$P3_0$–$P3_5$	I/O port P3 (Note 3)	•8-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level (CMOS/TTL level can be switched for $P3_6$ and $P3_7$). •CMOS 3-state output structure •$P3_0$ to $P3_6$ can output a large current for driving LED. •Whether a built-in pull-up resistor is to be used or not can be determined by program.	
$P3_6$/INT_1 $P3_7$/INT_0			•Interrupt input pins

Notes 1: V_{CC} = 2.4 to 5.5 V for the extended operating temperature version (–40 to 85 °C) and the extended operating temperature 125 °C version (–40 to 125 °C).

2: 6-bit I/O port ($P2_0$–$P2_5$) for the 32-pin version.

3: 6-bit I/O port ($P3_0$–$P3_4$, $P3_7$/INT_0) for the 32-pin version.

GROUP EXPANSION

Mitsubishi plans to expand the 7531 group as follow:

Memory type

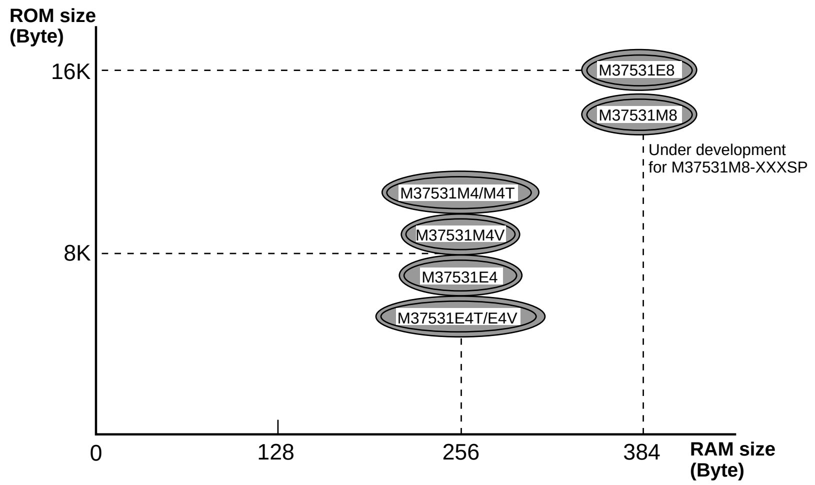
Support for Mask ROM version, One Time PROM version, and Emulator MCU .

Memory size

ROM/PROM size .... 8 K to 16 K bytes
RAM size .... 256 to 384 bytes

Package

32P4B .... 32 pin plastic molded SDIP
32P6B-A .... 0.8 mm-pitch plastic molded LQFP
36P2R-A .... 0.8 mm-pitch plastic molded SSOP
42S1M .... 42 pin shrink ceramic PIGGY BACK



Note. Products under development: the development schedule and specification may be revised without notice.

Fig. 8 Memory expansion plan

Currently supported products are listed below.

Table 2 List of supported products

Product	(P) ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M37531M4-XXXSP	8192 (8062)	256	32P4B	Mask ROM version
M37531M4T-XXXSP				Mask ROM version (extended operating temperature version)
M37531E4SP				One Time PROM version (blank)
M37531M4-XXXFP			36P2R-A	Mask ROM version
M37531M4T-XXXFP				Mask ROM version (extended operating temperature version)
M37531E4FP				One Time PROM version (blank)
M37531M4-XXXGP			32P6B-A	Mask ROM version
M37531M4T-XXXGP				Mask ROM version (extended operating temperature version)
M37531M4V-XXXGP				Mask ROM version (extended operating temperature 125 °C version)
M37531E4GP				One Time PROM version (blank)
M37531E4T-XXXGP				One Time PROM version (shipped after programming, extended operating temperature version)
M37531E4V-XXXGP				One Time PROM version (shipped after programming, extended operating temperature 125 °C version)
M37531M8-XXXSP	16384 (16254)	384	32P4B	Mask ROM version
M37531E8SP				One Time PROM version (blank)
M37531M8-XXXFP			36P2R-A	Mask ROM version
M37531E8FP				One Time PROM version (blank)
M37531M8-XXXGP			32P6B-A	Mask ROM version
M37531RSS	——		42S1M	Emulator MCU

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The 7531 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.
Machine-resident 740 family instructions are as follows:
The FST and SLW instructions cannot be used.
The MUL and DIV instructions cannot be used.
The WIT and STP instructions can be used.
The central processing unit (CPU) has the six registers.

Accumulator (A)

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

Index register X (X), Index register Y (Y)

Both index register X and index register Y are 8-bit registers. In the index addressing modes, the value of the OPERAND is added to the contents of register X or register Y and specifies the real address.
When the T flag in the processor status register is set to “1”, the value contained in index register X becomes the address for the second OPERAND.

Stack pointer (S)

The stack pointer is an 8-bit register used during sub-routine calls and interrupts. The stack is used to store the current address data and processor status when branching to subroutines or interrupt routines.
The lower eight bits of the stack address are determined by the contents of the stack pointer. The upper eight bits of the stack address are determined by the Stack Page Selection Bit. If the Stack Page Selection Bit is “0”, then the RAM in the zero page is used as the stack area. If the Stack Page Selection Bit is “1”, then RAM in page 1 is used as the stack area.
The Stack Page Selection Bit is located in the SFR area in the zero page. Note that the initial value of the Stack Page Selection Bit varies with each microcomputer type. Also some microcomputer types have no Stack Page Selection Bit and the upper eight bits of the stack address are fixed. The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 10.

Program counter (PC)

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

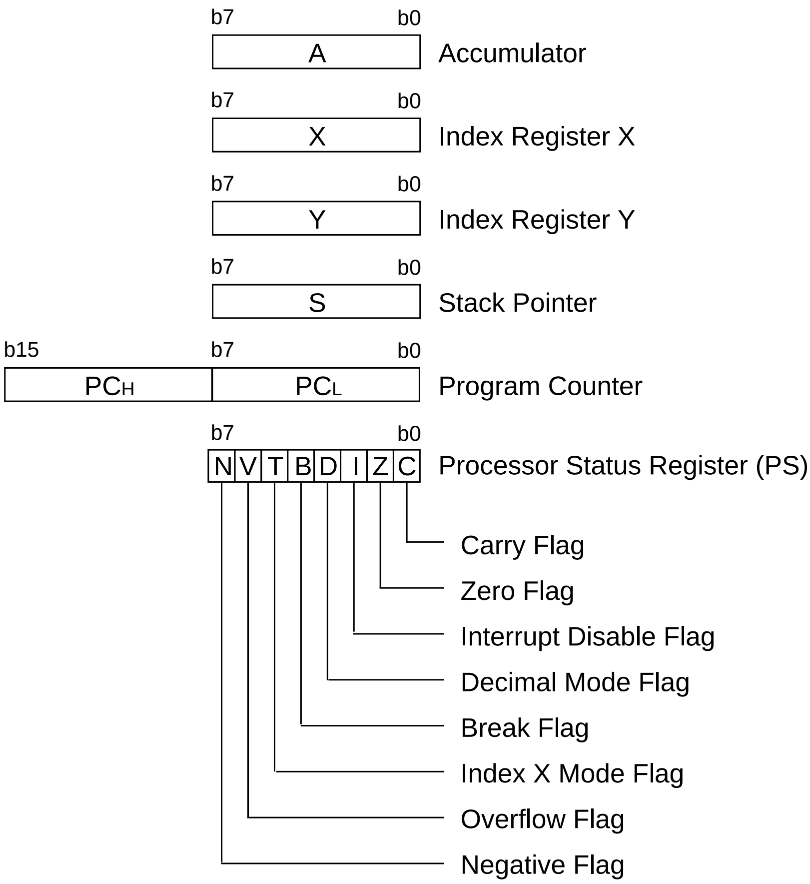


Fig. 9 740 Family CPU register structure

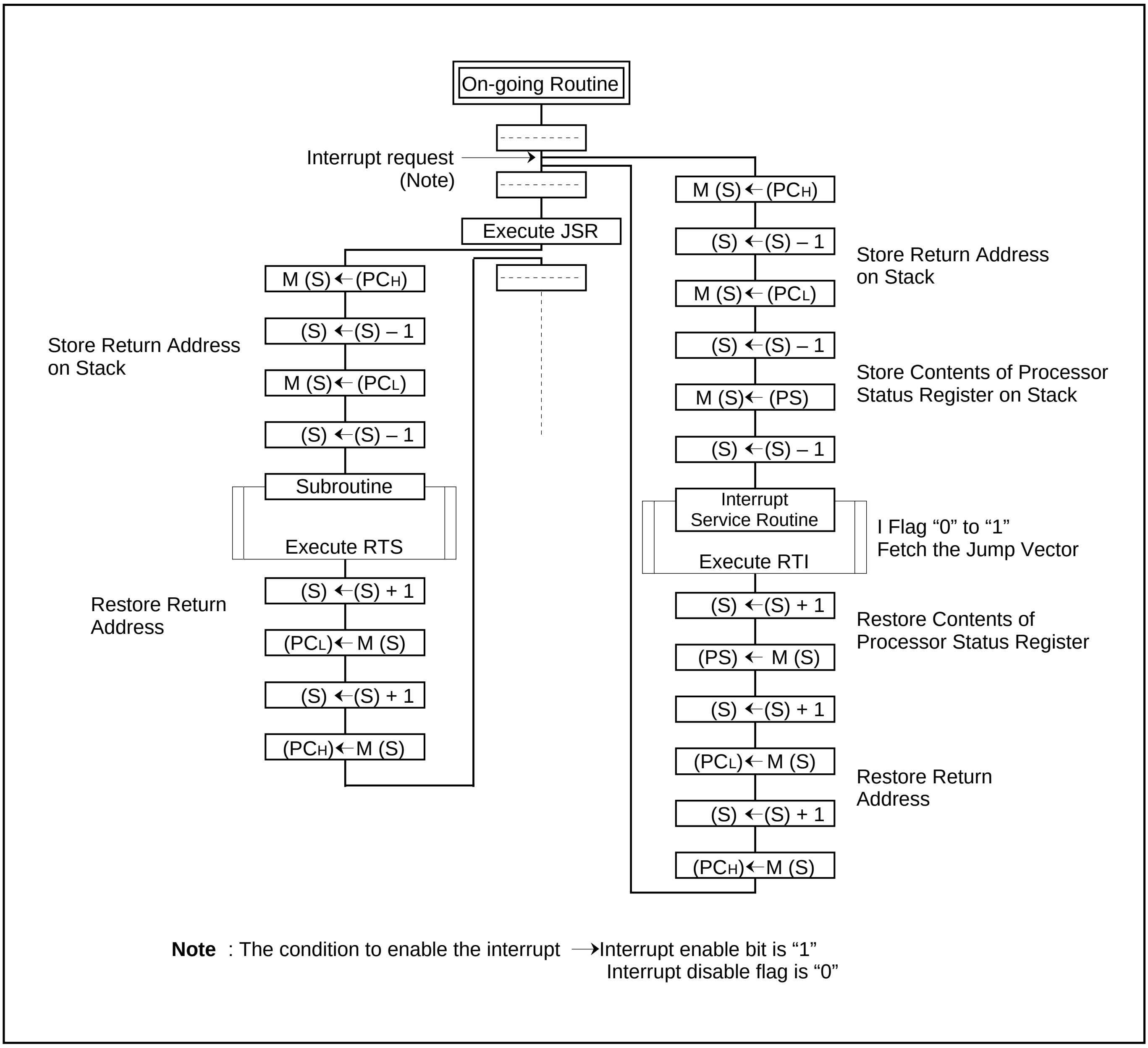


Fig. 10 Register push and pop at interrupt generation and subroutine call

Table 3 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

Processor status register (PS)

The processor status register is an 8-bit register consisting of flags which indicate the status of the processor after an arithmetic operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

After reset, the Interrupt disable (I) flag is set to “1”, but all other flags are undefined. Since the Index X mode (T) and Decimal mode (D) flags directly affect arithmetic operations, they should be initialized in the beginning of a program.

(1) Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

(2) Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

(3) Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is “1”.

When an interrupt occurs, this flag is automatically set to “1” to prevent other interrupts from interfering until the current interrupt is serviced.

(4) Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”. Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

(5) Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”. The saved processor status is the only place where the break flag is ever set.

(6) Index X mode flag (T)

When the T flag is “0”, arithmetic operations are performed between accumulator and memory, e.g. the results of an operation between two memory locations is stored in the accumulator. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations, i.e. between memory and memory, memory and I/O, and I/O and I/O. In this case, the result of an arithmetic operation performed on data in memory location 1 and memory location 2 is stored in memory location 1. The address of memory location 1 is specified by index register X, and the address of memory location 2 is specified by normal addressing modes.

(7) Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

(8) Negative flag (N)

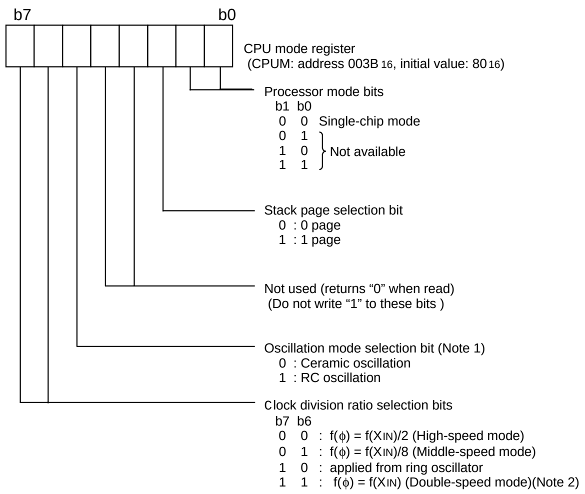
The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 4 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register] CPUM

The CPU mode register contains the stack page selection bit.
This register is allocated at address 003B16.

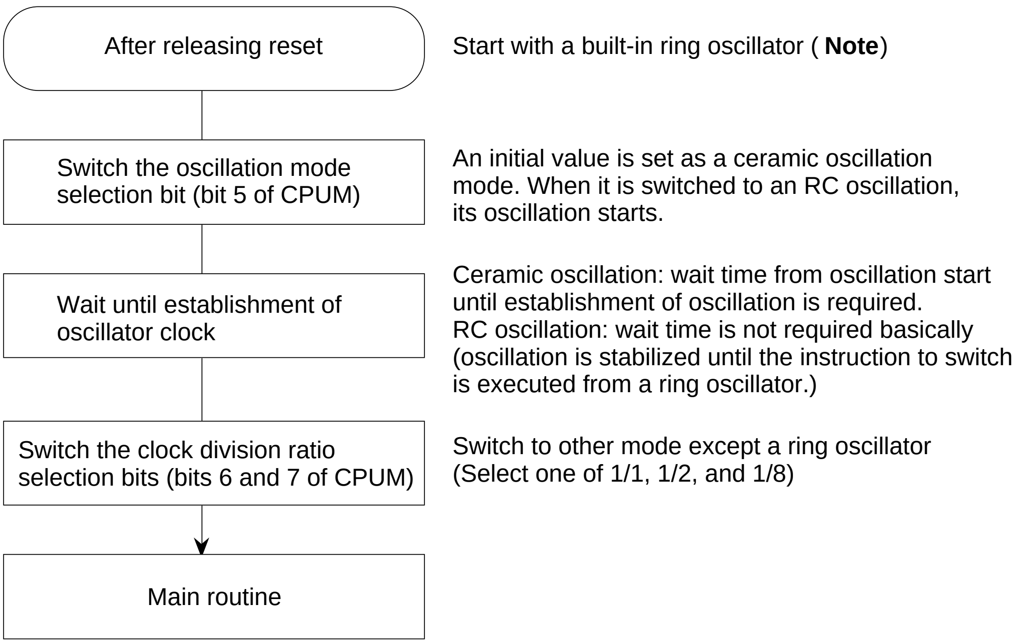


Note 1: The bit can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. However, by reset the bit is initialized and can be rewritten, again.
2: These bits are used only when a ceramic oscillation is selected. Do not use these when an RC oscillation is selected.

Fig. 11 Structure of CPU mode register

Switching method of CPU mode register

Switch the CPU mode register (CPUM) at the head of program after releasing Reset in the following method.



Note. After releasing reset the operation starts by starting a ring oscillator automatically. Do not use a ring oscillator at ordinary operation.

Fig. 12 Switching method of CPU mode register

Memory

Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM capacity (bytes)	address $XXXX_{16}$
256	$013F_{16}$
384	$01BF_{16}$

ROM area

ROM capacity (bytes)	address $YYYY_{16}$	address $ZZZZ_{16}$
8192	$E000_{16}$	$E080_{16}$
16384	$C000_{16}$	$C080_{16}$

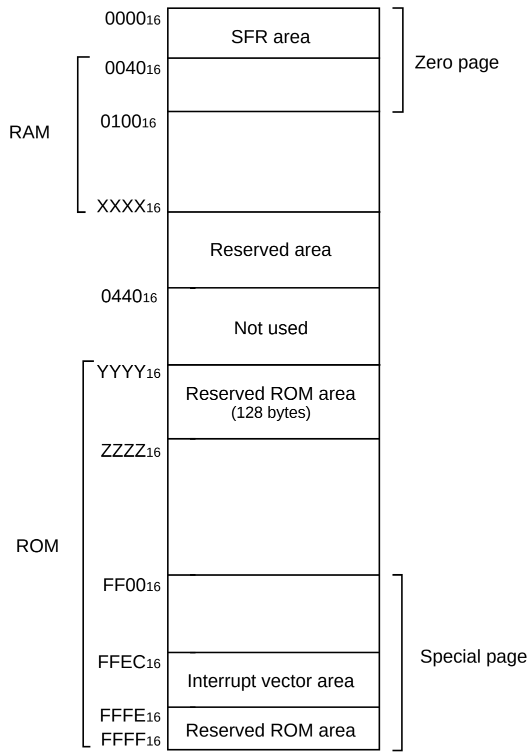


Fig. 13 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	
0001_{16}	Port P0 direction register (P0D)	0021_{16}	
0002_{16}	Port P1 (P1)	0022_{16}	
0003_{16}	Port P1 direction register (P1D)	0023_{16}	
0004_{16}	Port P2 (P2)	0024_{16}	
0005_{16}	Port P2 direction register (P2D)	0025_{16}	
0006_{16}	Port P3 (P3)	0026_{16}	
0007_{16}	Port P3 direction register (P3D)	0027_{16}	
0008_{16}		0028_{16}	Prescaler 12 (PRE12)
0009_{16}		0029_{16}	Timer 1 (T1)
$000A_{16}$		$002A_{16}$	Timer 2 (T2)
$000B_{16}$		$002B_{16}$	Timer X mode register (TM)
$000C_{16}$		$002C_{16}$	Prescaler X (PREX)
$000D_{16}$		$002D_{16}$	Timer X (TX)
$000E_{16}$		$002E_{16}$	Timer count source set register (TCSS)
$000F_{16}$		$002F_{16}$	
0010_{16}		0030_{16}	Serial I/O2 control register (SIO2CON)
0011_{16}		0031_{16}	Serial I/O2 register (SIO2)
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	A-D control register (ADCON)
0015_{16}		0035_{16}	A-D conversion register (low-order) (ADL)
0016_{16}	Pull-up control register (PULL)	0036_{16}	A-D conversion register (high-order) (ADH)
0017_{16}	Port P1P3 control register (P1P3C)	0037_{16}	
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	MISRG
0019_{16}	Serial I/O1 status register (SIO1STS)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$		$003D_{16}$	
$001E_{16}$		$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$		$003F_{16}$	

Note : Do not access to the SFR area including nothing.

Fig. 14 Memory map of special function register (SFR)

I/O Ports

[Direction registers] PiD

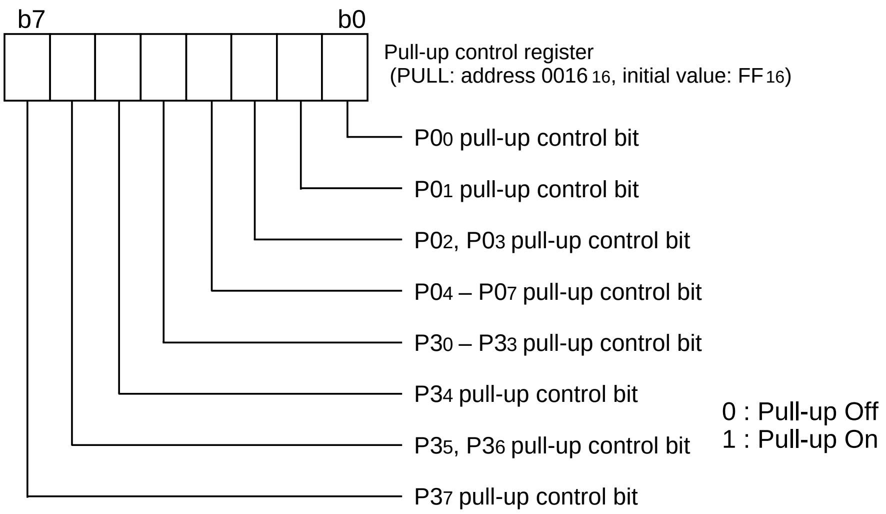
The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output.
When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port.
When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.
If a pin set to input is written to, only the port latch is written to and the pin remains floating.

[Pull-up control] PULL

By setting the pull-up control register (address 0016_{16}), ports P0 and P3 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

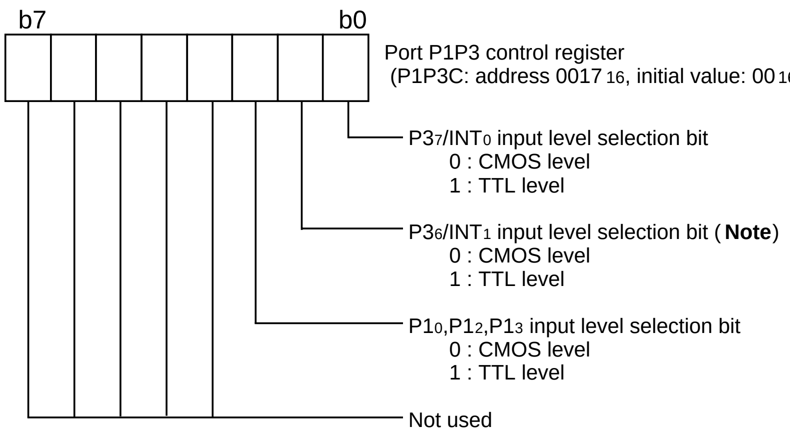
[Port P1P3 control] P1P3C

By setting the port P1P3 control register (address 0017_{16}), a CMOS input level or a TTL input level can be selected for ports $P1_0$, $P1_2$, $P1_3$, $P3_6$, and $P3_7$ by program.



Note 1: Pins set to output ports are disconnected from pull-up control.
2: Keep setting the $P3_5$, $P3_6$ pull-up control bit to "1" (initial value) for 32-pin version.

Fig. 15 Structure of pull-up control register



Note: Keep setting the $P3_6$/INT_1 input level selection bit to "0" (initial value) for 32-pin version.

Fig. 16 Structure of port P1P3 control register

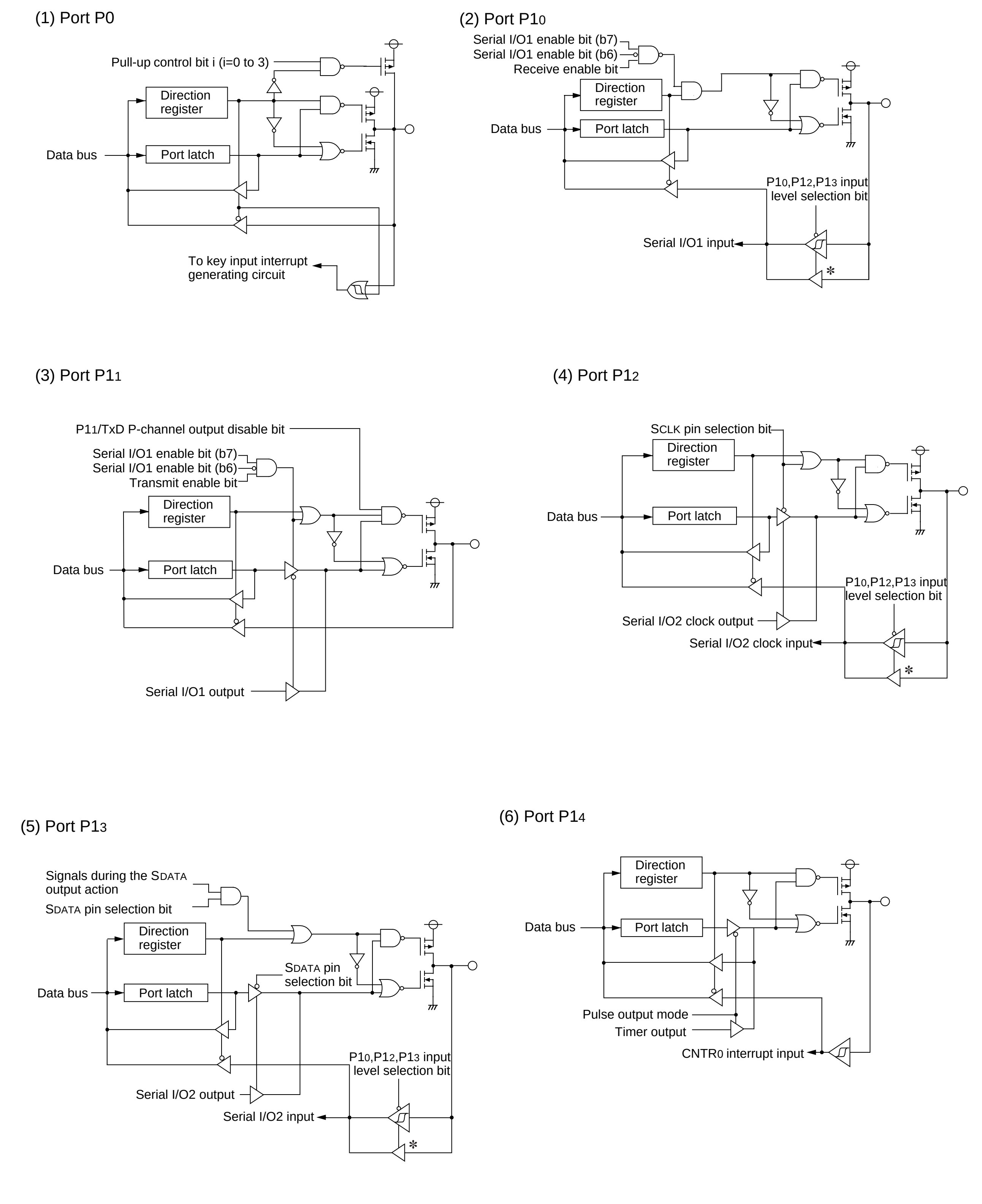
Table 5 I/O port function table

Pin	Name	Input/output	I/O format	Non-port function	Related SFRs	Diagram No.
$P0_0$–$P0_7$	I/O port P0	I/O individual bits	•CMOS compatible input level •CMOS 3-state output (Note 1)	Key input interrupt	Pull-up control register	(1)
$P1_0$/RxD $P1_1$/TxD	I/O port P1			Serial I/O1 function input/output	Serial I/O1 control register	(2) (3)
$P1_2$/S_{CLK} $P1_3$/S_{DATA}				Serial I/O2 function input/output	Serial I/O2 control register	(4) (5)
$P1_4$/$CNTR_0$				Timer X function input/output	Timer X mode register	(6)
$P2_0$/AN_0– $P2_7$/AN_7	I/O port P2 (Note 2)			A-D conversion input	A-D control register	(7)
$P3_0$–$P3_5$	I/O port P3 (Note 3)					(8)
$P3_6$/INT_1 $P3_7$/INT_0				External interrupt input	Interrupt edge selection register	(9)

Notes 1: Ports $P1_0$, $P1_2$, $P1_3$, $P3_6$, and $P3_7$ are CMOS/TTL level.

2: The $P2_6$/AN_6 and $P2_7$/AN_7 pins do not exist for the 32-pin version.

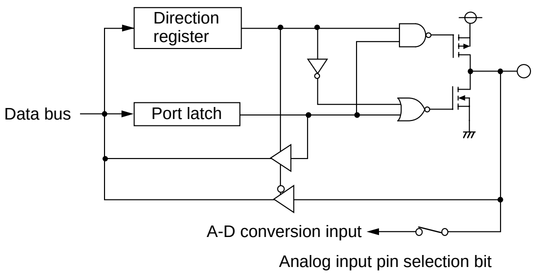
3: The $P3_5$ and $P3_6$/INT_1 pins do not exist for the 32-pin version.



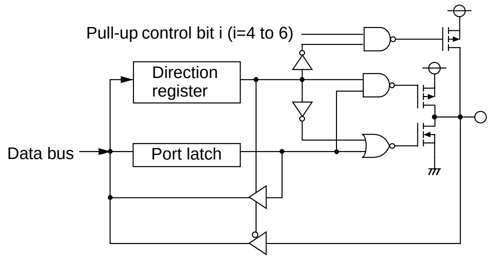
✻ P10, P12, P13, P36, and P37 input level are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

Fig. 17 Block diagram of ports (1)

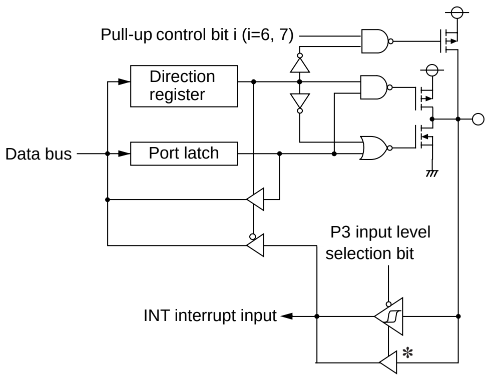
(7) Ports P2$_0$ – P2$_7$



(8) Ports P3$_0$ – P3$_5$



(9) Ports P3$_6$, P3$_7$



✻ P1$_0$, P1$_2$, P1$_3$, P3$_6$, and P3$_7$ input level are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

Fig. 18 Block diagram of ports (2)

Interrupts

Interrupts occur by 12 different sources : 4 external sources, 7 internal sources and 1 software source.

Interrupt control

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit, and they are controlled by the interrupt disable flag. When the interrupt enable bit and the interrupt request bit are set to “1” and the interrupt disable flag is set to “0”, an interrupt is accepted.
The interrupt request bit can be cleared by program but not be set. The interrupt enable bit can be set and cleared by program.
It becomes usable by switching $CNTR_0$ and AD conversion interrupt sources with bit 7 of the interrupt edge selection register, timer 2 and serial I/O2 interrupt sources with bit 6, timer X and key-on wake-up interrupt sources with bit 5, and serial I/O1 transmit and INT_1 interrupt sources with bit 4.
The reset and BRK instruction interrupt can never be disabled with any flag or bit. All interrupts except these are disabled when the interrupt disable flag is set.
When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. Concurrently with the push operation, the interrupt destination address is read from the vector table into the program counter.

Notes on use

When the active edge of an external interrupt (INT_0, INT_1,$CNTR_0$) is set, the interrupt request bit may be set.
Therefore, please take following sequence:

1. Disable the external interrupt which is selected.
2. Change the active edge in interrupt edge selection register. (in case of $CNTR_0$: Timer X mode register)
3. Clear the set interrupt request bit to “0”.
4. Enable the external interrupt which is selected.

Table 6 Interrupt vector address and priority

Interrupt source	Priority	Vector addresses (Note 1)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset input	Non-maskable
Serial I/O1 receive	2	$FFFB_{16}$	$FFFA_{16}$	At completion of serial I/O1 data receive	Valid when serial I/O1 is selected
Serial I/O1 transmit	3	$FFF9_{16}$	$FFF8_{16}$	At completion of serial I/O1 transmit shift or when transmit buffer is empty	Valid when serial I/O1 is selected
INT_1 (Note 3)				At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
INT_0	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
Timer X	5	$FFF5_{16}$	$FFF4_{16}$	At timer X underflow	
Key-on wake-up				At falling of conjunction of input logical level for port P0 (at input)	External interrupt (valid at falling)
Timer 1	6	$FFF3_{16}$	$FFF2_{16}$	At timer 1 underflow	STP release timer underflow
Timer 2	7	$FFF1_{16}$	$FFF0_{16}$	At timer 2 underflow	
Serial I/O2				At completion of transmit/receive shift	
$CNTR_0$	8	$FFEF_{16}$	$FFEE_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
A-D conversion				At completion of A-D conversion	
BRK instruction	9	$FFED_{16}$	$FFEC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1: Vector addressed contain internal jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.
3: It is an interrupt which can use only for 36 pin version.

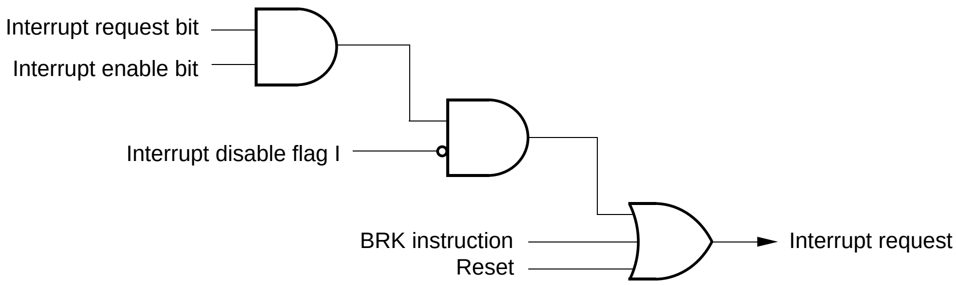


Fig. 19 Interrupt control

b7 b0 Interrupt edge selection register
(INTEDGE : address $003A_{16}$, initial value: 00_{16})

- INT$_0$ interrupt edge selection bit
  - 0 : Falling edge active
  - 1 : Rising edge active
- INT$_1$ interrupt edge selection bit
  - 0 : Falling edge active
  - 1 : Rising edge active
- Not used (returns “0” when read)
- Serial I/O1 or INT$_1$ interrupt selection bit
  (Do not write “1” for 32 pin version)
  - 0 : Serial I/O1
  - 1 : INT$_1$
- Timer X or key-on wake up interrupt selection bit
  - 0 : Timer X
  - 1 : Key-on wake up
- Timer 2 or serial I/O2 interrupt selection bit
  - 0 : Timer 2
  - 1 : Serial I/O2
- CNTR$_0$ or AD converter interrupt selection bit
  - 0 : CNTR$_0$
  - 1 : AD converter

b7 b0 Interrupt request register 1
(IREQ1 : address $003C_{16}$, initial value: 00_{16})

- Serial I/O1 receive interrupt request bit
- Serial I/O1 transmit or INT$_1$ interrupt request bit
- INT$_0$ interrupt request bit
- Timer X or key-on wake up interrupt request bit
- Timer 1 interrupt request bit
- Timer 2 or serial I/O2 interrupt request bit
- CNTR$_0$ or AD converter interrupt request bit
- Not used (returns “0” when read)

0 : No interrupt request issued
1 : Interrupt request issued

b7 b0 Interrupt control register 1
(ICON1 : address $003E_{16}$, initial value: 00_{16})

- Serial I/O1 receive interrupt enable bit
- Serial I/O1 transmit or INT$_1$ interrupt enable bit
- INT$_0$ interrupt enable bit
- Timer X or key-on wake up interrupt enable bit
- Timer 1 interrupt enable bit
- Timer 2 or serial I/O2 interrupt enable bit
- CNTR$_0$ or AD converter interrupt enable bit
- Not used (returns “0” when read)
  (Do not write “1” to this bit)

0 : Interrupts disabled
1 : Interrupts enabled

Fig. 20 Structure of Interrupt-related registers

Key Input Interrupt (Key-On Wake-Up)

A key-on wake-up interrupt request is generated by applying “L” level to any pin of port P0 that has been set to input mode.

In other words, it is generated when the AND of input level goes from “1” to “0”. An example of using a key input interrupt is shown in Figure 21, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports $P0_0$ to $P0_3$ as input ports.

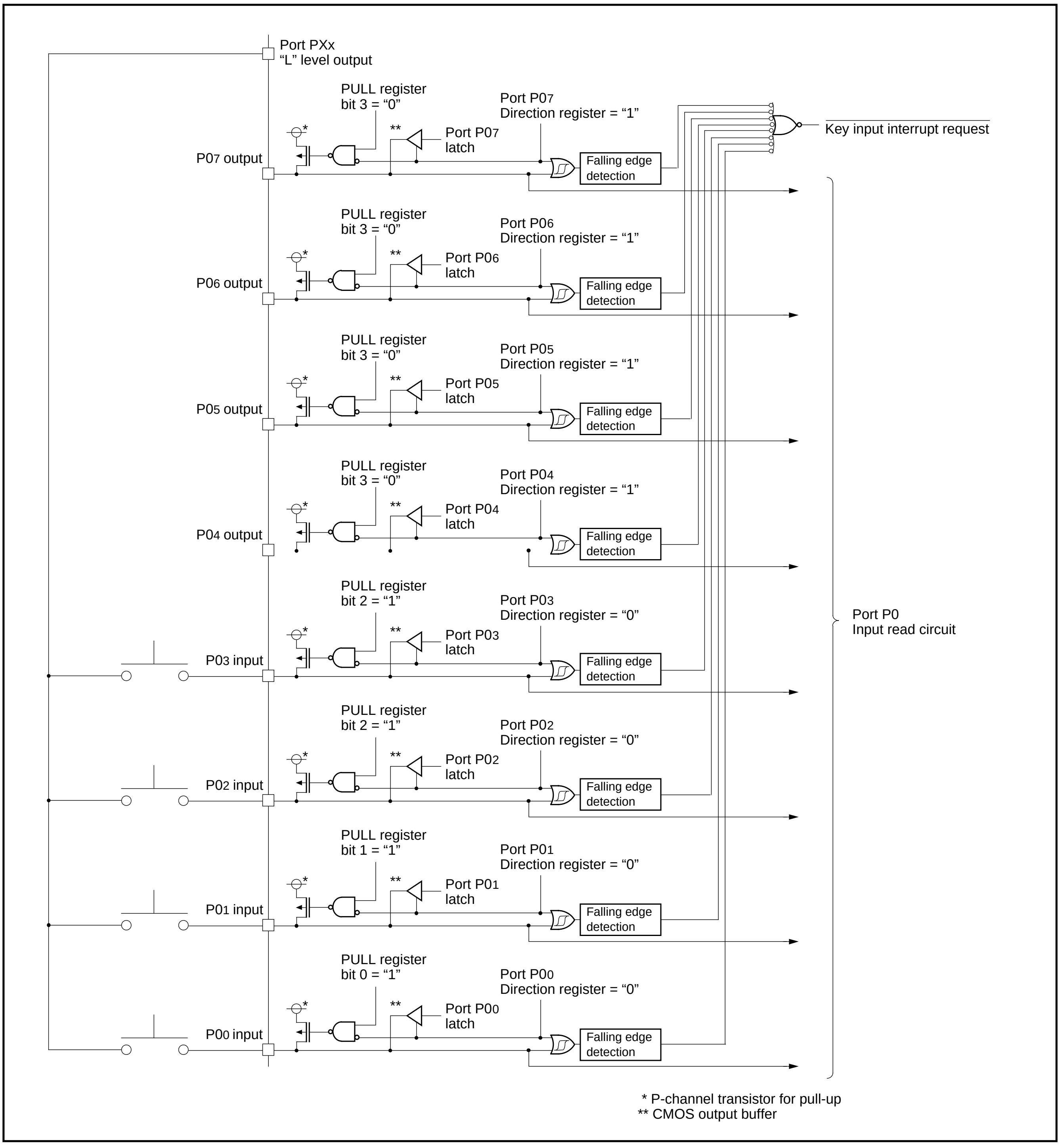


Fig. 21 Connection example when using key input interrupt and port P0 block diagram

Timers

The 7531 Group has 3 timers: timer X, timer 1 and timer 2.
The division ratio of every timer and prescaler is 1/(n+1) provided that the value of the timer latch or prescaler is n.
All the timers are down count timers. When a timer reaches “0”, an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to “1”.

●Timer 1, Timer 2

Prescaler 12 always counts f(X_{IN})/16. Timer 1 and timer 2 always count the prescaler output and periodically sets the interrupt request bit.

●Timer X

Timer X can be selected in one of 4 operating modes by setting the timer X mode register.

• Timer Mode

The timer counts the signal selected by the timer X count source selection bit.

• Pulse Output Mode

The timer counts the signal selected by the timer X count source selection bit, and outputs a signal whose polarity is inverted each time the timer value reaches “0”, from the $CNTR_0$ pin.
When the $CNTR_0$ active edge switch bit is “0”, the output of the $CNTR_0$ pin is started with an “H” output.
At “1”, this output is started with an “L” output. When using a timer in this mode, set the port $P1_4$ direction register to output mode.

• Event Counter Mode

The operation in the event counter mode is the same as that in the timer mode except that the timer counts the input signal from the $CNTR_0$ pin.
When the $CNTR_0$ active edge switch bit is “0”, the timer counts the rising edge of the $CNTR_0$ pin. When this bit is “1”, the timer counts the falling edge of the $CNTR_0$ pin.

• Pulse Width Measurement Mode

When the $CNTR_0$ active edge switch bit is “0”, the timer counts the signal selected by the timer X count source selection bit while the $CNTR_0$ pin is “H”. When this bit is “1”, the timer counts the signal while the $CNTR_0$ pin is “L”.
In any mode, the timer count can be stopped by setting the timer X count stop bit to “1”. Each time the timer overflows, the interrupt request bit is set.

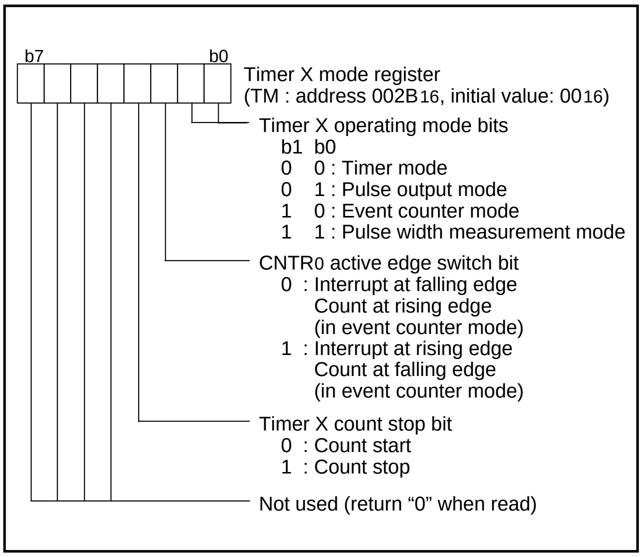


Fig. 22 Structure of timer X mode register

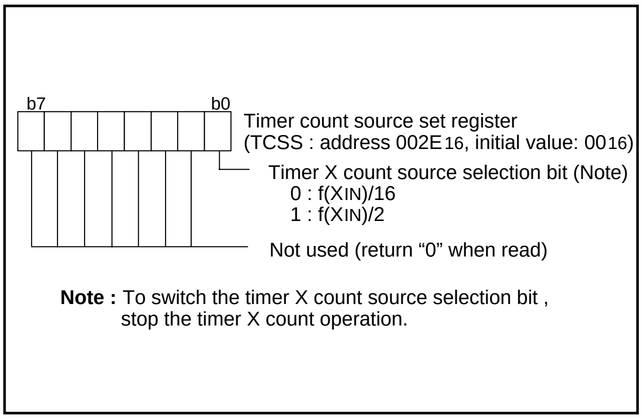


Fig. 23 Timer count source setting register

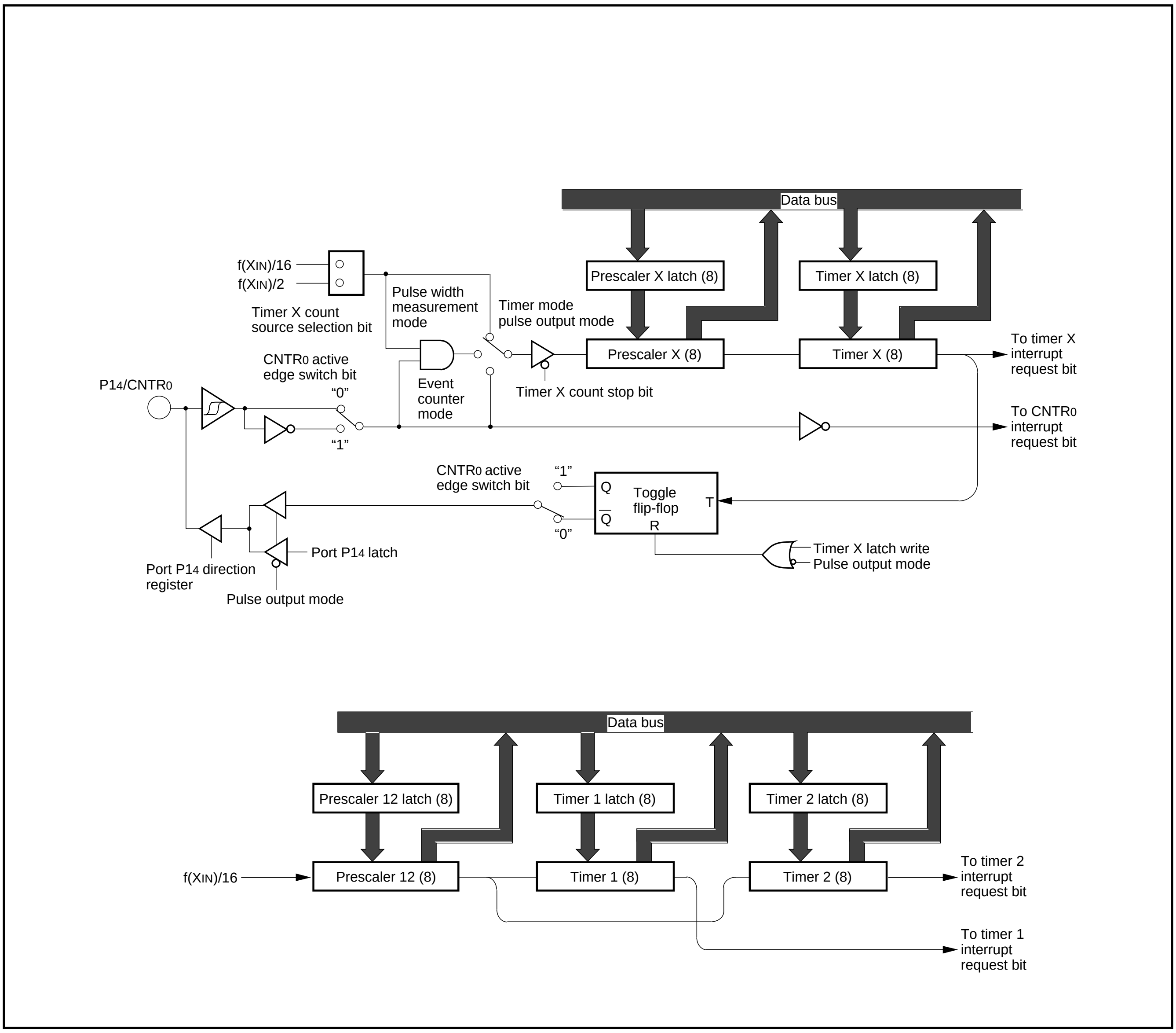


Fig. 24 Block diagram of timer X, timer 1 and timer 2

Serial I/O

●Serial I/O1

Serial I/O1 can be used as an asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation when serial I/O1 is in operation.
Eight serial data transfer formats can be selected, and the transfer formats to be used by a transmitter and a receiver must be identical.
Each of the transmit and receive shift registers has a buffer register (the same address on memory). Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the respective buffer registers. These buffer registers can also hold the next data to be transmitted and receive 2-byte receive data in succession.
By selecting “1” for continuous transmit valid bit (bit 2 of SIO1CON), continuous transmission of the same data is made possible.
This can be used as a simplified PWM.

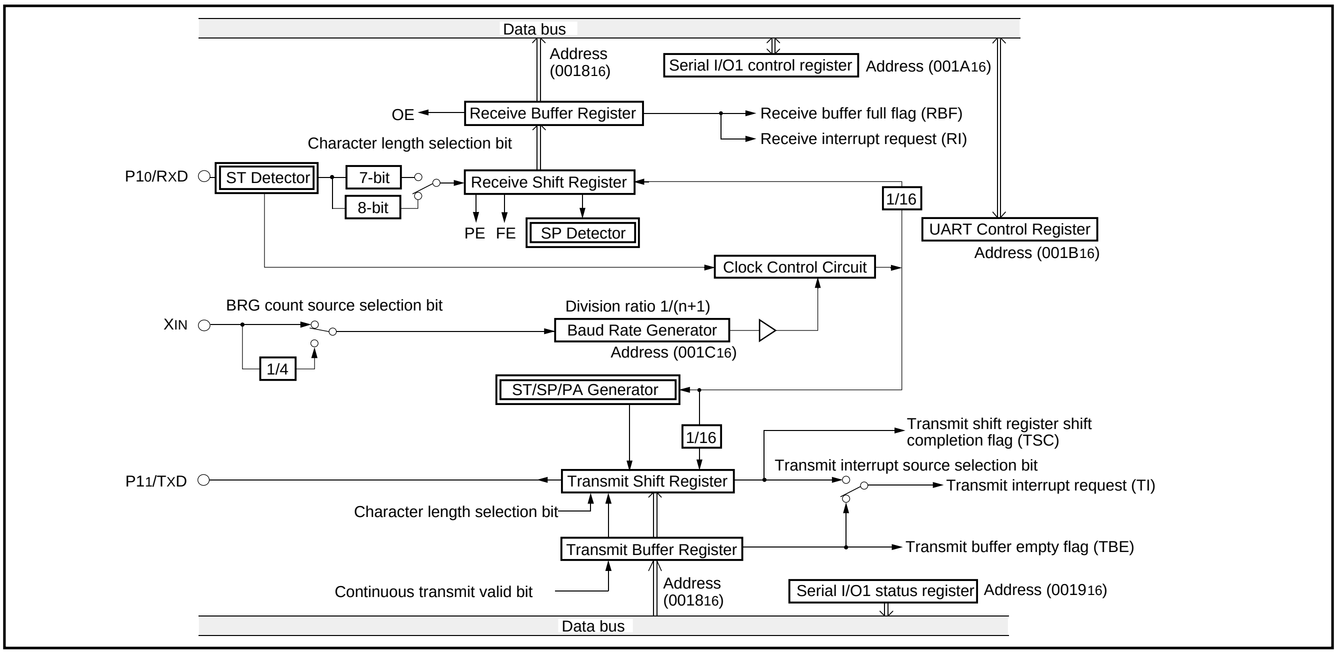
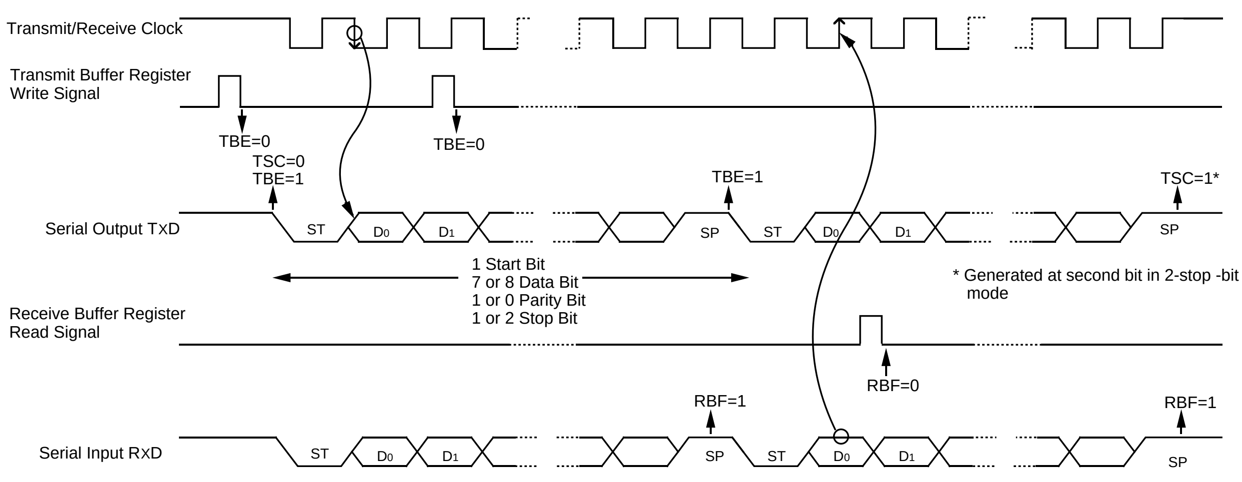


Fig. 25 Block diagram of UART serial I/O



Notes
1 : Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2 : The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes “1”, depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3 : The receive interrupt (RI) is set when the RBF flag becomes “1”.
4 : After data is written to the transmit buffer when TSC = 1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC = 0.

Fig. 26 Operation of UART serial I/O function

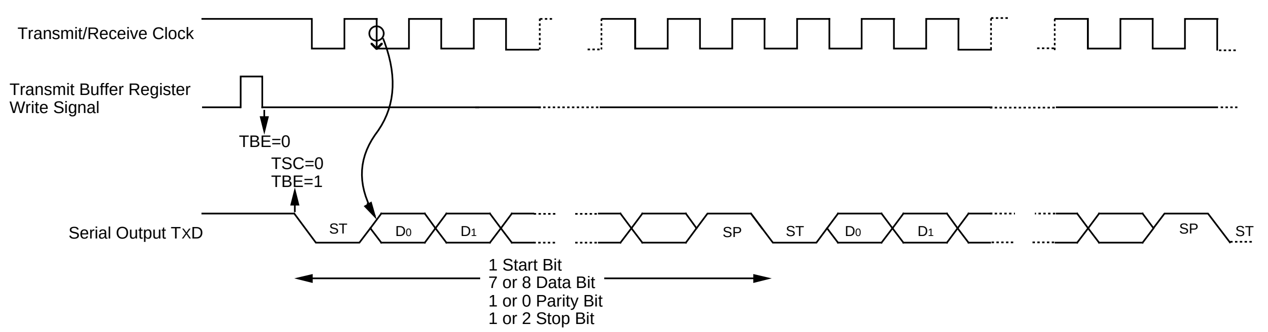
[Serial I/O1 control register] SIO1CON
The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART control register] UARTCON
The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the $P1_1$/TxD pin.

[Serial I/O1 status register] SIO1STS
The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.
The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing “11” to bits 7 and 6 of the serial I/O1 control register initializes this register.
All bits of the serial I/O1 status register are initialized to “81_{16}” at reset.

[Transmit/Receive buffer register] TB/RB
The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7-bit, the MSB of data stored in the receive buffer is "0".

[Baud Rate Generator] BRG
The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.



Notes 1 : When the serial I/O1 enable bit (b7) is “1”, the transmit enable bit is “1”, and continuous transmit valid bit is “1”, writing on the transmit buffer initiates continuous transmission of the same data.
2 : Select 0 for continuous transmit valid bit to stop continuous transmission.
The TxD pin will stop at high level after completing transmission of 1 byte.
3 : If the transmit buffer contents are rewritten during a continuous transmission, transmission of the rewritten data will be started after completing transmission of 1 byte.

Fig. 27 Continuous transmission operation of UART serial I/O

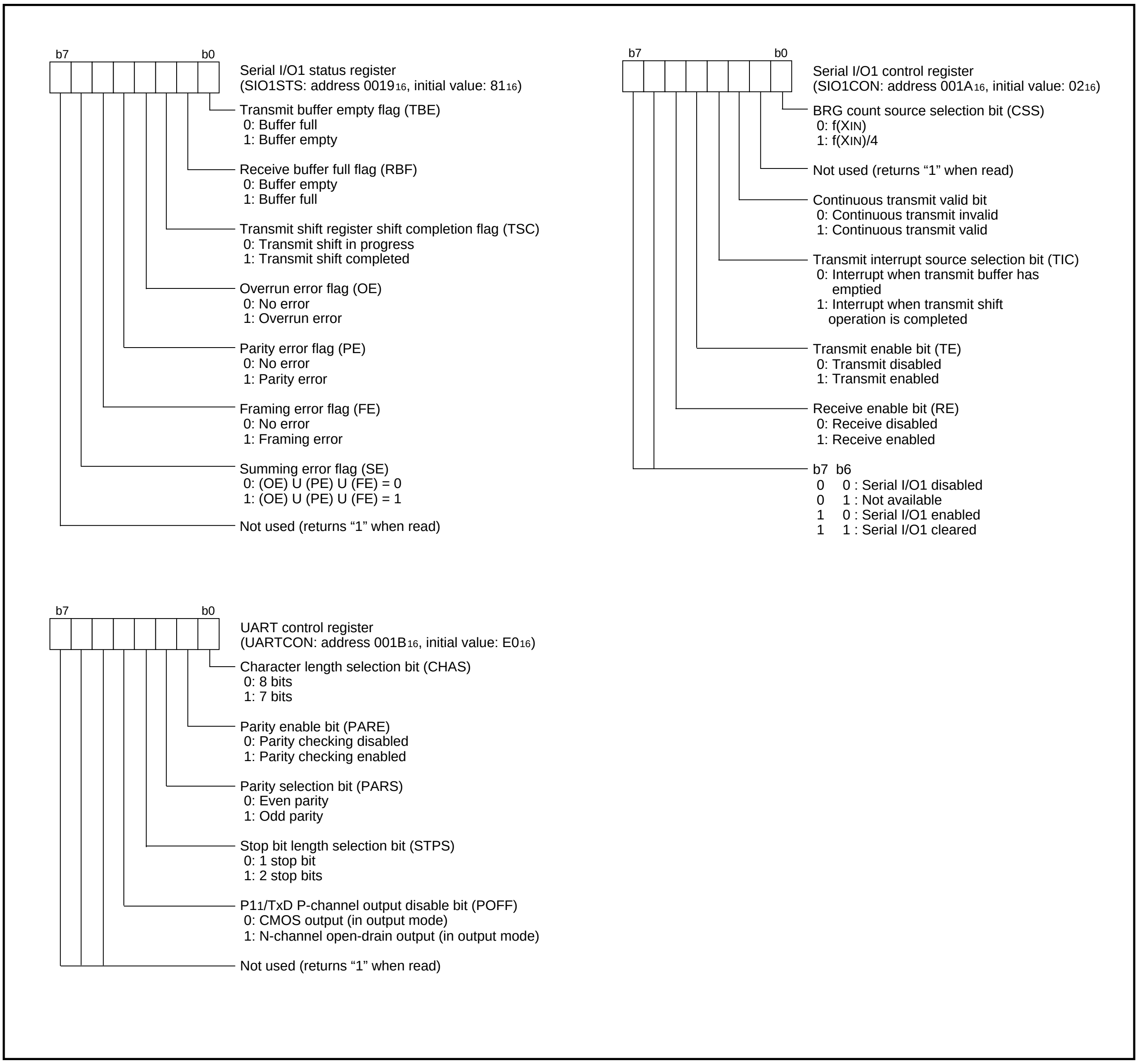


Fig. 28 Structure of serial I/O1-related registers (1)

●Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O2 the transmitter and the receiver must use the same clock. When the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

[Serial I/O2 control register] SIO2CON

The serial I/O2 control register contains 8 bits which control various serial I/O functions.

- Set “0” to bit 3 to receive.
- At reception, clear bit 7 to “0” by writing a dummy data to the serial I/O2 register after completion of shift.
- Bit 7 is set to “1” a half cycle (of the shift clock) earlier than completion of shift operation. Accordingly, when using this bit to confirm shift completion, a half cycle or more of the shift clock must pass after confirming that this bit is set to “1”, before performing read/write to the serial I/O2 register.

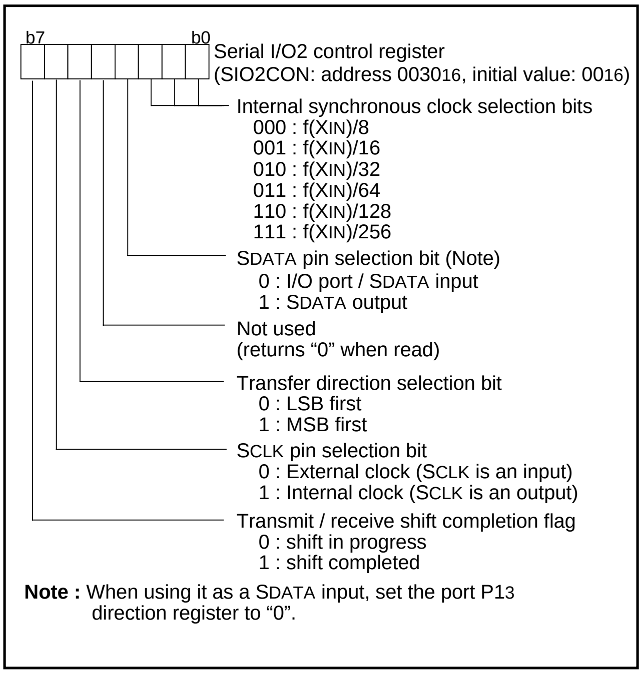


Fig. 29 Structure of serial I/O2 control registers

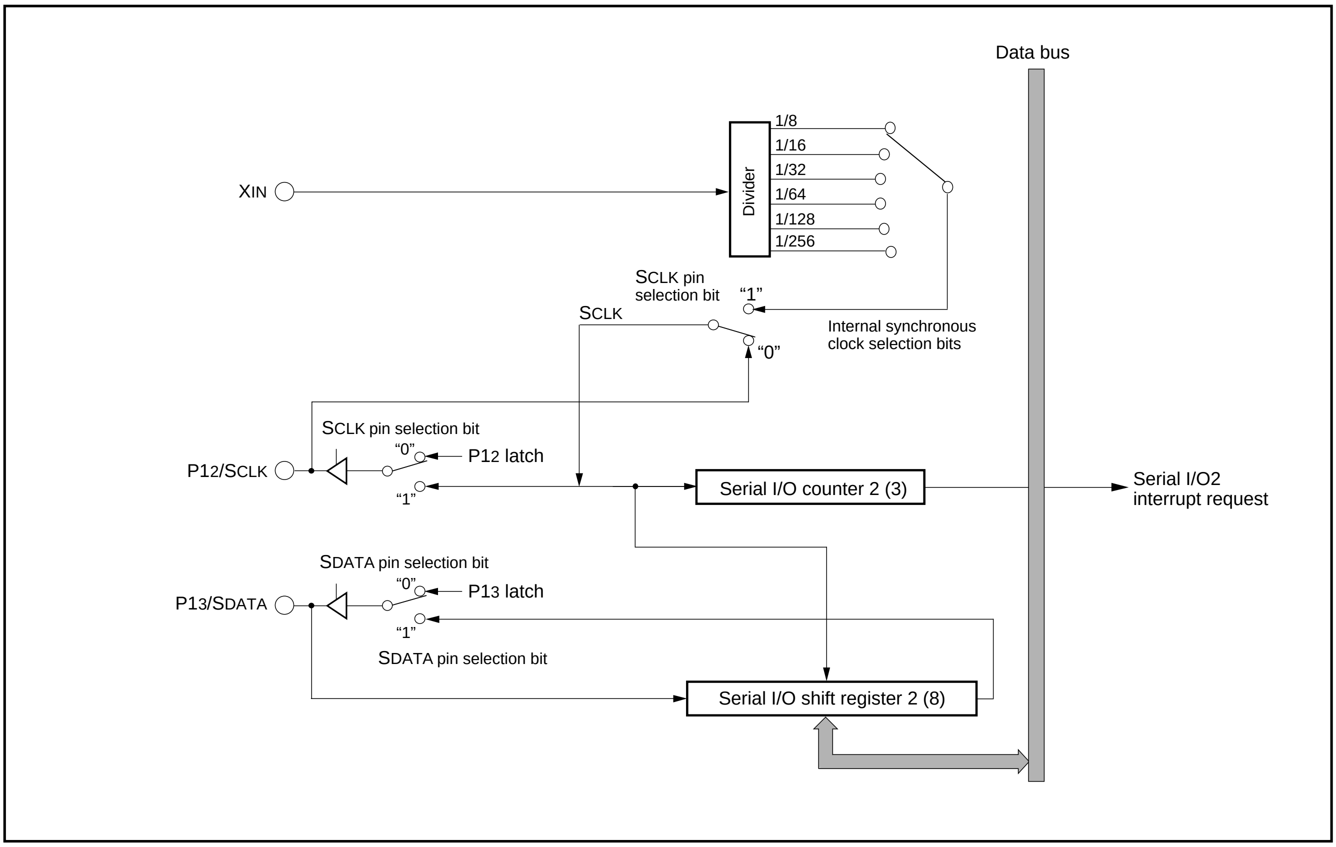


Fig. 30 Block diagram of serial I/O2

Serial I/O2 operation

By writing to the serial I/O2 register (address 0031_{16}) the serial I/O2 counter is set to “7”.

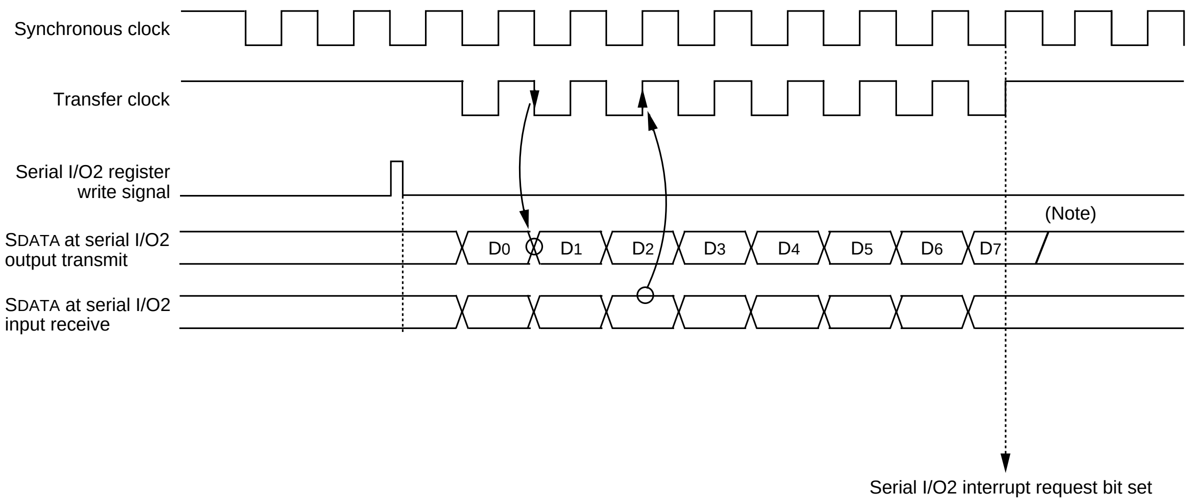
After writing, the SDATA pin outputs data every time the transfer clock shifts from a high to a low level. And, as the transfer clock shifts from a low to a high, the SDATA pin reads data, and at the same time the contents of the serial I/O2 register are shifted by 1 bit.

When the internal clock is selected as the transfer clock source, the following operations execute as the transfer clock counts up to 8.

• Serial I/O2 counter is cleared to “0”.
• Transfer clock stops at an “H” level.
• Interrupt request bit is set.
• Shift completion flag is set.

Also, the SDATA pin is in a high impedance state after the data transfer is complete (refer to figure 31).

When the external clock is selected as the transfer clock source, the interrupt request bit is set as the transfer clock counts up to 8, but external control of the clock is required since it does not stop. Notice that the SDATA pin is not in a high impedance state on the completion of data transfer.



Note : When the internal clock is selected as the transfer and the direction register of P1 3/SDATA pin is set to the input mode, the SDATA pin is in a high impedance state after the data transfer is completed.

Fig. 31 Serial I/O2 timing (LSB first)

A-D Converter

The functional blocks of the A-D converter are described below.

[A-D conversion register] AD

The A-D conversion register is a read-only register that stores the result of A-D conversion. Do not read out this register during an A-D conversion.

[A-D control register] ADCON

The A-D control register controls the A-D converter. Bit 2 to 0 are analog input pin selection bits. Bit 4 is the AD conversion completion bit. The value of this bit remains at “0” during A-D conversion, and changes to “1” at completion of A-D conversion.
A-D conversion is started by setting this bit to “0”.

[Comparison voltage generator]

The comparison voltage generator divides the voltage between V_{SS} and V_{REF} by 1024 by a resistor ladder, and outputs the divided voltages. Since the generator is disconnected from V_{REF} pin and V_{SS} pin, current is not flowing into the resistor ladder.

[Channel Selector]

The channel selector selects one of ports $P2_7/AN_7$ to $P2_0/AN_0$, and inputs the voltage to the comparator.

[Comparator and control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the A-D conversion register. When A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to “1”. Because the comparator is constructed linked to a capacitor, set $f(X_{IN})$ to 500 kHz or more during A-D conversion.

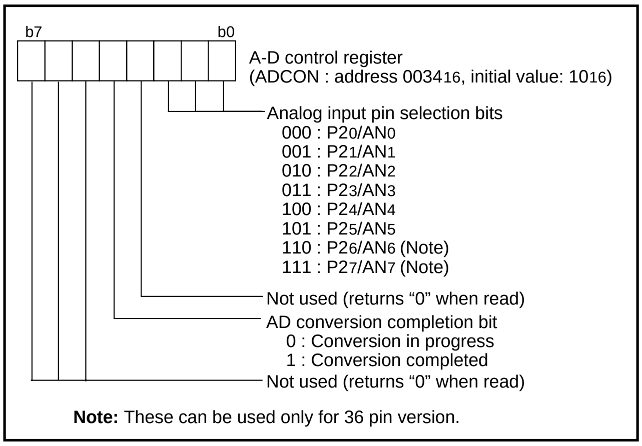


Fig. 32 Structure of A-D control register

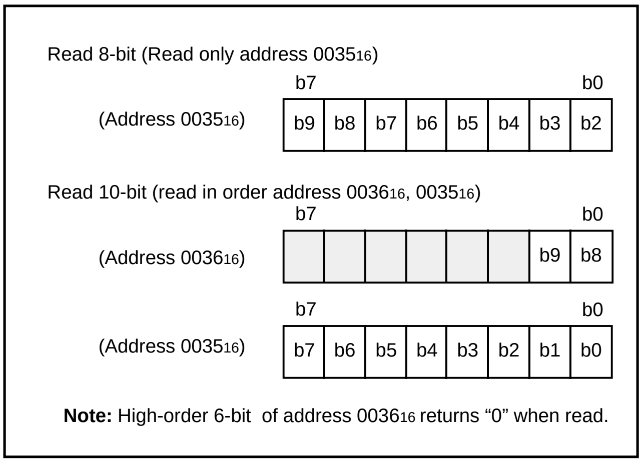


Fig. 33 Structure of A-D conversion register

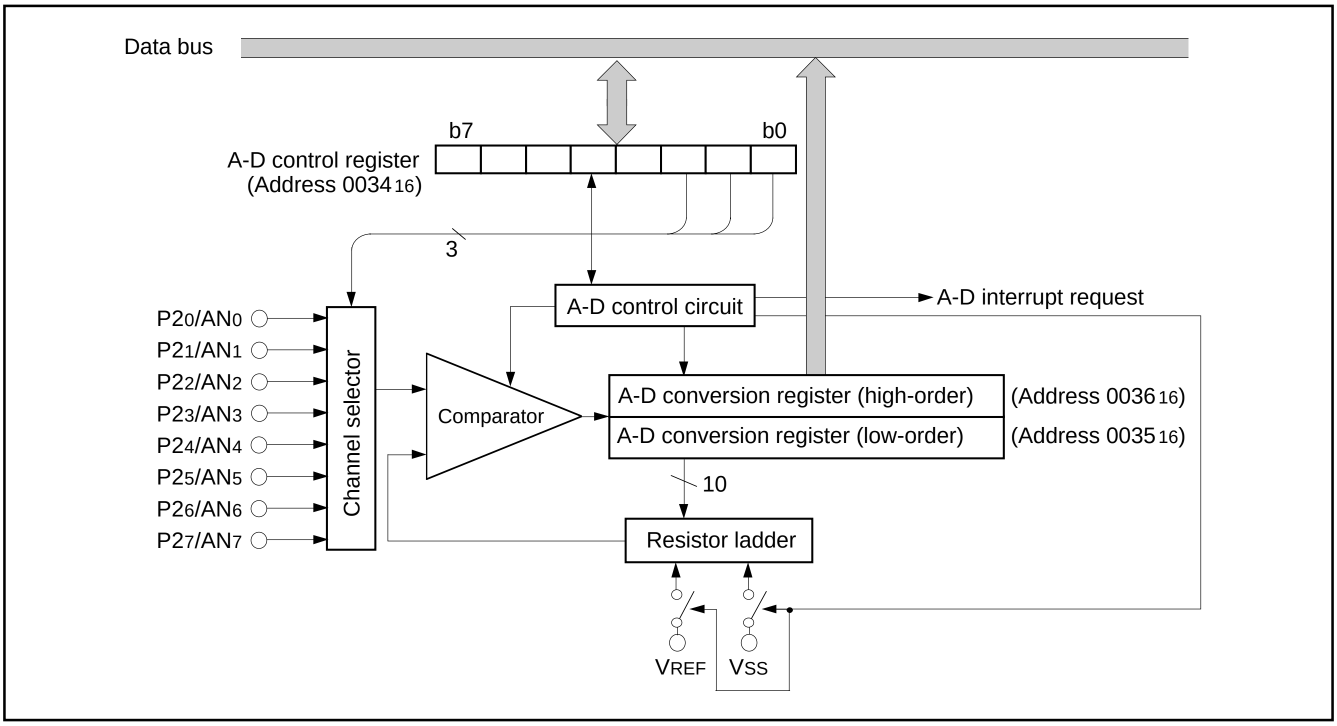


Fig. 34 Block diagram of A-D converter

Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter.

Standard operation of watchdog timer

The watchdog timer stops when the watchdog timer control register (address 0039_{16}) is not set after reset. Writing an optional value to the watchdog timer control register (address 0039_{16}) causes the watchdog timer to start to count down. When the watchdog timer H underflows, an internal reset occurs. Accordingly, it is programmed that the watchdog timer control register (address 0039_{16}) can be set before an underflow occurs.
When the watchdog timer control register (address 0039_{16}) is read, the values of the high-order 6-bit of the watchdog timer H, STP instruction disable bit and watchdog timer H count source selection bit are read.

Initial value of watchdog timer

By a reset or writing to the watchdog timer control register (address 0039_{16}), the watchdog timer H is set to “FF_{16}” and the watchdog timer L is set to “FF_{16}”.

Operation of watchdog timer H count source selection bit

A watchdog timer H count source can be selected by bit 7 of the watchdog timer control register (address 0039_{16}). When this bit is “0”, the count source becomes a watchdog timer L underflow signal. The detection time is 131.072 ms at $f(X_{IN})$=8 MHz.
When this bit is “1”, the count source becomes $f(X_{IN})/16$. In this case, the detection time is 512 µs at $f(X_{IN})$=8 MHz.
This bit is cleared to “0” after reset.

Operation of STP instruction disable bit

When the watchdog timer is in operation, the STP instruction can be disabled by bit 6 of the watchdog timer control register (address 0039_{16}).
When this bit is “0”, the STP instruction is enabled.
When this bit is “1”, the STP instruction is disabled, and an internal reset occurs if the STP instruction is executed.
Once this bit is set to “1”, it cannot be changed to “0” by program.
This bit is cleared to “0” after reset.

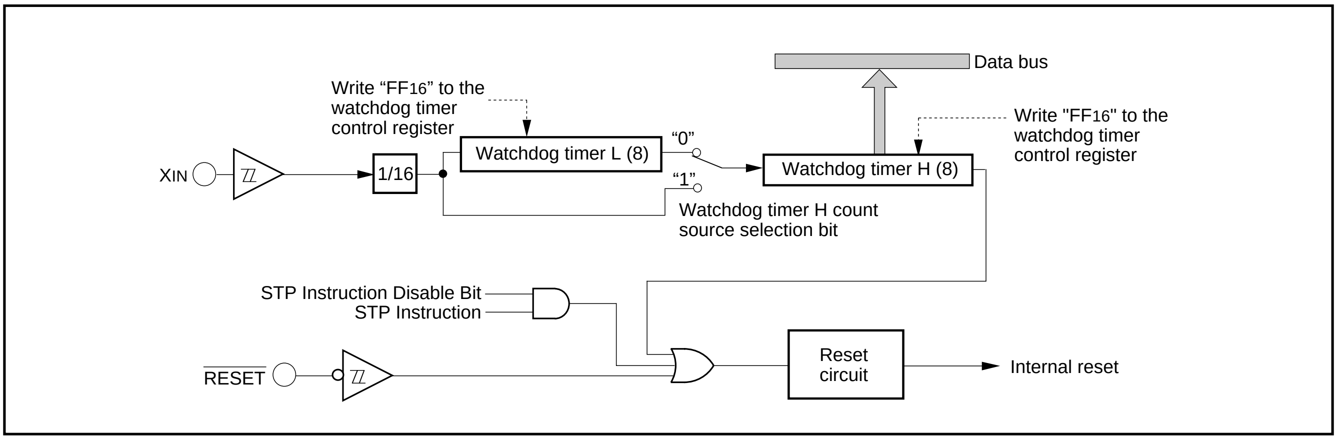


Fig. 35 Block diagram of watchdog timer

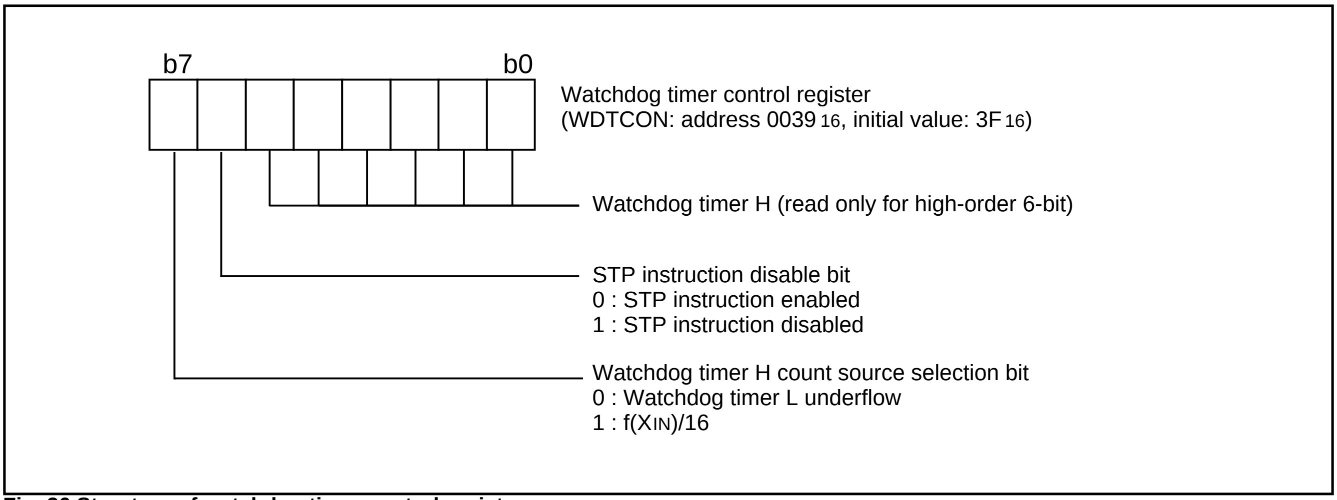


Fig. 36 Structure of watchdog timer control register

Reset Circuit

The microcomputer is put into a reset status by holding the RESET pin at the “L” level for the following interval or more according to the power source voltage and X_{IN} is in stable oscillation.
After that, this reset status is released by returning the RESET pin to the “H” level. The program starts from the address having the contents of address $FFFD_{16}$ as high-order address and the contents of address $FFFC_{16}$ as low-order address.
When V_{CC} = 2.2 to 5.5 V, reset input “L” interval is 45 µs or more
When V_{CC} = 2.4 to 5.5 V, reset input “L” interval is 35 µs or more
When V_{CC} = 4.0 to 5.5 V, reset input “L” interval is 15 µs or more

In the case of f(ϕ) ≤ 4 MHz, the reset input voltage must be 0.8 V or less when the power source voltage passes 4.0 V.
In the case of f(ϕ) ≤ 2 MHz, the reset input voltage must be 0.48 V or less when the power source voltage passes 2.4 V.
In the case of f(ϕ) ≤ 1 MHz, the reset input voltage must be 0.44 V or less when the power source voltage passes 2.2 V.

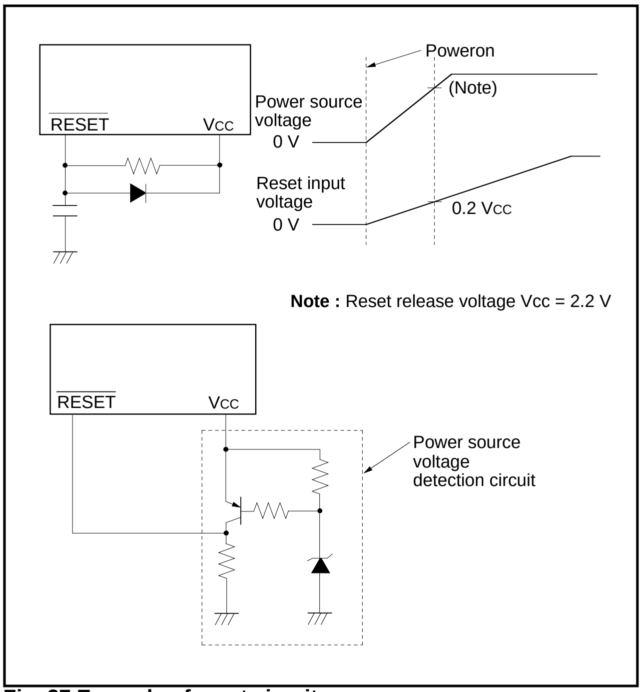


Fig. 37 Example of reset circuit

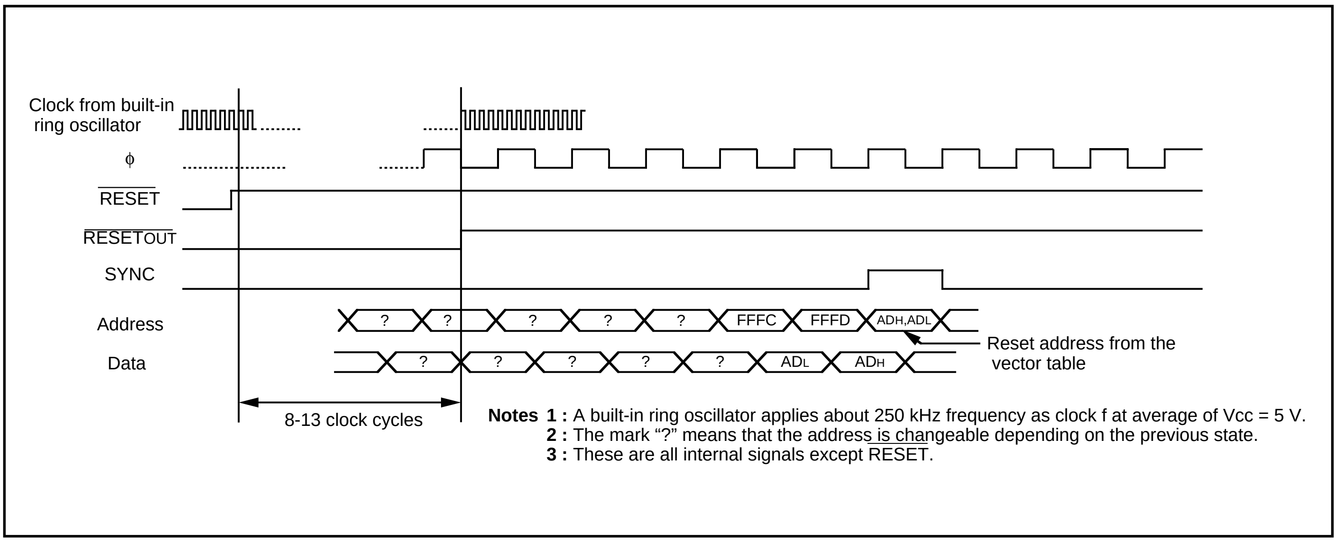


Fig. 38 Timing diagram at reset

	Register	Address	Register contents							
(1)	Port P0 direction register	0001_{16}	00_{16}							
(2)	Port P1 direction register	0003_{16}	X	X	X	0	0	0	0	0
(3)	Port P2 direction register	0005_{16}	00_{16}							
(4)	Port P3 direction register	0007_{16}	00_{16}							
(5)	Pull-up control register	0016_{16}	FF_{16}							
(6)	Port P1P3 control register	0017_{16}	00_{16}							
(7)	Serial I/O1 status register	0019_{16}	1	0	0	0	0	0	0	1
(8)	Serial I/O1 control register	$001A_{16}$	02_{16}							
(9)	UART control register	$001B_{16}$	1	1	1	0	0	0	0	0
(10)	Prescaler 12	0028_{16}	FF_{16}							
(11)	Timer 1	0029_{16}	01_{16}							
(12)	Timer 2	$002A_{16}$	00_{16}							
(13)	Timer X mode register	$002B_{16}$	00_{16}							
(14)	Prescaler X	$002C_{16}$	FF_{16}							
(15)	Timer X	$002D_{16}$	FF_{16}							
(16)	Timer count source set register	$002E_{16}$	00_{16}							
(17)	Serial I/O2 control register	0030_{16}	00_{16}							
(18)	A-D control register	0034_{16}	10_{16}							
(19)	MISRG	0038_{16}	00_{16}							
(20)	Watchdog timer control register	0039_{16}	0	0	1	1	1	1	1	1
(21)	Interrupt edge selection register	$003A_{16}$	00_{16}							
(22)	CPU mode register	$003B_{16}$	1	0	0	0	0	0	0	0
(23)	Interrupt request register 1	$003C_{16}$	00_{16}							
(24)	Interrupt control register 1	$003E_{16}$	00_{16}							
(25)	Processor status register	(PS)	X	X	X	X	X	1	X	X
(26)	Program counter	(PC_H)	Contents of address $FFFD_{16}$							
		(PC_L)	Contents of address $FFFC_{16}$							

Note X : Undefined

Fig. 39 Internal status of microcomputer at reset

Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between X_{IN} and X_{OUT}, and an RC oscillation circuit can be formed by connecting a resistor and a capacitor.
Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between X_{IN} and X_{OUT} since a feed-back resistor exists on-chip.
Set the constants of the resistor and capacitor when an RC oscillator is used, so that a frequency variation due to LSI variation and resistor and capacitor variations may not exceed the standard input frequency.

●Oscillation control

• Stop mode

When the STP instruction is executed, the internal clock f stops at an “H” level and the X_{IN} oscillator stops. At this time, timer 1 is set to “01_{16}” and prescaler 12 is set to “FF_{16}” when the oscillation stabilization time set bit after release of the STP instruction is “0”. On the other hand, timer 1 and prescaler 12 are not set when the above bit is “1”. Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used. f(X_{IN})/16 is forcibly connected to the input of prescaler 12. When an external interrupt is accepted, oscillation is restarted but the internal clock f remains at “H” until timer 1 underflows. As soon as timer 1 underflows, the internal clock f is supplied. This is because when a ceramic oscillator is used, some time is required until a start of oscillation. In case oscillation is restarted by reset, no wait time is generated. So apply an “L” level to the $\overline{\text{RESET}}$ pin while oscillation becomes stable.

• Wait mode

If the WIT instruction is executed, the internal clock f stops at an “H” level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to “1” before the STP or WIT instruction is executed.
When the STP status is released, prescaler 12 and timer 1 will start counting clock which is X_{IN} divided by 16, so set the timer 1 interrupt enable bit to “0” before the STP instruction is executed.

Note

For use with the oscillation stabilization set bit after release of the STP instruction set to “1”, set values in timer 1 and prescaler 12 after fully appreciating the oscillation stabilization time of the oscillator to be used.

●Switch of ceramic and RC oscillations

After releasing reset the operation starts by starting a built-in ring oscillator. Then, a ceramic oscillation or an RC oscillation is selected by setting bit 5 of the CPU mode register.
The bit 5 can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit.

●Double-speed mode

When a ceramic oscillation is selected, a double-speed mode can be used. Do not use it when an RC oscillation is selected.

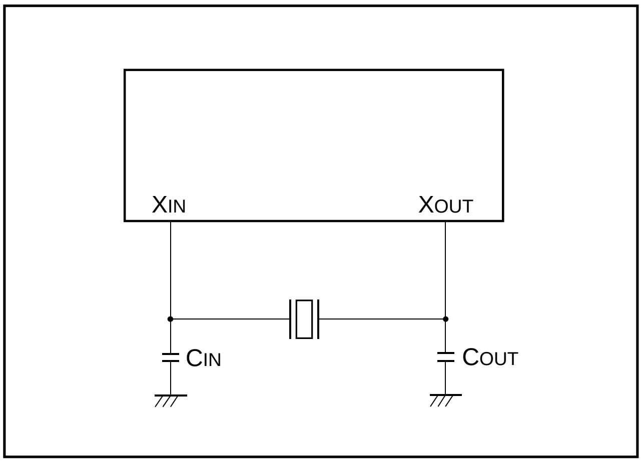


Fig. 40 External circuit of ceramic resonator

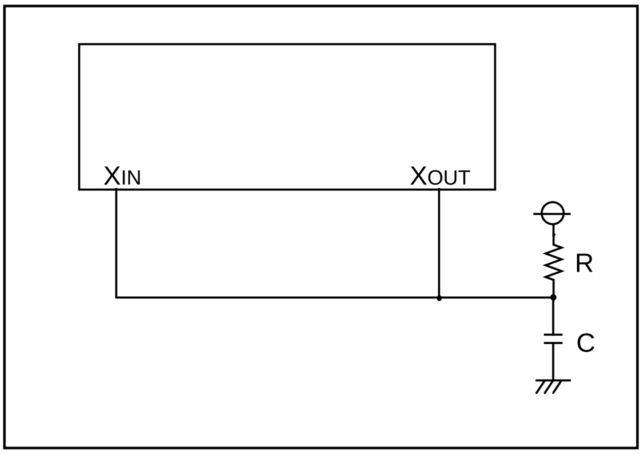


Fig. 41 External circuit of RC oscillation

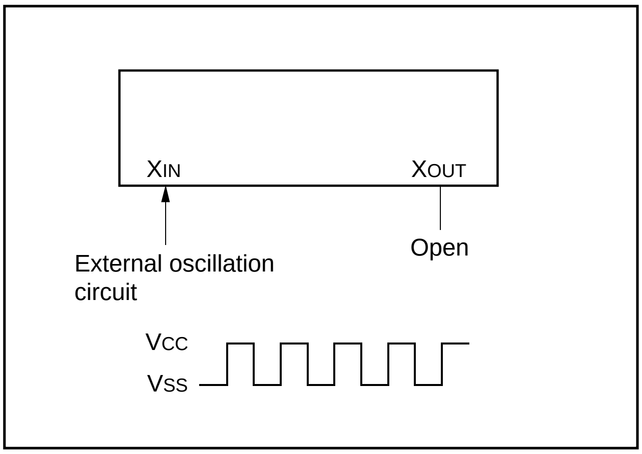


Fig. 42 External clock input circuit

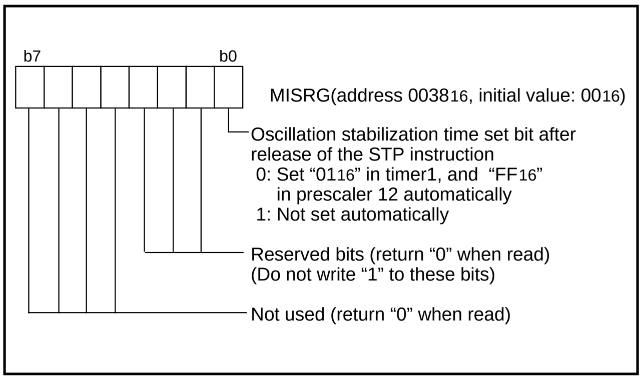


Fig. 43 Structure of MISRG

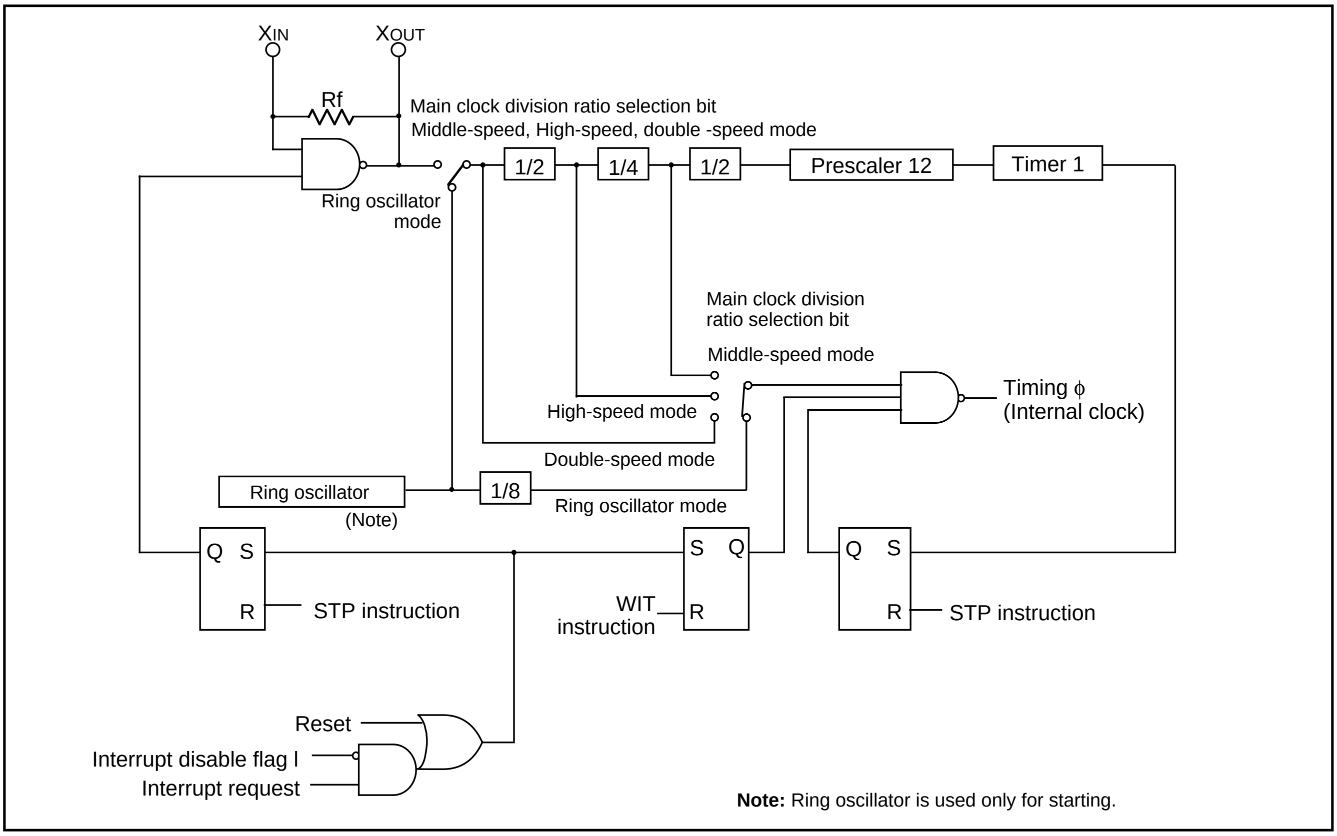


Fig. 44 Block diagram of internal clock generating circuit (for ceramic resonator)

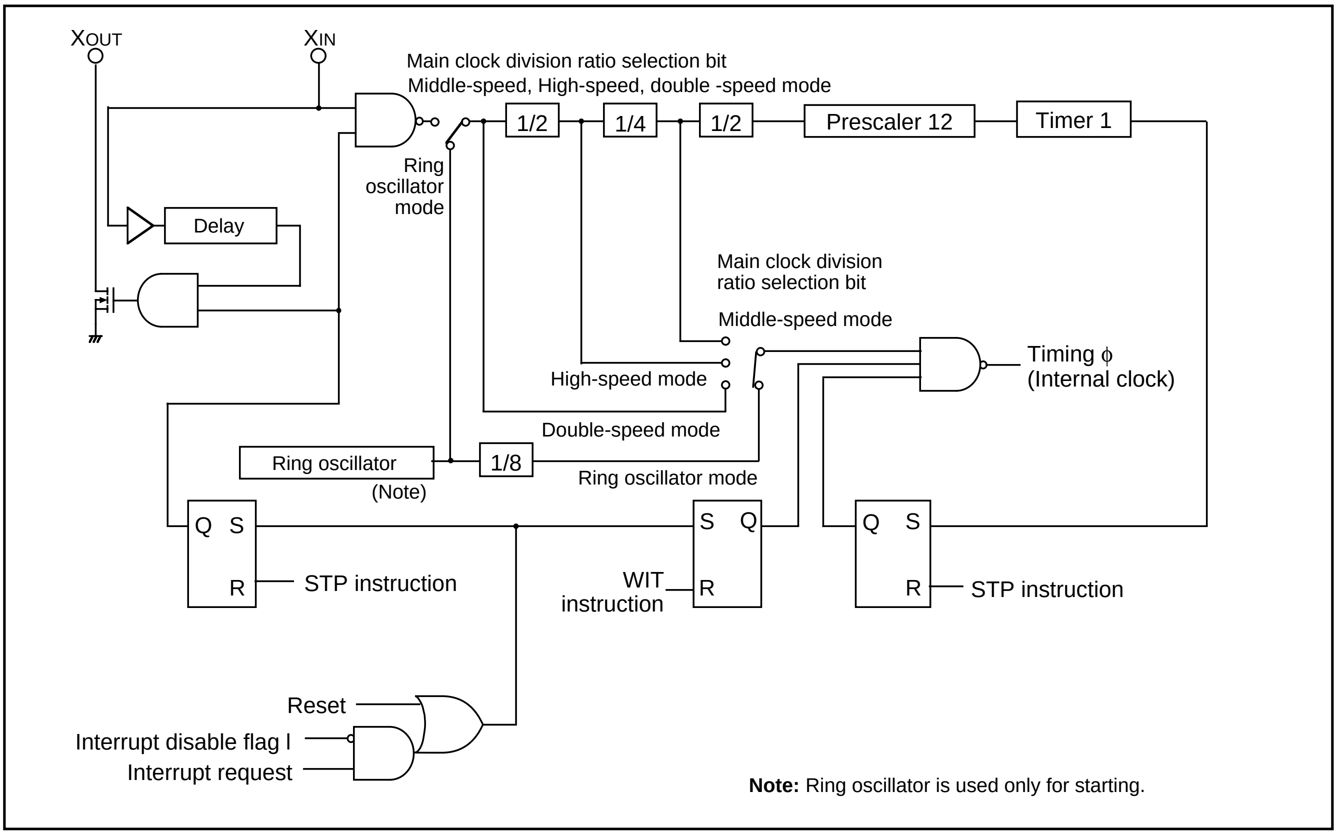


Fig. 45 Block diagram of internal clock generating circuit (for RC oscillation)

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is “1”. After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations.

Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

Decimal Calculations

- For calculations in decimal notation, set the decimal mode flag D to “1”, then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.
- In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

Timers

- When n (0 to 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
- When a count source of timer X is switched, stop a count of timer X.

Ports

- The values of the port direction registers cannot be read.
  That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is “1”, addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.
  It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.
  For setting direction registers, use the LDM instruction, STA instruction, etc.
- Set "1" to each bit 6 of the port P3 direction register and the port P3 register.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Make sure that f(X_{IN}) is 500kHz or more during A-D conversion.
Do not execute the STP instruction during A-D conversion.

Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.
The frequency of the internal clock ϕ is the same as that of the X_{IN} in double-speed mode, twice the X_{IN} cycle in high-speed mode and 8 times the X_{IN} cycle in middle-speed mode.

CPU Mode Register

The oscillation mode selection bit can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit.
When a ceramic oscillation is selected, a double-speed mode of the clock division ratio selection bits can be used. Do not use it when an RC oscillation is selected.

NOTES ON USE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 µF to 0.1 µF is recommended.

One Time PROM Version

The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.
To improve the noise reduction, connect a track between CNVss pin and Vss pin with 1 to 10 kΩ resistance.
The mask ROM version track of CNVss pin has no operational interference even if it is connected via a resistor.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form
(three identical copies)

DATA REQUIRED FOR ROM PROGRAMMING ORDERS

The following are necessary when ordering a ROM writing:

(1) ROM Programming Confirmation Form
(2) Mark Specification Form (for Special Mark)
(3) Data to be written to ROM, in EPROM form
(three identical copies)

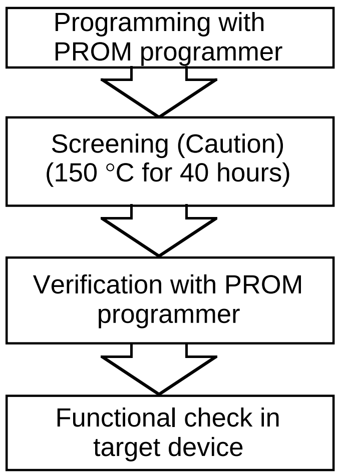
ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 7 Special programming adapter

Package	Name of Programming Adapter
32P4B	PCA7435SP
32P6B-A	PCA7435GP
36P2R-A	PCA7435FP

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 46 is recommended to verify programming.



Caution: The screening temperature is far higher than the storage temperature. Never expose to 150 °C exceeding 100 hours.

Fig. 46 Programming and testing of One Time PROM version

FUNCTIONAL DESCRIPTION SUPPLEMENT

Interrupt

7531 group permits interrupts on the basis of 12 (11 sources for 32-pin version) sources. It is vector interrupts with a fixed priority system. Accordingly, when two or more interrupt requests occur during the same sampling, the higher-priority interrupt is accepted first. This priority is determined by hardware, but variety of priority processing can be performed by software, using an interrupt enable bit and an interrupt disable flag.
For interrupt sources, vector addresses and interrupt priority, refer to **"Table 8."**

Table 8 Interrupt sources, vector addresses and interrupt priority

Priority	Interrupt sources	Vector addresses		Remarks
		High-order	Low-order	
1	Reset (Note 1)	$FFFD_{16}$	$FFFC_{16}$	Non-maskable
2	Serial I/O1 receive interrupt	$FFFB_{16}$	$FFFA_{16}$	Valid when serial I/O1 is selected
3	Serial I/O1 transmit interrupt	$FFF9_{16}$	$FFF8_{16}$	Valid when serial I/O1 is selected
	INT_1 interrupt (Note 2)			External interrupt (active edge selectable)
4	INT_0 interrupt	$FFF7_{16}$	$FFF6_{16}$	External interrupt (active edge selectable)
5	Timer X interrupt	$FFF5_{16}$	$FFF4_{16}$	
	Key on wake up interrupt			External interrupt (only at falling edge)
6	Timer 1 interrupt	$FFF3_{16}$	$FFF2_{16}$	STP instruction release timer underflow
7	Timer 2 interrupt	$FFF1_{16}$	$FFF0_{16}$	
	Serial I/O2 interrupt			
8	$CNTR_0$ interrupt	$FFEF_{16}$	$FFEE_{16}$	External interrupt (active edge selectable)
	A-D conversion interrupt			
9	BRK instruction interrupt	$FFED_{16}$	$FFEC_{16}$	Non-maskable software interrupt

Notes 1: Reset functions in the same way as an interrupt with the highest priority.
2: It is available for 36-pin version.

Timing After Interrupt

The interrupt processing routine begins with the machine cycle following the completion of the instruction that is currently in execution.

Figure 47 shows a timing chart after an interrupt occurs, and Figure 48 shows the time up to execution of the interrupt processing routine.

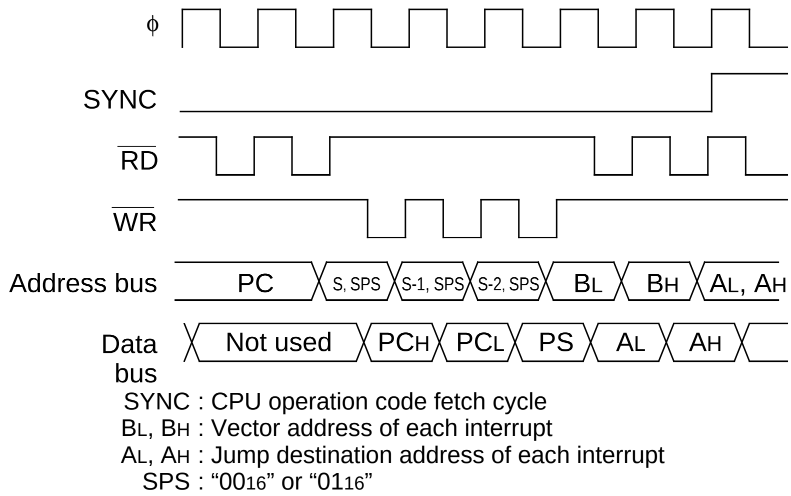


Fig. 47 Timing chart after an interrupt occurs

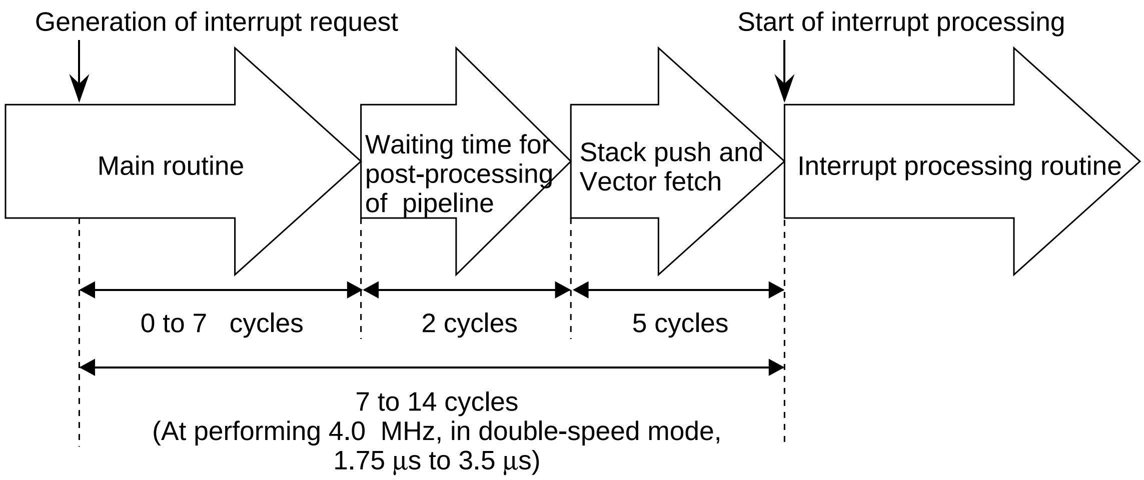


Fig. 48 Time up to execution of the interrupt processing routine

A-D Converter

A-D conversion is started by setting AD conversion completion bit to “0.” During A-D conversion, internal operations are performed as follows.

1. After the start of A-D conversion, A-D conversion register goes to “00_{16}.”
2. The highest-order bit of A-D conversion register is set to “1,” and the comparison voltage Vref is input to the comparator. Then, Vref is compared with analog input voltage V_{IN}.
3. As a result of comparison, when Vref < V_{IN}, the highest-order bit of A-D conversion register becomes “1.” When Vref > V_{IN}, the highest-order bit becomes “0.”

By repeating the above operations up to the lowest-order bit of the A-D conversion register, an analog value converts into a digital value.
A-D conversion completes at 122 clock cycles (15.25 µs at $f(X_{IN})$ = 8.0 MHz) after it is started, and the result of the conversion is stored into the A-D conversion register.
Concurrently with the completion of A-D conversion, A-D conversion interrupt request occurs, so that the AD conversion interrupt request bit is set to “1.”

Relative formula for a reference voltage VREF of A-D converter and Vref

When n = 0 Vref = 0

When n = 1 to 1023 $\text{Vref} = \dfrac{V_{REF}}{1024} \times n$

n : the value of A-D converter (decimal numeral)

Table 9 Change of A-D conversion register during A-D conversion

	Change of A-D conversion register	Value of comparison voltage (Vref)
At start of conversion	0 0 0 0 0 0 0 0 0 0	0
First comparison	1 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2}$
Second comparison	*1 1 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4}$
Third comparison	*1 *2 1 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8}$
⋮	⋮	⋮
After completion of tenth comparison	A result of A-D conversion *1 *2 *3 *4 *5 *6 *7 *8 *9 *10	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \cdots \pm \frac{V_{REF}}{1024}$

✻1–✻10: A result of the first to tenth comparison

Figure 49 shows A-D conversion equivalent circuit, and Figure 50 shows A-D conversion timing chart.

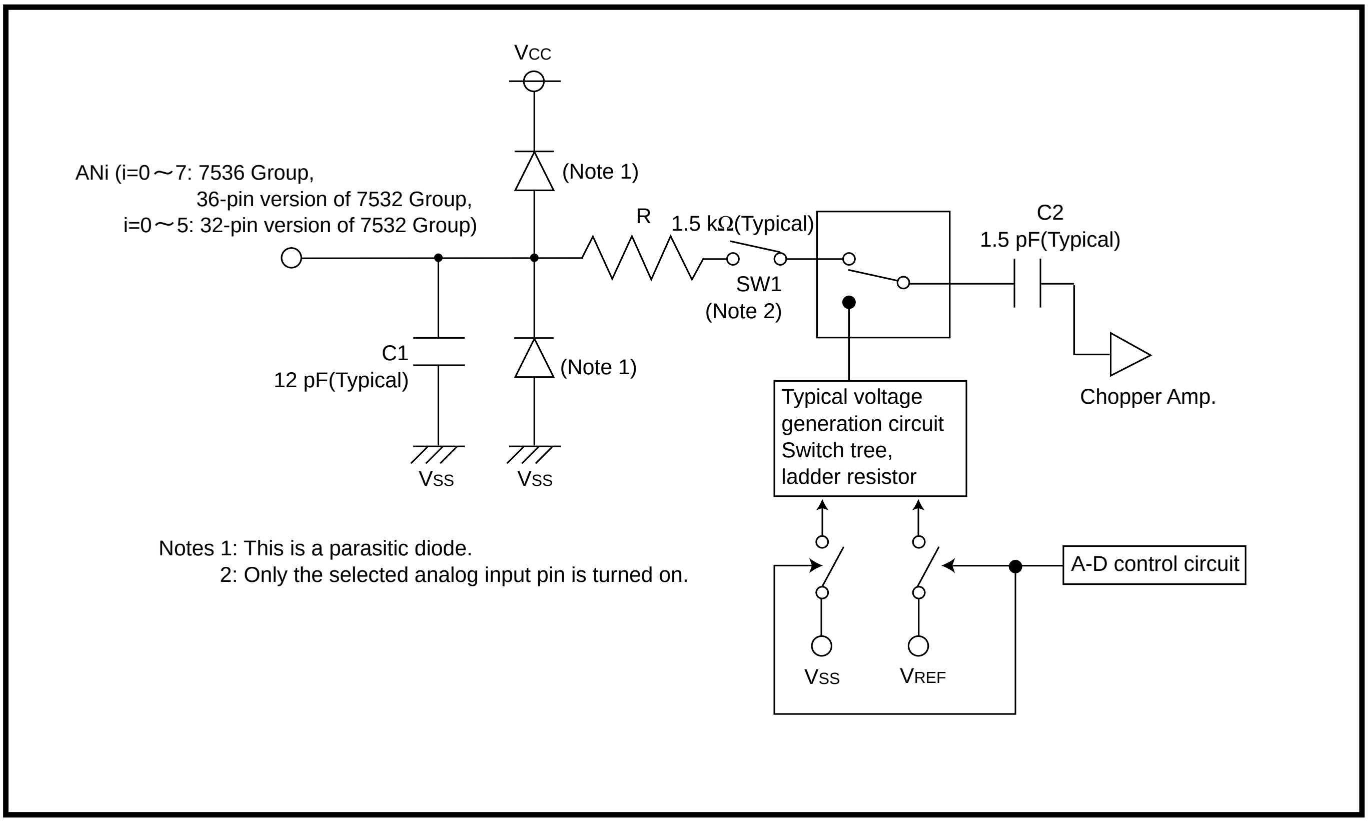


Fig. 49 A-D conversion equivalent circuit

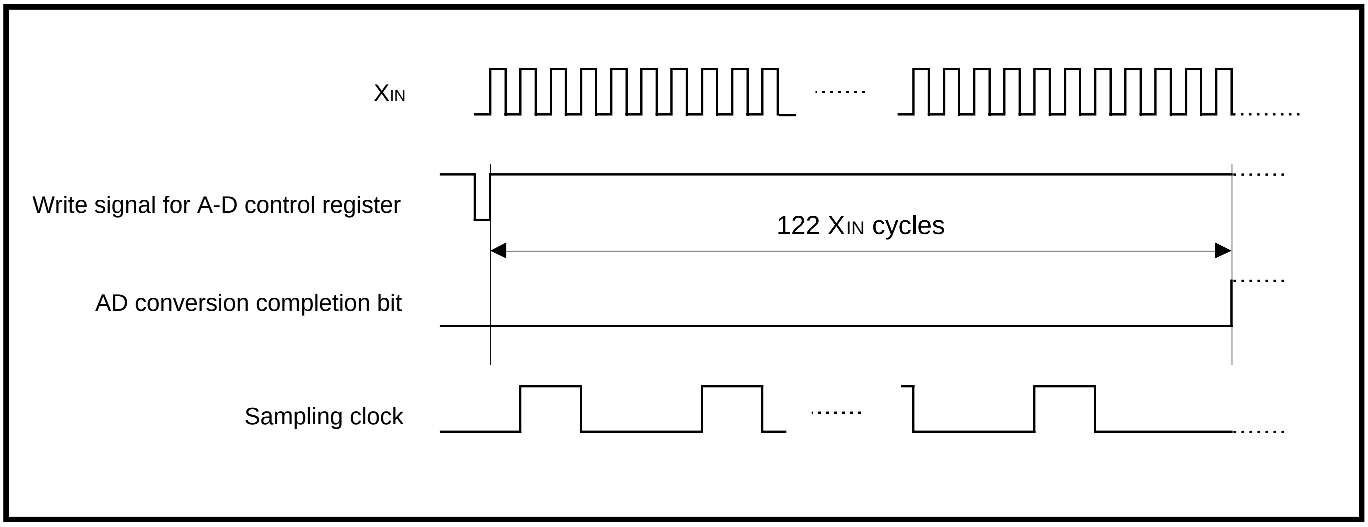


Fig. 50 A-D conversion timing chart

CHAPTER 2

APPLICATION

2.1 I/O port
2.2 Timer
2.3 Serial I/O
2.4 A-D converter
2.5 Reset

2.1 I/O port

This paragraph explains the registers setting method and the notes relevant to the I/O ports.

2.1.1 Memory map

Address	Register
0000_{16}	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)

Fig. 2.1.1 Memory map of registers relevant to I/O port

2.1.2 Relevant registers

Port Pi

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi (Pi) (i = 0, 2, 3) [Address : 00_{16}, 04_{16}, 06_{16}]

B	Name	Function	At reset	R	W
0	Port Pi_0	• In output mode Write, Read : Port latch • In input mode Write : Port latch Read : Value of pins	?	○	○
1	Port Pi_1		?	○	○
2	Port Pi_2		?	○	○
3	Port Pi_3		?	○	○
4	Port Pi_4		?	○	○
5	Port Pi_5		?	○	○
6	Port Pi_6		?	○	○
7	Port Pi_7		?	○	○

Note: The 32-pin package versions have nothing to be allocated for the following:
- Bits 6 and 7 of port P2
- Bits 5 and 6 of port P3.

Fig. 2.1.2 Structure of Port Pi (i = 0, 2, 3)

Port P1

b7 b6 b5 b4 b3 b2 b1 b0

Port P1 (P1) [Address : 02_{16}]

B	Name	Function	At reset	R	W
0	Port $P1_0$	• In output mode Write } Port latch Read } • In input mode Write : Port latch Read : Value of pins	?	○	○
1	Port $P1_1$		?	○	○
2	Port $P1_2$		?	○	○
3	Port $P1_3$		?	○	○
4	Port $P1_4$		?	○	○
5	Nothing is allocated for these bits. When these bits are read out, the values are undefined.		?	×	×
6			?	×	×
7			?	×	×

Fig. 2.1.3 Structure of Port P1

Port Pi direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi direction register (PiD) (i = 0, 2, 3) [Address : 01_{16}, 05_{16}, 07_{16}]

B	Name	Function	At reset	R	W
0	Port Pi direction register	0 : Port Pi_0 input mode 1 : Port Pi_0 output mode	0	×	○
1		0 : Port Pi_1 input mode 1 : Port Pi_1 output mode	0	×	○
2		0 : Port Pi_2 input mode 1 : Port Pi_2 output mode	0	×	○
3		0 : Port Pi_3 input mode 1 : Port Pi_3 output mode	0	×	○
4		0 : Port Pi_4 input mode 1 : Port Pi_4 output mode	0	×	○
5		0 : Port Pi_5 input mode 1 : Port Pi_5 output mode	0	×	○
6		0 : Port Pi_6 input mode 1 : Port Pi_6 output mode	0	×	○
7		0 : Port Pi_7 input mode 1 : Port Pi_7 output mode	0	×	○

Note: The 32-pin package versions have nothing to be allocated for the following:
- Bits 6 and 7 of P2D
- Bits 5 and 6 of P3D.

Fig. 2.1.4 Structure of Port Pi direction register (i = 0, 2, 3)

Port P1 direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port P1 direction register (P1D) [Address : 03$_{16}$]

B	Name	Function	At reset	R	W
0	Port P1 direction register	0 : Port $P1_0$ input mode 1 : Port $P1_0$ output mode	0	×	○
1		0 : Port $P1_1$ input mode 1 : Port $P1_1$ output mode	0	×	○
2		0 : Port $P1_2$ input mode 1 : Port $P1_2$ output mode	0	×	○
3		0 : Port $P1_3$ input mode 1 : Port $P1_3$ output mode	0	×	○
4		0 : Port $P1_4$ input mode 1 : Port $P1_4$ output mode	0	×	○
5	Nothing is allocated for these bits. When these bits are read out, the values are undefined.		?	×	×
6			?	×	×
7			?	×	×

Fig. 2.1.5 Structure of Port P1 direction register

Pull-up control register

b7 b6 b5 b4 b3 b2 b1 b0

Pull-up control register (PULL) [Address : 16$_{16}$]

B	Name	Function	At reset	R	W
0	$P0_0$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
1	$P0_1$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
2	$P0_2$, $P0_3$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
3	$P0_4$ – $P0_7$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
4	$P3_0$ – $P3_3$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
5	$P3_4$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
6	$P3_5$, $P3_6$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
7	$P3_7$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○

Notes 1: Pins set to output are disconnected from the pull-up control.
2: Keep setting the $P3_5$, $P3_6$ pull-up control bit to “1” (initial value) for the 32-pin package versions.

Fig. 2.1.6 Structure of Pull-up control register

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt edge selection register (INTEDGE) [Address : $3A_{16}$]

B	Name	Function	At reset	R	W
0	INT_0 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
1	INT_1 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
2	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".		0	○	×
3			0	○	×
4	Serial I/O1 or INT_1 interrupt selection bit (**Note**)	0 : Serial I/O1 1 : INT_1	0	○	○
5	Timer X or key-on wake up interrupt selection bit	0 : Timer X 1 : Key-on wake up	0	○	○
6	Timer 2 or serial I/O2 interrupt selection bit	0 : Timer 2 1 : Serial I/O2	0	○	○
7	$CNTR_0$ or AD converter interrupt selection bit	0 : $CNTR_0$ 1 : AD converter	0	○	○

Note: Do not write "1" to bit 4 in the 32-pin package versions.

Fig. 2.1.7 Structure of Interrupt edge selection register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address : $3C_{16}$]

B	Name	Function	At reset	R	W
0	Serial I/O1 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
1	Serial I/O1 transmit or INT_1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
2	INT_0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
3	Timer X or key-on wake up interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
4	Timer 1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
5	Timer 2 or serial I/O2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
6		0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0".		0	○	×

✻: These bits can be cleared to "0" by program, but cannot be set.

Fig. 2.1.8 Structure of Interrupt request register 1

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address : $3E_{16}$]

B	Name	Function	At reset	R	W
0	Serial I/O1 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Serial I/O1 transmit or INT_1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	INT_0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Timer X or key-on wake up interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Timer 2 or serial I/O2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	$CNTR_0$ or AD converter interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Nothing is allocated for this bit. Do not write “1” to this bit. When this bit is read out, the value is “0”.		0	○	×

Fig. 2.1.9 Structure of Interrupt control register 1

2.1.3 Application example of key-on wake up

Outline: The built-in pull-up resistor is used.

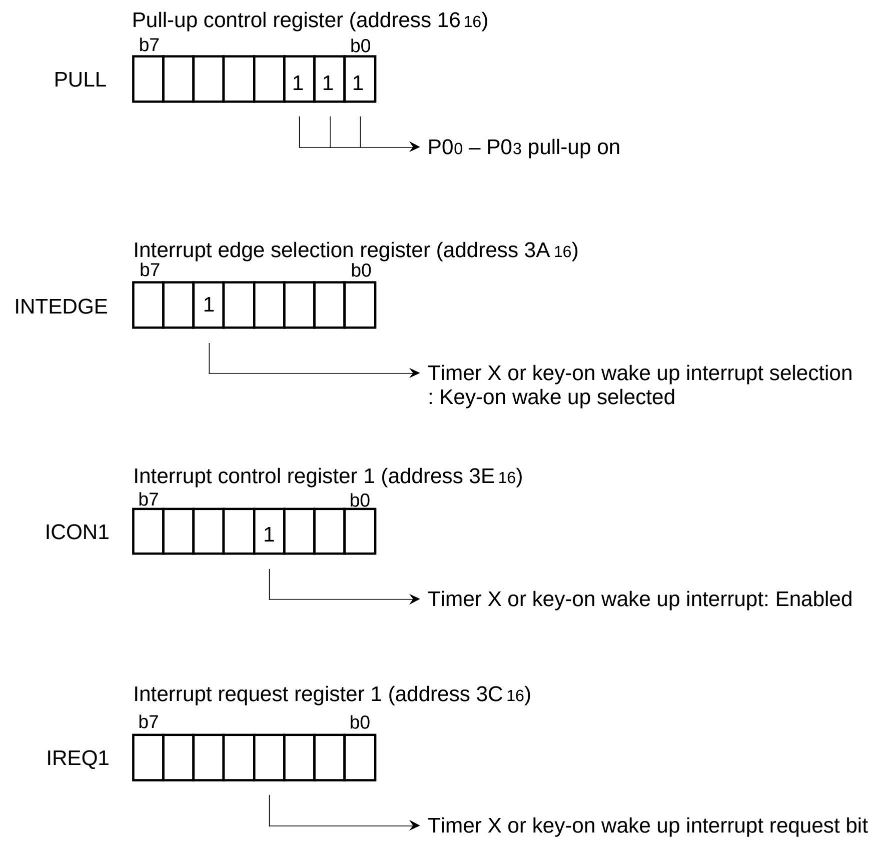


Fig. 2.1.10 Relevant registers setting

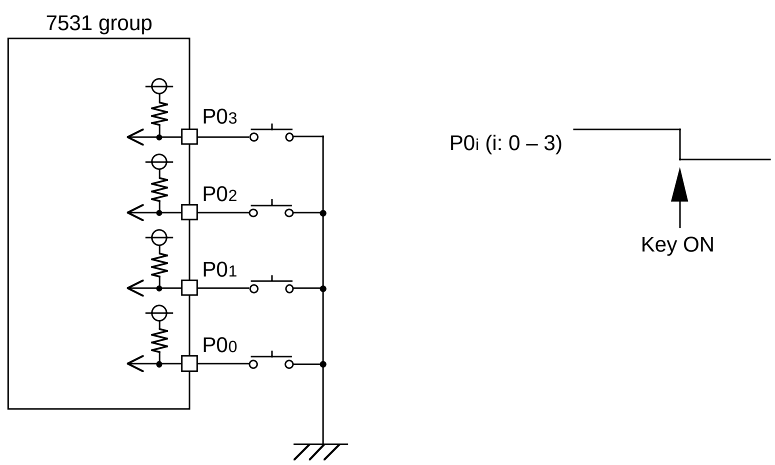


Fig. 2.1.11 Application circuit example

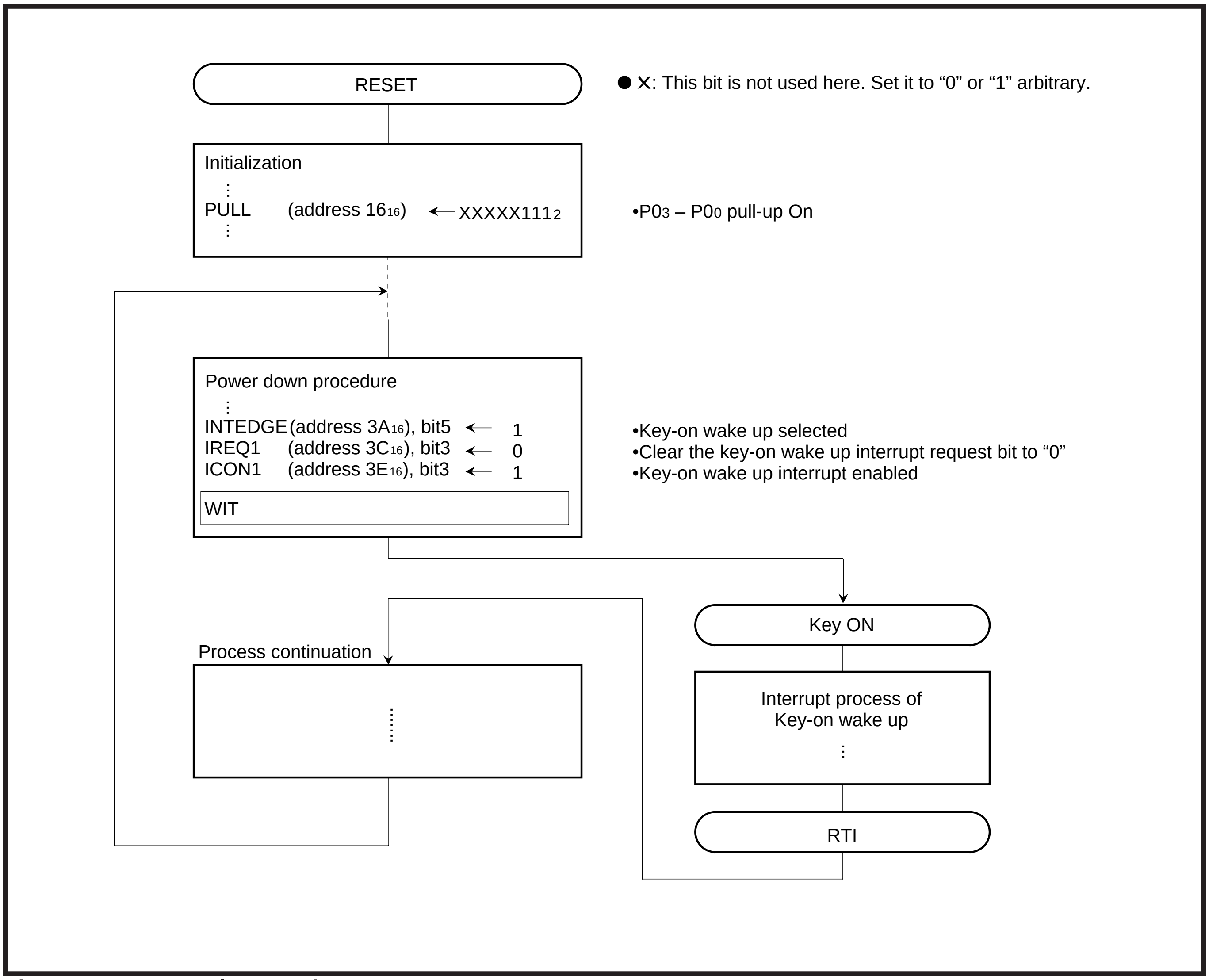


Fig. 2.1.12 Control procedure

2.1.4 Handling of unused pins

Table 2.1.1 Handling of unused pins

Pins/Ports name	Handling
P0, P1, P2, P3	•Set to the input mode and connect each to Vcc or Vss through a resistor of 1 kΩ to 10 kΩ. •Set to the output mode and open at "L" or "H" level.
V_{REF}	•Connect to Vss (GND).
X_{OUT}	•Open, only when using an external clock

2.1.5 Notes on input and output pins

(1) Notes in stand-by state

In stand-by state*[1] for low-power dissipation, do not make input levels of an input port and an I/O port "undefined".
Pull-up (connect the port to V_{CC}) or pull-down (connect the port to V_{SS}) these ports through a resistor.
When determining a resistance value, note the following points:
• External circuit
• Variation of output levels during the ordinary operation

When using a built-in pull-up or pull-down resistor, note on varied current values:
• When setting as an input port : Fix its input level
• When setting as an output port : Prevent current from flowing out to external.

● **Reason**

The output transistor becomes the OFF state, which causes the ports to be the high-impedance state. Note that the level becomes "undefined" depending on external circuits.
Accordingly, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of a input port and an I/O port are "undefined". This may cause power source current.

*[1] stand-by state : the stop mode by executing the **STP** instruction
the wait mode by executing the **WIT** instruction

(2) Modifying output data with bit managing instruction

When the port latch of an I/O port is modified with the bit managing instruction*[2], the value of the unspecified bit may be changed.

● **Reason**

The bit managing instructions are read-modify-write form instructions for reading and writing data by a byte unit. Accordingly, when these instructions are executed on a bit of the port latch of an I/O port, the following is executed to all bits of the port latch.
• As for a bit which is set for an input port :
The pin state is read in the CPU, and is written to this bit after bit managing.
• As for a bit which is set for an output port :
The bit value of the port latch is read in the CPU, and is written to this bit after bit managing.

Note the following :
• Even when a port which is set as an output port is changed for an input port, its port latch holds the output data.
• As for a bit of the port latch which is set for an input port, its value may be changed even when not specified with a bit managing instruction in case where the pin state differs from its port latch contents.

*[2] bit managing instructions : **SEB**, and **CLB** instructions

2.1.6 Termination of unused pins

(1) Terminate unused pins

① Output ports : Open

② Input ports :
Connect each pin to Vcc or Vss through each resistor of 1 kΩ to 10 kΩ.
Ports that permit the selecting of a built-in pull-up or pull-down resistor can also use this resistor. As for pins whose potential affects to operation modes such as pins CNVss, INT or others, select the Vcc pin or the Vss pin according to their operation mode.

③ I/O ports :
- Set the I/O ports for the input mode and connect them to Vcc or Vss through each resistor of 1 kΩ to 10 kΩ.
  Ports that permit the selecting of a built-in pull-up or pull-down resistor can also use this resistor.
  Set the I/O ports for the output mode and open them at “L” or “H”.
- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

(2) Termination remarks

① Input ports and I/O ports :
Do not open in the input mode.

● **Reason**
- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination ② and ③ shown on the above.

② I/O ports :
When setting for the input mode, do not connect to Vcc or Vss directly.

● **Reason**
If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between a port and Vcc (or Vss).

③ I/O ports :
When setting for the input mode, do not connect multiple ports in a lump to Vcc or Vss through a resistor.

● **Reason**
If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

- At the termination of unused pins, perform wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

2.2 Timer

This paragraph explains the registers setting method and the notes relevant to the timers.

2.2.1 Memory map

Address	Register
0028_{16}	Prescaler 12 (PRE12)
0029_{16}	Timer 1 (T1)
$002A_{16}$	Timer 2 (T2)
$002B_{16}$	Timer X mode register (TM)
$002C_{16}$	Prescaler X (PREX)
$002D_{16}$	Timer X (TX)
$002E_{16}$	Timer count source set register (TCSS)
$003A_{16}$	Interrupt edge selection register (INTEDGE)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003E_{16}$	Interrupt control register 1 (ICON1)

Fig. 2.2.1 Memory map of registers relevant to timers

2.2.2 Relevant registers

Prescaler 12, Prescaler X

b7 b6 b5 b4 b3 b2 b1 b0

Prescaler 12 (PRE12) [Address : 28_{16}]
Prescaler X (PREX) [Address : $2C_{16}$]

B	Function	At reset	R	W
0	•Set a count value of each prescaler. •The value set in this register is written to both each prescaler and the corresponding prescaler latch at the same time. •When this register is read out, the count value of the corresponding prescaler is read out.	1	○	○
1		1	○	○
2		1	○	○
3		1	○	○
4		1	○	○
5		1	○	○
6		1	○	○
7		1	○	○

Fig. 2.2.2 Structure of Prescaler 12, Prescaler X

Timer 1

b7 b6 b5 b4 b3 b2 b1 b0

Timer 1 (T1) [Address : 29$_{16}$]

B	Function	At reset	R	W
0	•Set a count value of timer 1. •The value set in this register is written to both timer 1 and timer 1 latch at the same time. •When this register is read out, the timer 1's count value is read out.	1	○	○
1		0	○	○
2		0	○	○
3		0	○	○
4		0	○	○
5		0	○	○
6		0	○	○
7		0	○	○

Fig. 2.2.3 Structure of Timer 1

Timer 2

b7 b6 b5 b4 b3 b2 b1 b0

Timer 2 (T2) [Address : 2A$_{16}$]

B	Function	At reset	R	W
0	•Set a count value of timer 2. •The value set in this register is written to both timer 2 and timer 2 latch at the same time. •When this register is read out, the timer 2's count value is read out.	0	○	○
1		0	○	○
2		0	○	○
3		0	○	○
4		0	○	○
5		0	○	○
6		0	○	○
7		0	○	○

Fig. 2.2.4 Structure of Timer 2

Timer X

b7 b6 b5 b4 b3 b2 b1 b0

Timer X (TX) [Address : $2D_{16}$]

B	Function	At reset	R	W
0	•Set a count value of timer X. •The value set in this register is written to both timer X and timer X latch at the same time. •When this register is read out, the timer X's count value is read out.	1	○	○
1		1	○	○
2		1	○	○
3		1	○	○
4		1	○	○
5		1	○	○
6		1	○	○
7		1	○	○

Fig. 2.2.5 Structure of Timer X

Timer X mode register

b7 b6 b5 b4 b3 b2 b1 b0

Timer X mode register (TM) [Address : $2B_{16}$]

B	Name	Function	At reset	R	W
0	Timer X operating mode bits	b1 b0 0 0 : Timer mode 0 1 : Pulse output mode 1 0 : Event counter mode 1 1 : Pulse width measurement mode	0	○	○
1			0	○	○
2	$CNTR_0$ active edge switch bit	The function depends on the operating mode. (Refer to Table 2.2.1)	0	○	○
3	Timer X count stop bit	0 : Count start 1 : Count stop	0	○	○
4	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".		0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 2.2.6 Structure of Timer X mode register

Table 2.2.1 $CNTR_0$ active edge switch bit function

Timer X operation modes		$CNTR_0$ active edge switch bit (bit 2 of address $2B_{16}$) contents
Timer mode	"0"	$CNTR_0$ interrupt request occurrence: Falling edge ; No influence to timer count
	"1"	$CNTR_0$ interrupt request occurrence: Rising edge ; No influence to timer count
Pulse output mode	"0"	Pulse output start: Beginning at "H" level $CNTR_0$ interrupt request occurrence: Falling edge
	"1"	Pulse output start: Beginning at "L" level $CNTR_0$ interrupt request occurrence: Rising edge
Event counter mode	"0"	Timer X: Rising edge count $CNTR_0$ interrupt request occurrence: Falling edge
	"1"	Timer X: Falling edge count $CNTR_0$ interrupt request occurrence: Rising edge
Pulse width measurement mode	"0"	Timer X: "H" level width measurement $CNTR_0$ interrupt request occurrence: Falling edge
	"1"	Timer X: "L" level width measurement $CNTR_0$ interrupt request occurrence: Rising edge

Timer count source set register

b7 b6 b5 b4 b3 b2 b1 b0

Timer count source set register (TCSS) [Address : 2E 16]

B	Name	Function	At reset	R	W
0	Timer X count source selection bit (Note)	0 : f(XIN) / 16 1 : f(XIN) / 2	0	○	○
1	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".		0	○	×
2			0	○	×
3			0	○	×
4			0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Note: To switch the timer X count source selection bit, stop the timer X count operation before do that.

Fig. 2.2.7 Structure of Timer count source set register

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt edge selection register (INTEDGE) [Address : 3A 16]

B	Name	Function	At reset	R	W
0	INT0 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
1	INT1 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
2	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".		0	○	×
3			0	○	×
4	Serial I/O1 or INT1 interrupt selection bit (**Note**)	0 : Serial I/O1 1 : INT1	0	○	○
5	Timer X or key-on wake up interrupt selection bit	0 : Timer X 1 : Key-on wake up	0	○	○
6	Timer 2 or serial I/O2 interrupt selection bit	0 : Timer 2 1 : Serial I/O2	0	○	○
7	CNTR0 or AD converter interrupt selection bit	0 : CNTR0 1 : AD converter	0	○	○

Note: Do not write "1" to bit 4 in the 32-pin package versions.

Fig. 2.2.8 Structure of Interrupt edge selection register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address : $3C_{16}$]

B	Name	Function	At reset	R	W
0	Serial I/O1 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
1	Serial I/O1 transmit or INT_1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
2	INT_0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
3	Timer X or key-on wake up interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
4	Timer 1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
5	Timer 2 or serial I/O2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
6	$CNTR_0$ or AD converter interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0".		0	○	×

✻: These bits can be cleared to "0" by program, but cannot be set to "1".

Fig. 2.2.9 Structure of Interrupt request register 1

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address : $3E_{16}$]

B	Name	Function	At reset	R	W
0	Serial I/O1 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Serial I/O1 transmit or INT_1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	INT_0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Timer X or key-on wake up interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Timer 2 or serial I/O2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	$CNTR_0$ or AD converter interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Nothing is allocated for this bit. Do not write "1" to this bit. When this bit is read out, the value is "0".		0	○	×

Fig. 2.2.10 Structure of Interrupt control register 1

2.2.3 Timer application examples

(1) Basic functions and uses

[Function 1] Control of Event interval (Timer X, Timer 1, Timer 2)

When a certain time, by setting a count value to each timer, has passed, the timer interrupt request occurs.

<Use>

- •Generation of an output signal timing
- •Generation of a wait time

[Function 2] Control of Cyclic operation (Timer X, Timer 1, Timer 2)

The value of the timer latch is automatically written to the corresponding timer each time the timer underflows, and each timer interrupt request occurs in cycles.

<Use>

- •Generation of cyclic interrupts
- •Clock function (measurement of 250 ms); see Application example 1
- •Control of a main routine cycle

[Function 3] Output of Rectangular waveform (Timer X)

The output level of the $CNTR_0$ pin is inverted each time the timer underflows (in the pulse output mode).

<Use>

- •Piezoelectric buzzer output; see Application example 2
- •Generation of the remote-control carrier waveforms

[Function 4] Count of External pulses (Timer X)

External pulses input to the $CNTR_0$ pin are counted as the timer count source (in the event counter mode).

<Use>

- •Frequency measurement; see Application example 3
- •Division of external pulses
- •Generation of interrupts due to a cycle using external pulses as the count source; count of a reel pulse

[Function 5] Measurement of External pulse width (Timer X)

The “H” or “L” level width of external pulses input to $CNTR_0$ pin is measured (in the pulse width measurement mode).

<Use>

- •Measurement of external pulse frequency (measurement of pulse width of FG pulse* for a motor); see Application example 4
- •Measurement of external pulse duty (when the frequency is fixed)

FG pulse*: Pulse used for detecting the motor speed to control the motor speed.

(2) Timer application example 1: Clock function (measurement of 250 ms)

Outline: The input clock is divided by the timer so that the clock can count up at 250 ms intervals.

Specifications: •The clock $f(X_{IN})$ = 4.19 MHz (2^{22} Hz) is divided by the timer.
•The clock is counted up in the process routine of the timer X interrupt which occurs at 250 ms intervals.

Figure 2.2.11 shows the timers connection and setting of division ratios; Figure 2.2.12 shows the relevant registers setting; Figure 2.2.13 shows the control procedure.

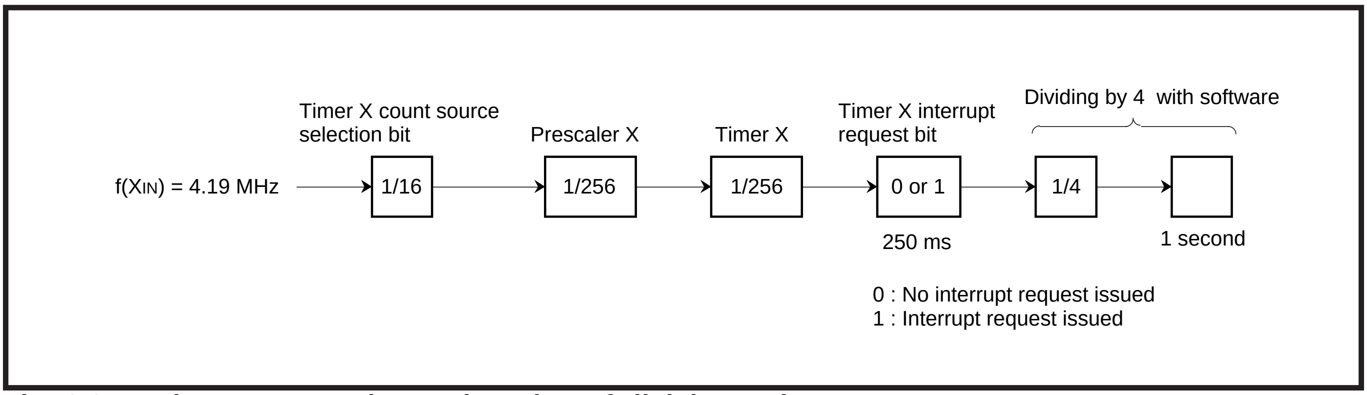


Fig. 2.2.11 Timers connection and setting of division ratios

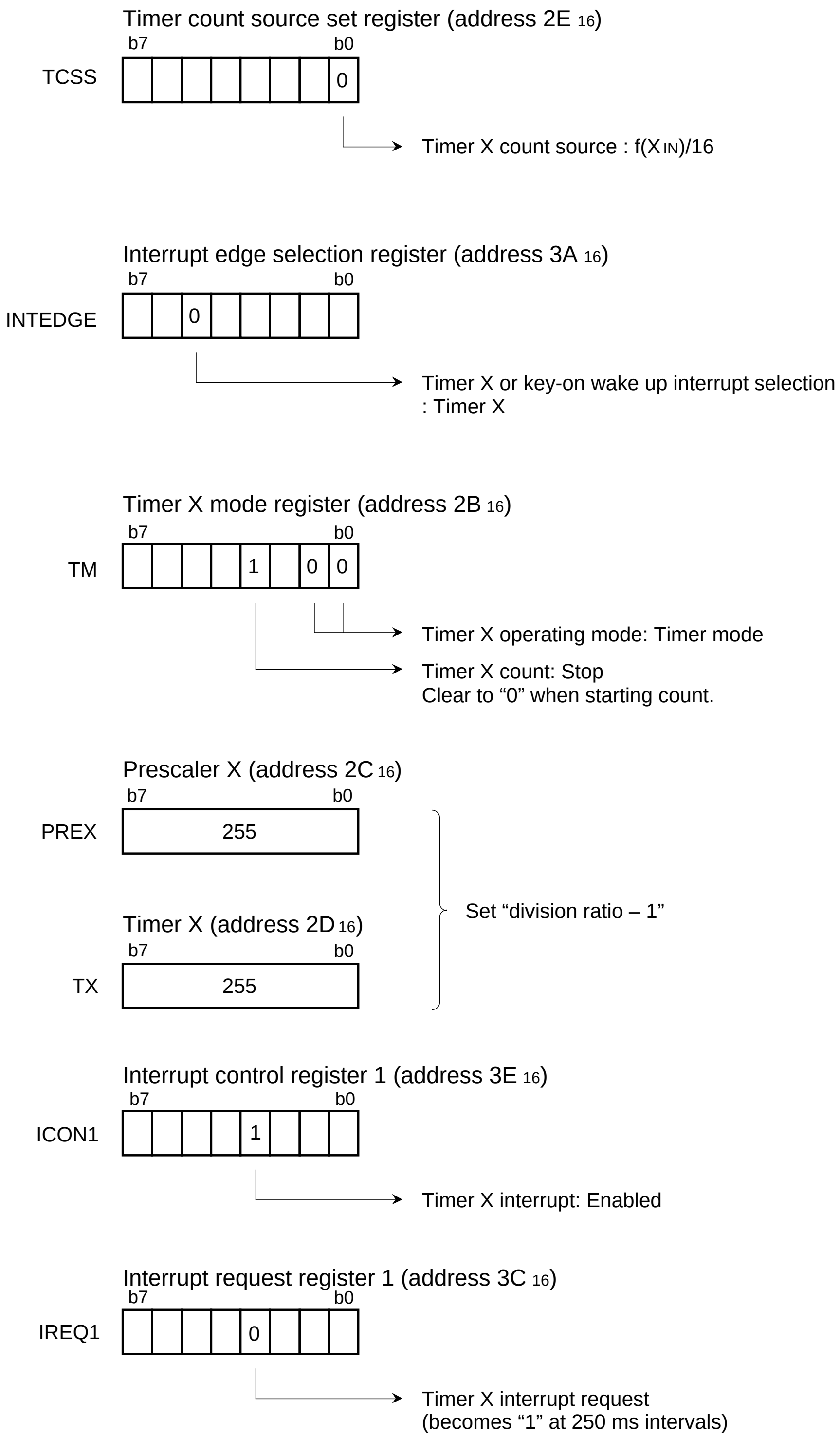


Fig. 2.2.12 Relevant registers setting

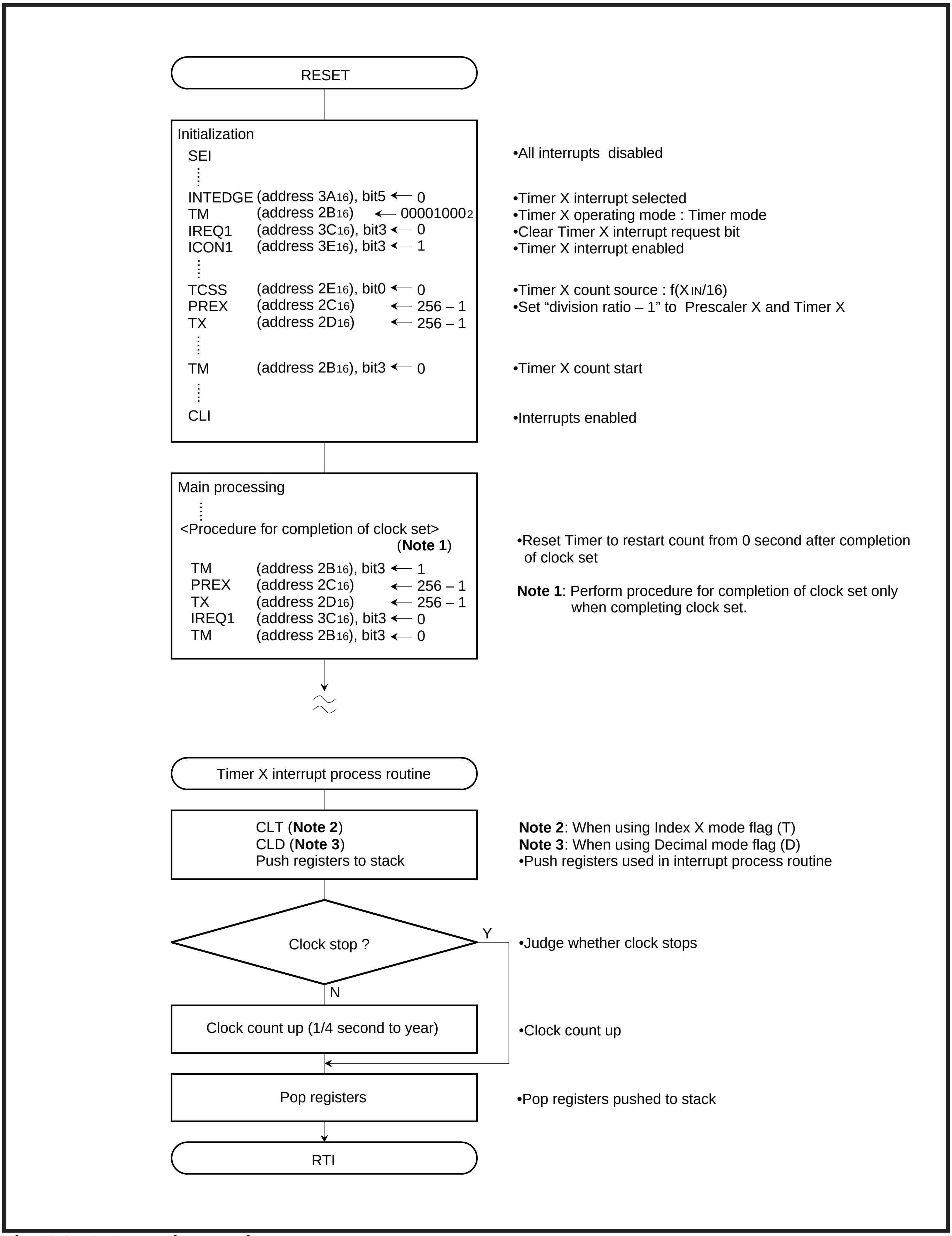


Fig. 2.2.13 Control procedure

(3) Timer application example 2: Piezoelectric buzzer output

Outline: The rectangular waveform output function of the timer is applied for a piezoelectric buzzer output.

Specifications: •The rectangular waveform, dividing the clock f(X_{IN}) = 4.19 MHz (2^{22} Hz) into about 2 kHz (2048 Hz), is output from the $P1_4$/$CNTR_0$ pin.
•The level of the $P1_4$/$CNTR_0$ pin is fixed to “H” while a piezoelectric buzzer output stops.

Figure 2.2.14 shows a peripheral circuit example, and Figure 2.2.15 shows the timers connection and setting of division ratios. Figures 2.2.16 shows the relevant registers setting, and Figure 2.2.17 shows the control procedure.

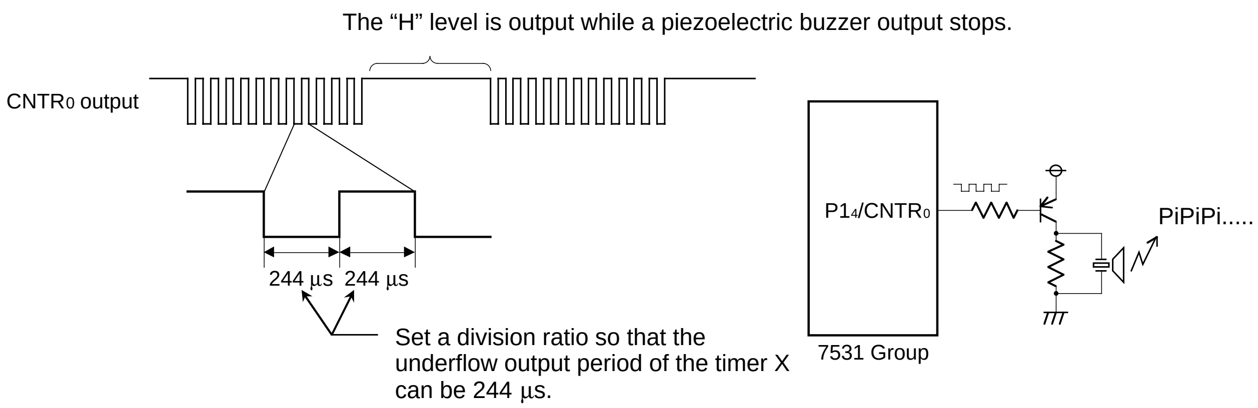


Fig. 2.2.14 Peripheral circuit example

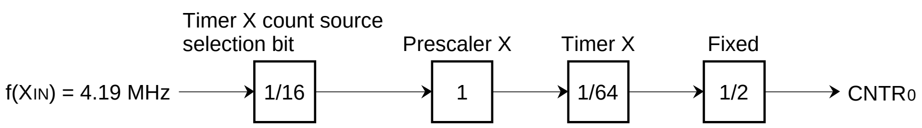


Fig. 2.2.15 Timers connection and setting of division ratios

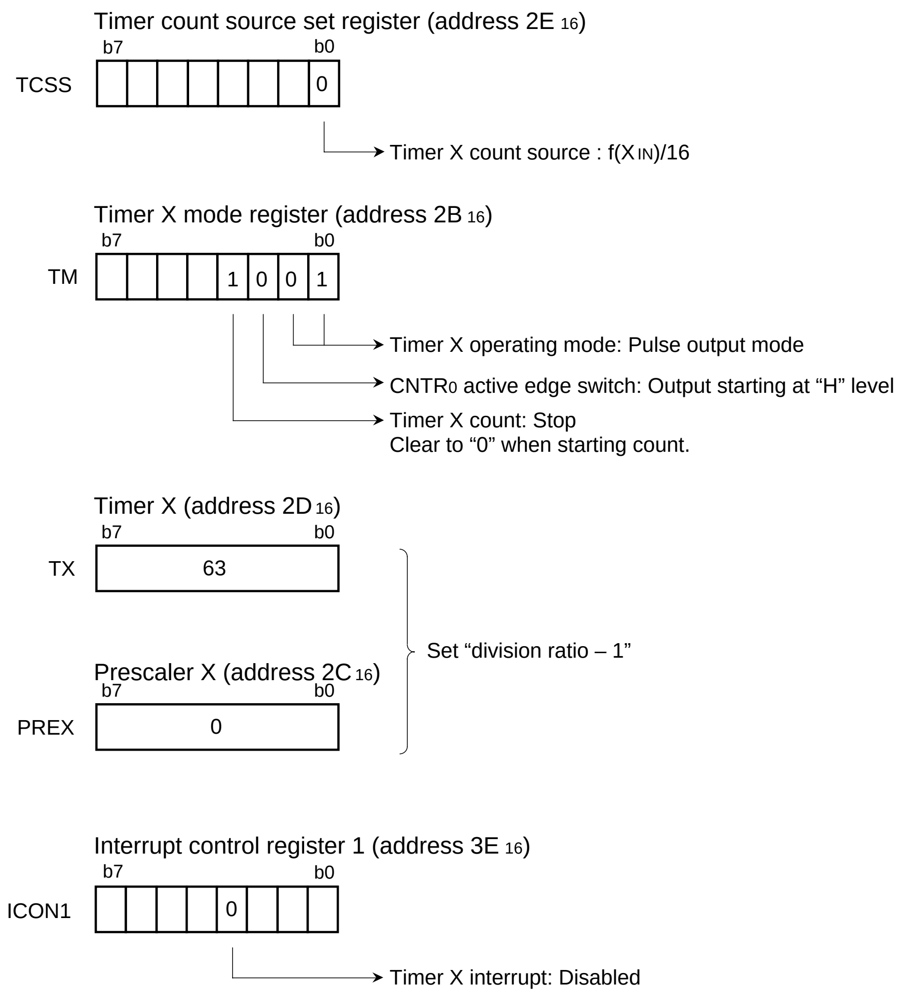


Fig. 2.2.16 Relevant registers setting

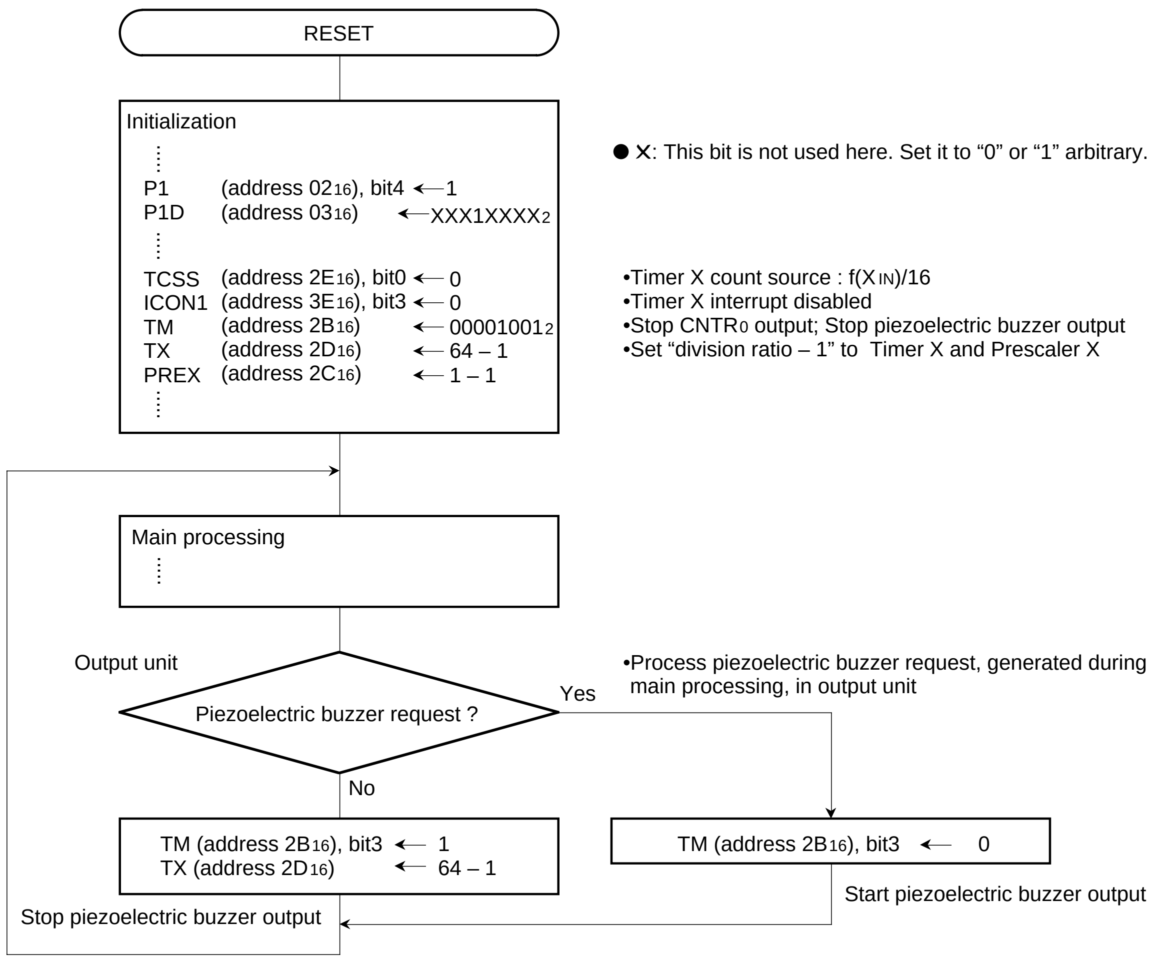


Fig. 2.2.17 Control procedure

(4) Timer application example 3: Frequency measurement

Outline: The following two values are compared to judge whether the frequency is within a valid range.

•A value by counting pulses input to $P1_4/CNTR_0$ pin with the timer.

•A reference value

Specifications: •The pulse is input to the $P1_4/CNTR_0$ pin and counted by the timer X.

•A count value is read out at about 2 ms intervals, the timer 1 interrupt interval. When the count value is 28 to 40, it is judged that the input pulse is valid.

•Because the timer is a down-counter, the count value is compared with 227 to 215 (Note).

Note: 227 to 215 = {255 (initial value of counter) – 28} to {255 – 40}; 28 to 40 means the number of valid value.

Figure 2.2.18 shows the judgment method of valid/invalid of input pulses; Figure 2.2.19 shows the relevant registers setting; Figure 2.2.20 shows the control procedure.

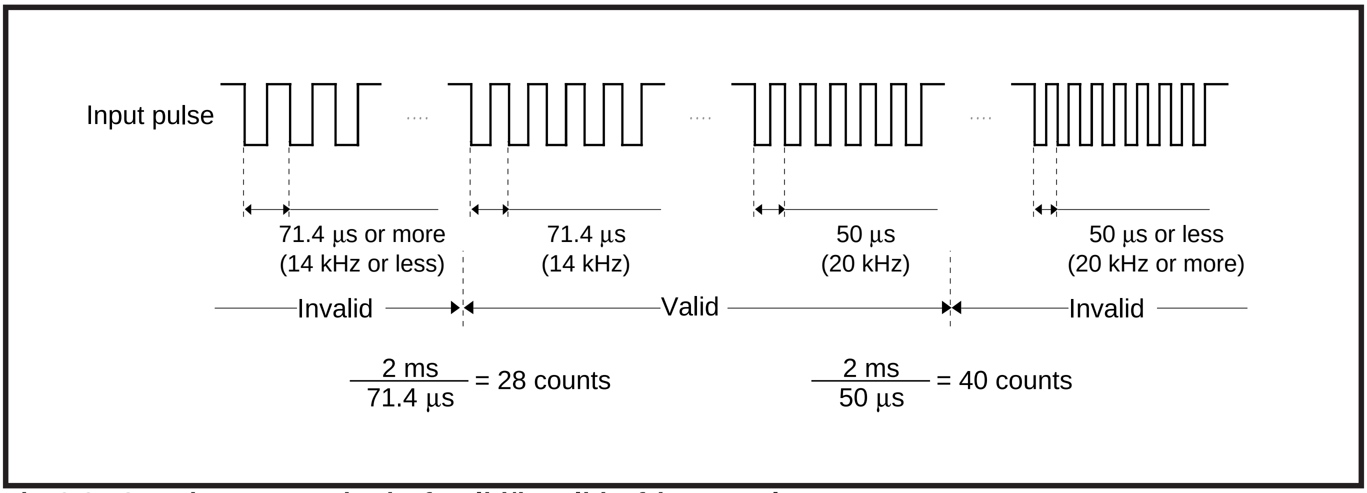


Fig 2.2.18 Judgment method of valid/invalid of input pulses

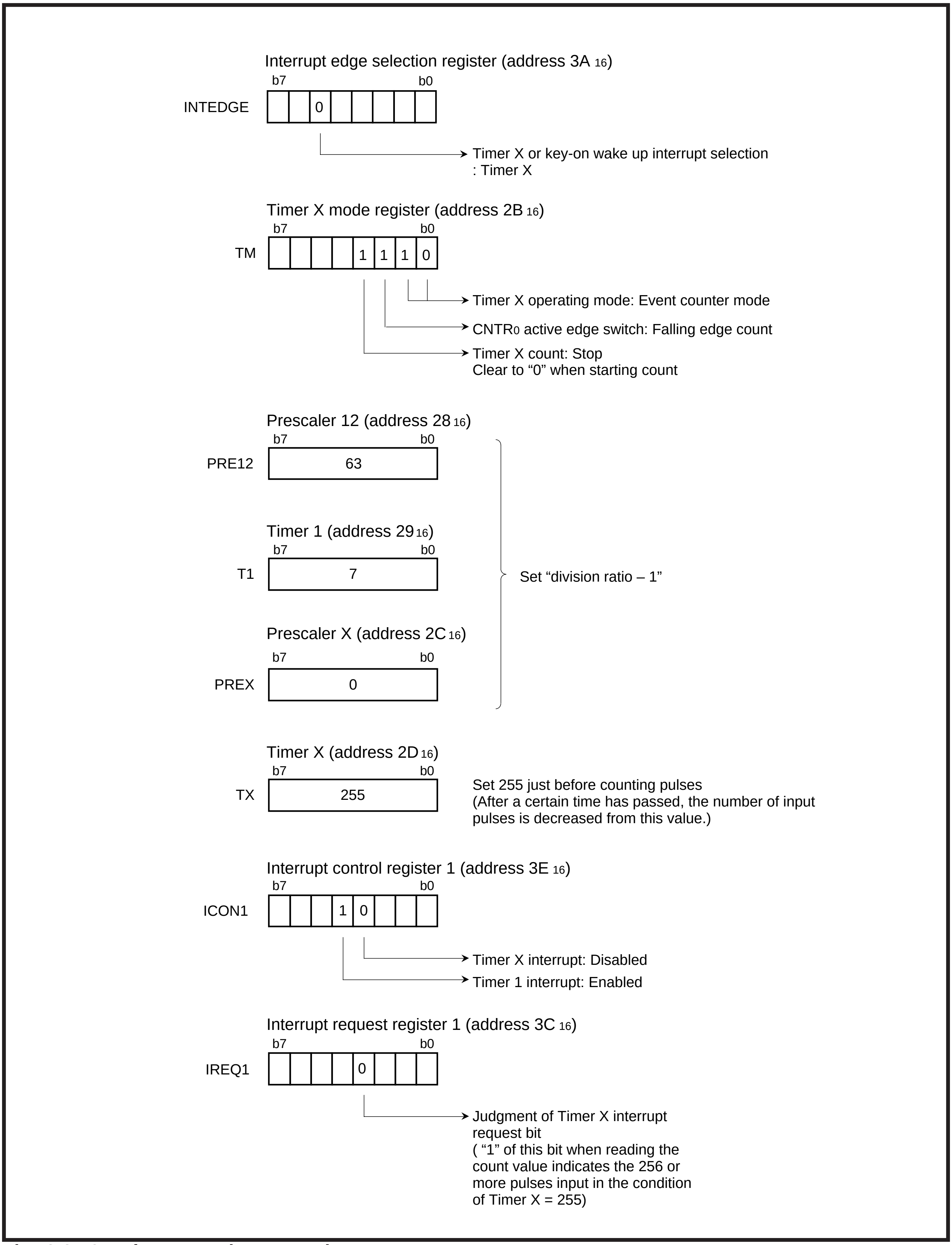


Fig. 2.2.19 Relevant registers setting

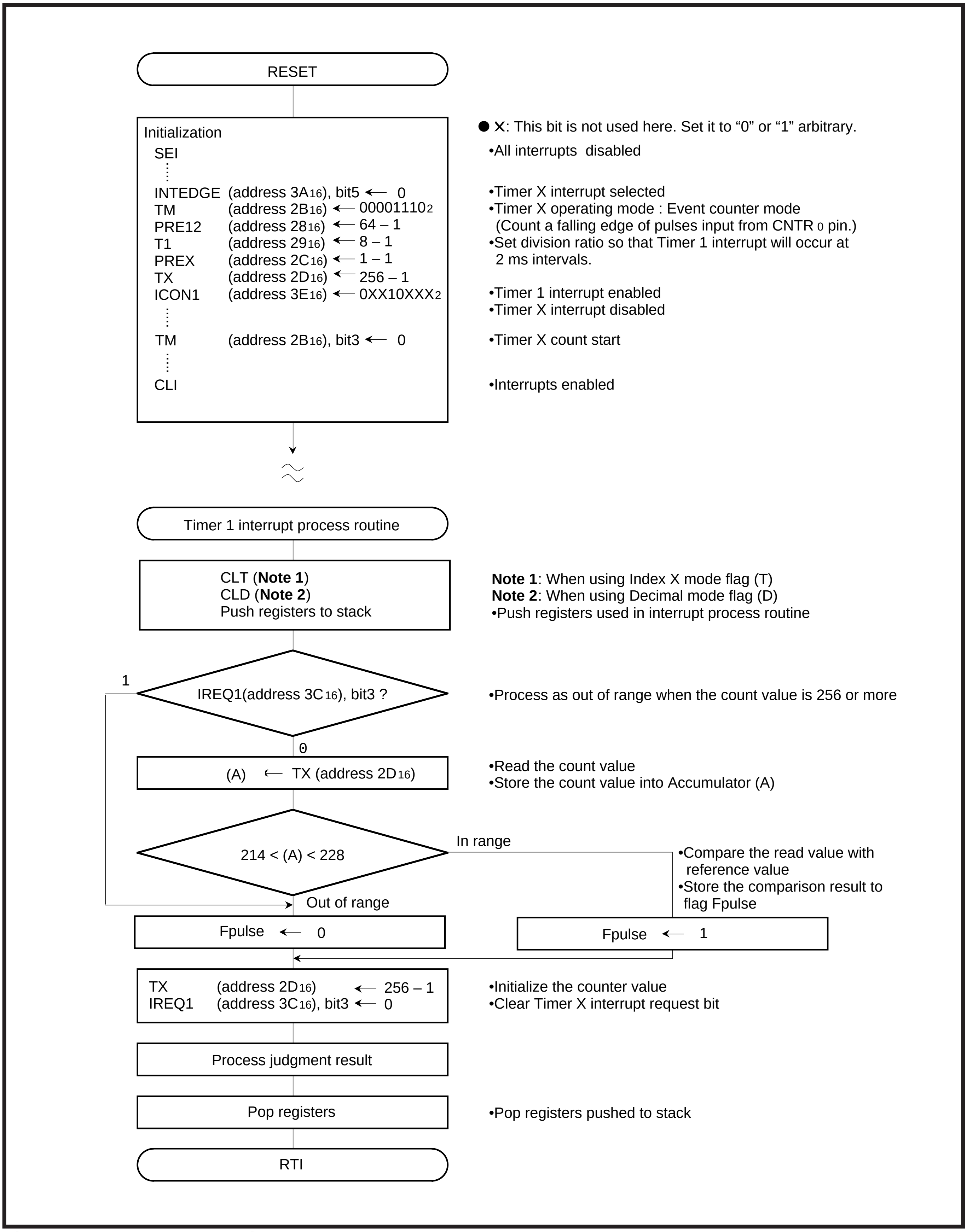


Fig. 2.2.20 Control procedure

(5) Timer application example 4: Measurement of FG pulse width for motor

Outline: The timer X counts the “H” level width of the pulses input to the $P1_4/CNTR_0$ pin. An underflow is detected by the timer X interrupt and an end of the input pulse “H” level is detected by the $CNTR_0$ interrupt.

Specifications: •The timer X counts the “H” level width of the FG pulse input to the $P1_4/CNTR_0$ pin.

<Example>

When the clock frequency is 4.19 MHz, the count source is 3.8 µs, which is obtained by dividing the clock frequency by 16. Measurement can be made up to 250 ms in the range of $FFFF_{16}$ to 0000_{16}.

Figure 2.2.21 shows the timers connection and setting of division ratio; Figure 2.2.22 shows the relevant registers setting; Figure 2.2.23 shows the control procedure.

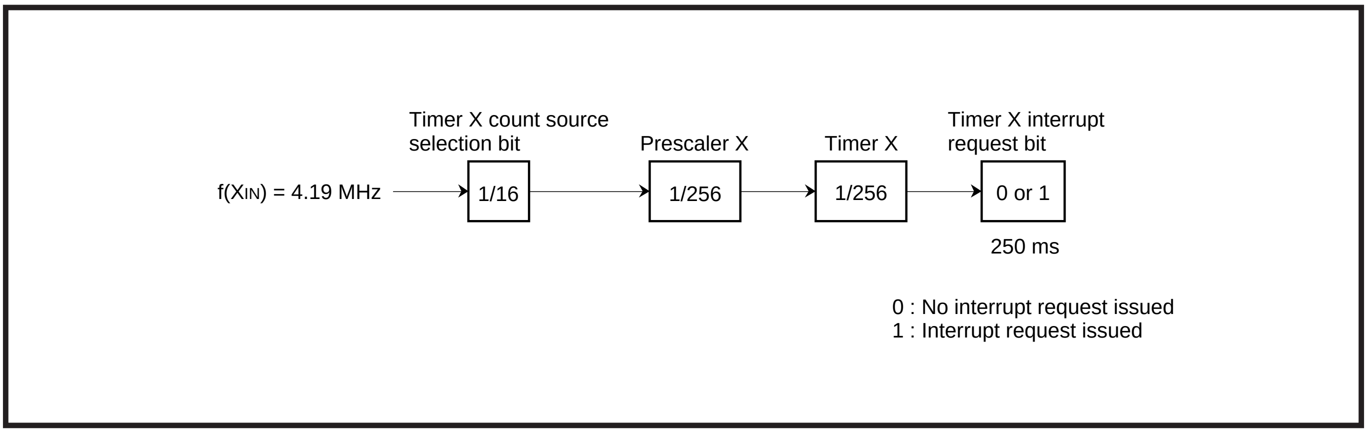


Fig. 2.2.21 Timers connection and setting of division ratios

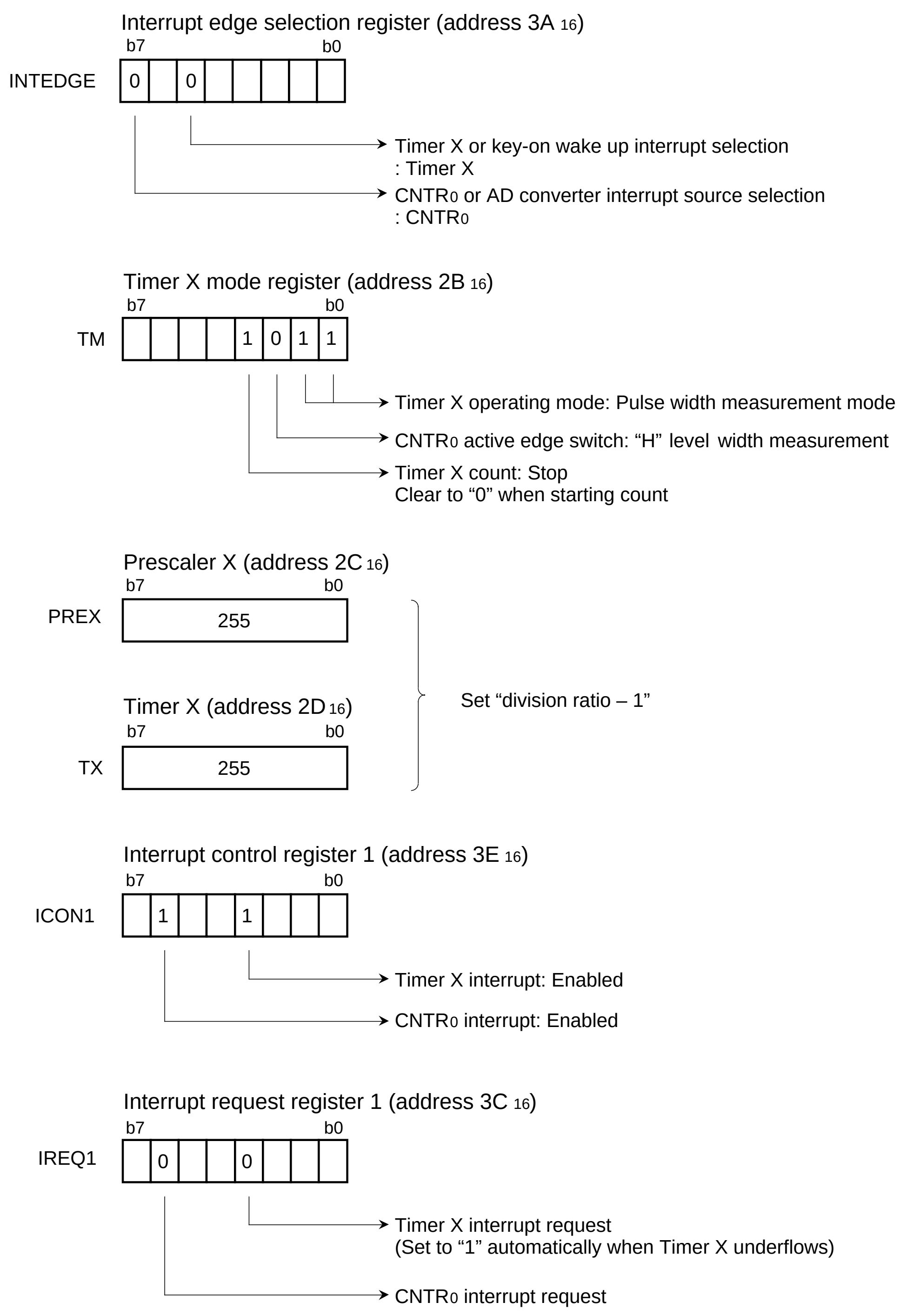


Fig. 2.2.22 Relevant registers setting

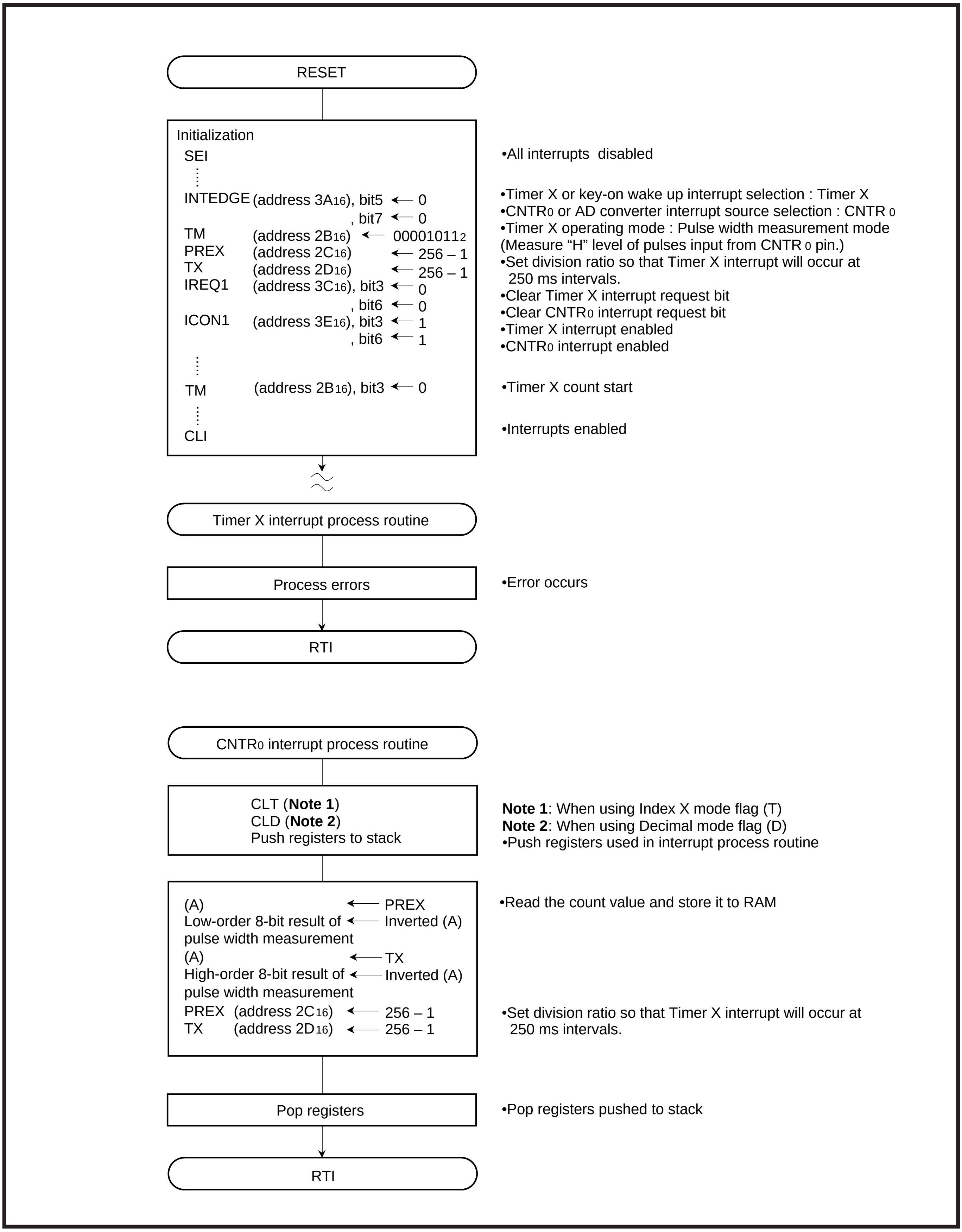


Fig. 2.2.23 Control procedure

2.3 Serial I/O

This paragraph explains the registers setting method and the notes relevant to the serial I/O.

2.3.1 Memory map

Address	Register
0018_{16}	Transmit/Receive buffer register (TB/RB)
0019_{16}	Serial I/O1 status register (SIO1STS)
$001A_{16}$	Serial I/O1 control register (SIO1CON)
$001B_{16}$	UART control register (UARTCON)
$001C_{16}$	Baud rate generator (BRG)
0030_{16}	Serial I/O2 control register (SIO2CON)
0031_{16}	Serial I/O2 register (SIO2)
$003A_{16}$	Interrupt edge selection register (INTEDGE)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003E_{16}$	Interrupt control register 1 (ICON1)

Fig. 2.3.1 Memory map of registers relevant to serial I/O

2.3.2 Relevant registers

Transmit/Receive buffer register

b7 b6 b5 b4 b3 b2 b1 b0

Transmit/Receive buffer register (TB/RB) [Address : 18_{16}]

B	Function	At reset	R	W
0	The transmission data is written to or the receive data is read out from this buffer register. • At writing: A data is written to the transmit buffer register. • At reading: The contents of the receive buffer register are read out.	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5		?	○	○
6		?	○	○
7		?	○	○

Note: The contents of transmit buffer register cannot be read out.
The data cannot be written to the receive buffer register.

Fig. 2.3.2 Structure of Transmit/Receive buffer register

Serial I/O1 status register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O1 status register (SIO1STS) [Address : 19 16]

B	Name	Function	At reset	R	W
0	Transmit buffer empty flag (TBE)	0 : Buffer full 1 : Buffer empty	1	○	×
1	Receive buffer full flag (RBF)	0 : Buffer empty 1 : Buffer full	0	○	×
2	Transmit shift register shift completion flag (TSC)	0 : Transmit shift in progress 1 : Transmit shift completed	0	○	×
3	Overrun error flag (OE)	0 : No error 1 : Overrun error	0	○	×
4	Parity error flag (PE)	0 : No error 1 : Parity error	0	○	×
5	Framing error flag (FE)	0 : No error 1 : Framing error	0	○	×
6	Summing error flag (SE)	0 : (OE) $\cup$ (PE) $\cup$ (FE) = 0 1 : (OE) $\cup$ (PE) $\cup$ (FE) = 1	0	○	×
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "1".		1	○	×

Fig. 2.3.3 Structure of Serial I/O1 status register

Serial I/O1 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O1 control register (SIO1CON) [Address : 1A 16]

B	Name	Function	At reset	R	W
0	BRG count source selection bit (CSS)	0 : f(XIN) 1 : f(XIN)/4	0	○	○
1	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "1".		1	○	×
2	Continuous transmit valid bit	0 : Continuous transmit invalid 1 : Continuous transmit valid	0	○	○
3	Transmit interrupt source selection bit (TIC)	0 : Interrupt when transmit buffer has emptied 1 : Interrupt when transmit shift operation is completed	0	○	○
4	Transmit enable bit (TE)	0 : Transmit disabled 1 : Transmit enabled	0	○	○
5	Receive enable bit (RE)	0 : Receive disabled 1 : Receive enabled	0	○	○
6	Serial I/O1 enable bit (SIOE)	b7 b6 0 0 : Serial I/O1 disabled 0 1 : Not available 1 0 : Serial I/O1 enabled 1 1 : Serial I/O1 cleared	0	○	○
7			0	○	○

Fig. 2.3.4 Structure of Serial I/O1 control register

UART control register

b7 b6 b5 b4 b3 b2 b1 b0

UART control register (UARTCON) [Address : $1B_{16}$]

B	Name	Function	At reset	R	W
0	Character length selection bit (CHAS)	0 : 8 bits 1 : 7 bits	0	○	○
1	Parity enable bit (PARE)	0 : Parity checking disabled 1 : Parity checking enabled	0	○	○
2	Parity selection bit (PARS)	0 : Even parity 1 : Odd parity	0	○	○
3	Stop bit length selection bit (STPS)	0 : 1 stop bit 1 : 2 stop bits	0	○	○
4	$P1_1$/TxD P-channel output disable bit (POFF)	In output mode 0 : CMOS output 1 : N-channel open-drain output	0	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are “1”.		1	○	×
6			1	○	×
7			1	○	×

Fig. 2.3.5 Structure of UART control register

Baud rate generator

b7 b6 b5 b4 b3 b2 b1 b0

Baud rate generator (BRG) [Address : $1C_{16}$]

B	Function	At reset	R	W
0	Set a count value of baud rate generator.	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5		?	○	○
6		?	○	○
7		?	○	○

Fig. 2.3.6 Structure of Baud rate generator

Serial I/O2 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O2 control register (SIO2CON) [Address : 30 16]

B	Name	Function	At reset	R	W
0	Internal synchronous clock selection bits	b2 b1 b0 0 0 0 : f(XIN)/8 0 0 1 : f(XIN)/16 0 1 0 : f(XIN)/32 0 1 1 : f(XIN)/64 1 1 0 : f(XIN)/128 1 1 1 : f(XIN)/256	0	○	○
1			0	○	○
2			0	○	○
3	SDATA pin selection bit (**Note**)	0 : I/O port / SDATA input 1 : SDATA output	0	○	○
4	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0".		0	○	×
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○
6	SCLK pin selection bit	0 : External clock (SCLK is input) 1 : Internal clock (SCLK is output)	0	○	○
7	Transmit / receive shift completion flag	0 : shift in progress 1 : shift completed	0	○	×

Note: When using it as a SDATA input, set the port P13 direction register bit to "0".

Fig. 2.3.7 Structure of Serial I/O2 control register

Serial I/O2 register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O2 register (SIO2) [Address : 31 16]

B	Function	At reset	R	W
0	A shift register for serial transmission and reception. • At transmitting : Set a transmission data. • At receiving : A reception data is stored.	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5		?	○	○
6		?	○	○
7		?	○	○

Fig. 2.3.8 Structure of Serial I/O2 register

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt edge selection register (INTEDGE) [Address : $3A_{16}$]

B	Name	Function	At reset	R	W
0	INT_0 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
1	INT_1 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
2	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".		0	○	×
3			0	○	×
4	Serial I/O1 or INT_1 interrupt selection bit (**Note**)	0 : Serial I/O1 1 : INT_1	0	○	○
5	Timer X or key-on wake up interrupt selection bit	0 : Timer X 1 : Key-on wake up	0	○	○
6	Timer 2 or serial I/O2 interrupt selection bit	0 : Timer 2 1 : Serial I/O2	0	○	○
7	$CNTR_0$ or AD converter interrupt selection bit	0 : $CNTR_0$ 1 : AD converter	0	○	○

Note: Do not write "1" to bit 4 in the 32-pin package versions.

Fig. 2.3.9 Structure of Interrupt edge selection register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address : $3C_{16}$]

B	Name	Function	At reset	R	W
0	Serial I/O1 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
1	Serial I/O1 transmit or INT_1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
2	INT_0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
3	Timer X or key-on wake up interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
4	Timer 1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
5	Timer 2 or serial I/O2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
6	$CNTR_0$ or AD converter interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0".		0	○	×

✻: These bits can be cleared to "0" by program, but cannot be set to "1".

Fig. 2.3.10 Structure of Interrupt request register 1

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address : $3E_{16}$]

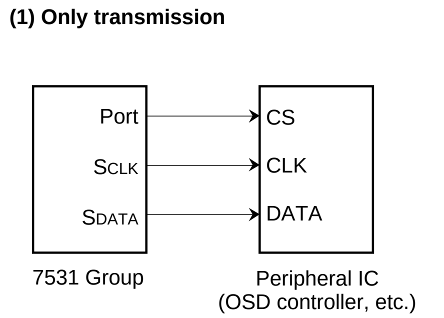
B	Name	Function	At reset	R	W
0	Serial I/O1 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Serial I/O1 transmit or INT_1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	INT_0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Timer X or key-on wake up interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Timer 2 or serial I/O2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	$CNTR_0$ or AD converter interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Nothing is allocated for this bit. Do not write “1” to this bit. When this bit is read out, the value is “0”.		0	○	×

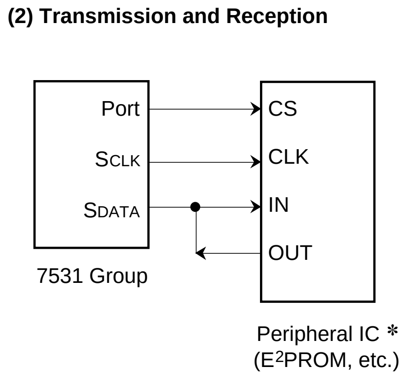
Fig. 2.3.11 Structure of Interrupt control register 1

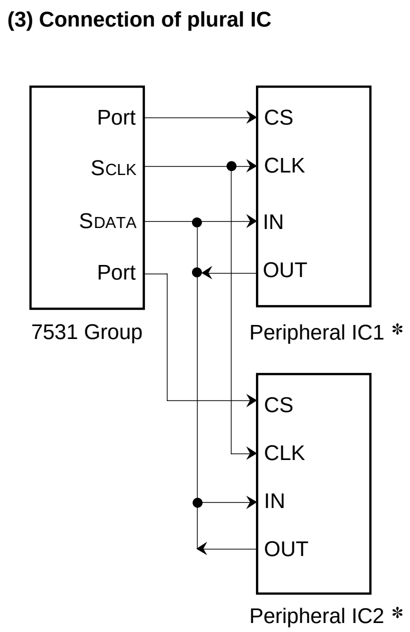
2.3.3 Serial I/O connection examples

(1) Control of peripheral IC equipped with CS pin

Figure 2.3.12 shows connection examples with a peripheral IC equipped with the CS pin. Each case uses the clock synchronous serial I/O mode.







✻ : Use the peripheral IC of which OUT pin has an N-channel open-drain output structure and which enters a high-impedance state while receiving data.

Note: “Port” means an output port controlled by software.

Fig. 2.3.12 Serial I/O connection examples (1)

(2) Connection with microcomputer

Figure 2.3.13 shows connection examples with another microcomputer.

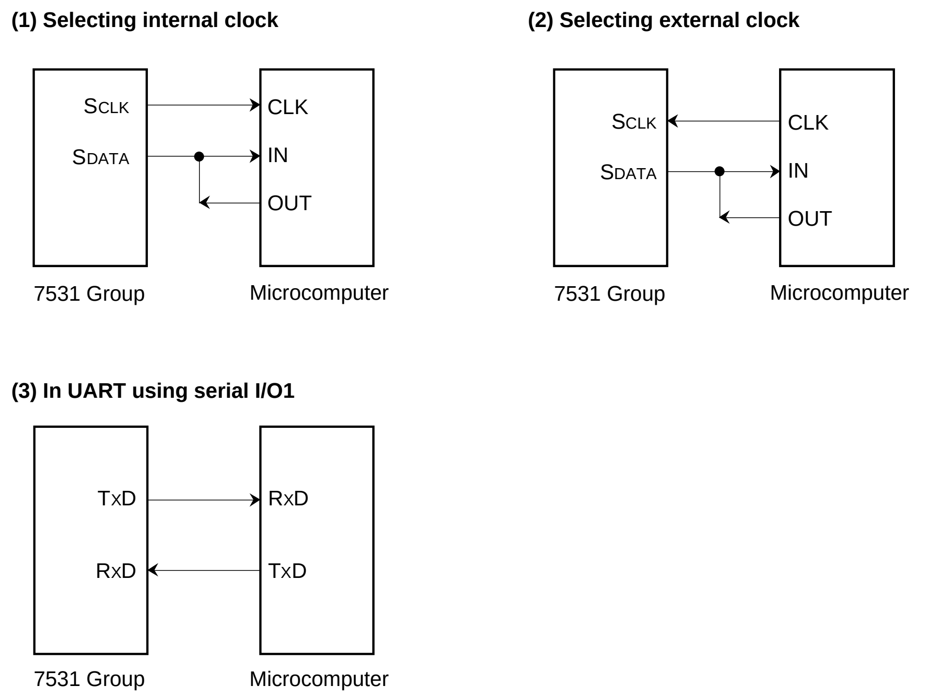


Fig. 2.3.13 Serial I/O connection examples (2)

2.3.4 Serial I/O transfer data format

The clock synchronous or the clock asynchronous (UART) can be selected as the serial I/O. Figure 2.3.14 shows the serial I/O transfer data format.

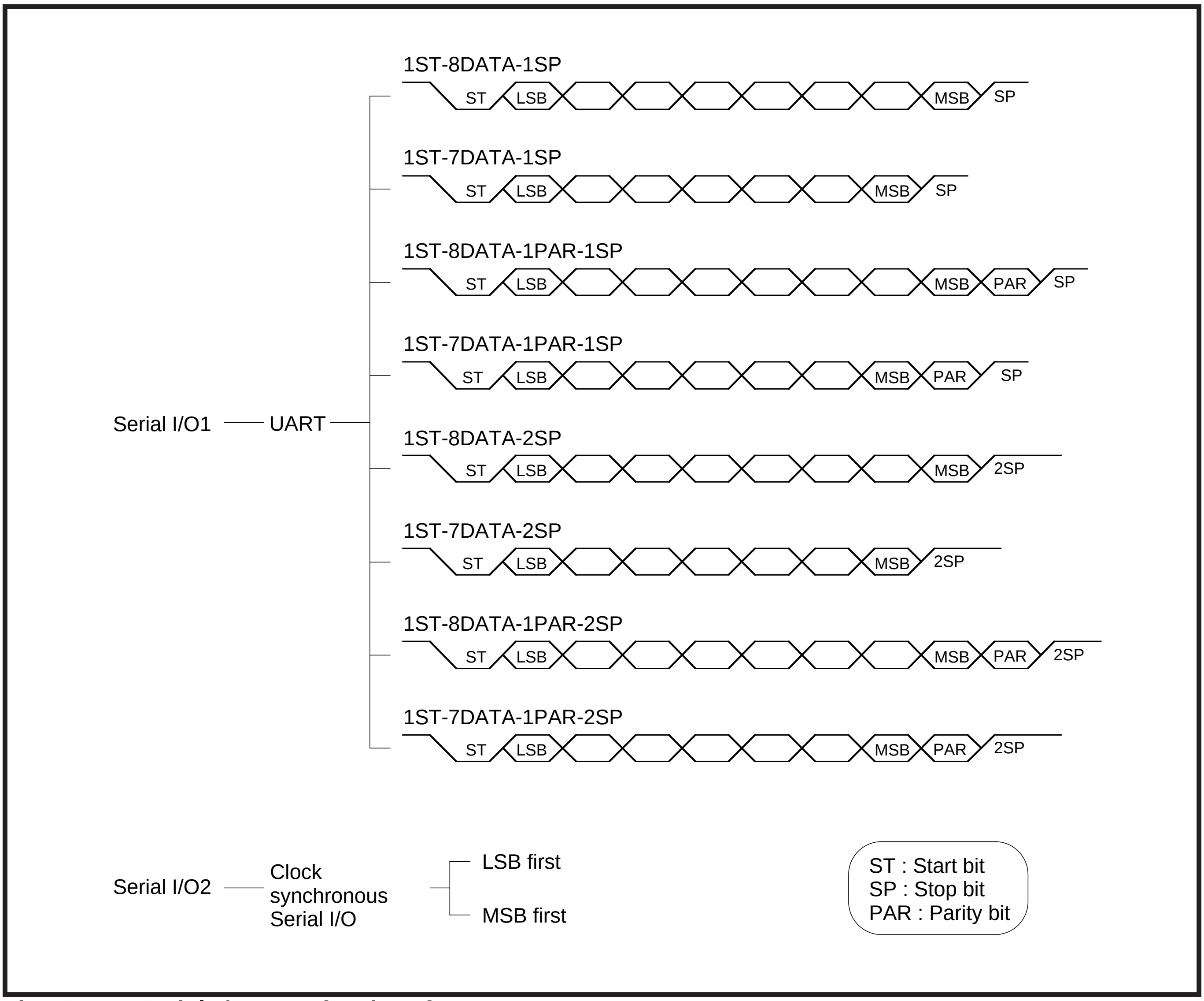


Fig. 2.3.14 Serial I/O transfer data format

2.3.5 Serial I/O application examples

(1) Communication using clock synchronous serial I/O (transmit/receive)

Outline : 2-byte data is transmitted and received, using the clock synchronous serial I/O. Port $P0_0$ is used for communication control and outputs the quasi-$\overline{S_{RDY}}$ signal.

The following explain an example using the serial I/O2. Figure 2.3.15 shows a connection diagram, and Figure 2.3.16 shows a timing chart.

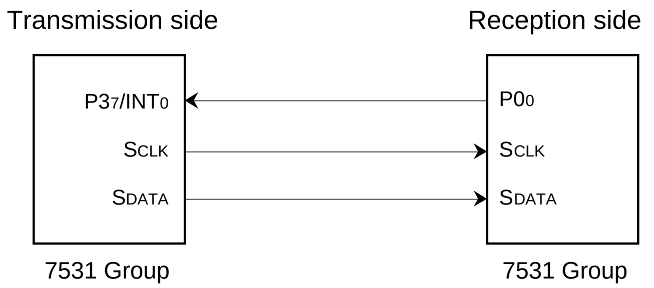


Fig. 2.3.15 Connection diagram

Specifications :
- The Serial I/O2, clock synchronous serial I/O, is used.
- Synchronous clock frequency : 125 kHz; $f(X_{IN})$ = 8 MHz divided by 64
- Transfer direction : LSB first
- The reception side outputs the quasi-$\overline{S_{RDY}}$ signal at 2 ms intervals which the timer generates, and 2-byte data is transferred from the transmission side to the reception side.

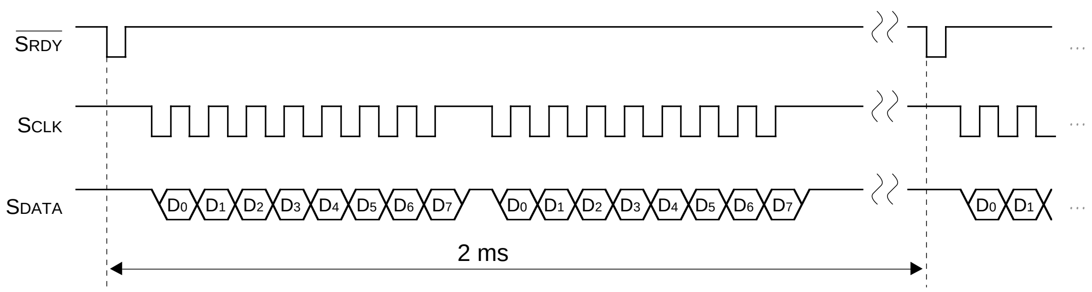


Fig. 2.3.16 Timing chart

Figures 2.3.17 and 2.3.19 show the registers setting relevant to the serial I/O2 and Figure 2.3.18 shows the transmission data setting of the serial I/O2.

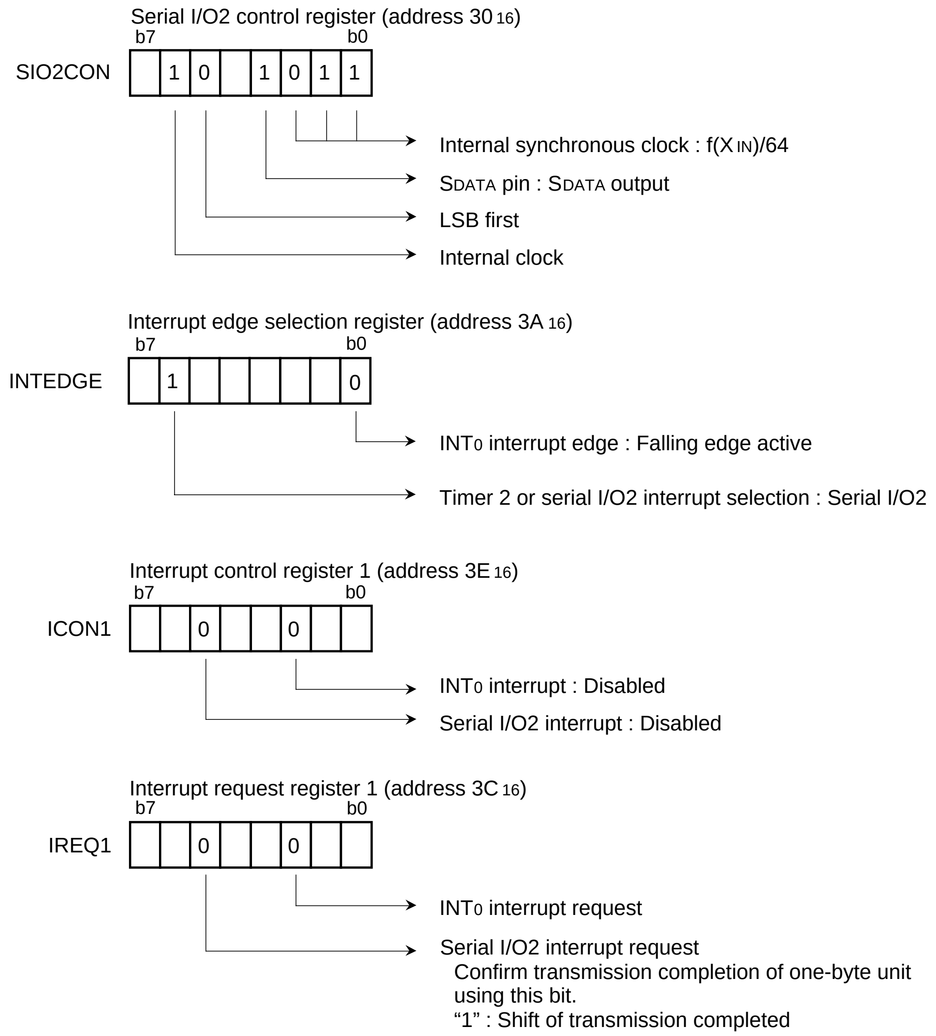


Fig. 2.3.17 Registers setting relevant to transmission side

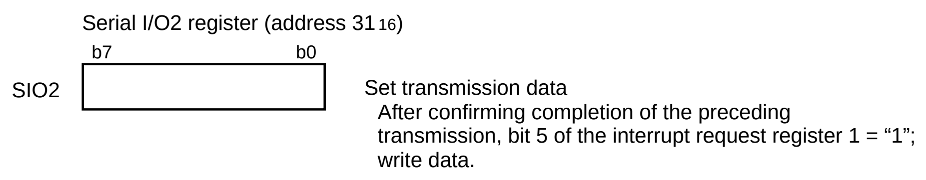


Fig. 2.3.18 Transmission data setting of serial I/O2

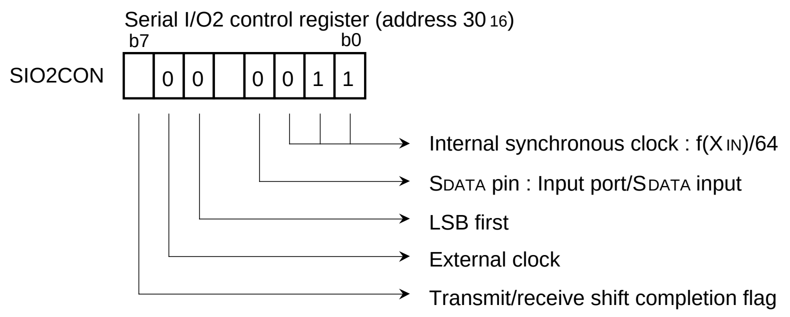


Fig. 2.3.19 Registers setting relevant to reception side

Figure 2.3.20 shows a control procedure of transmission side, and Figure 2.3.21 shows a control procedure of reception side.

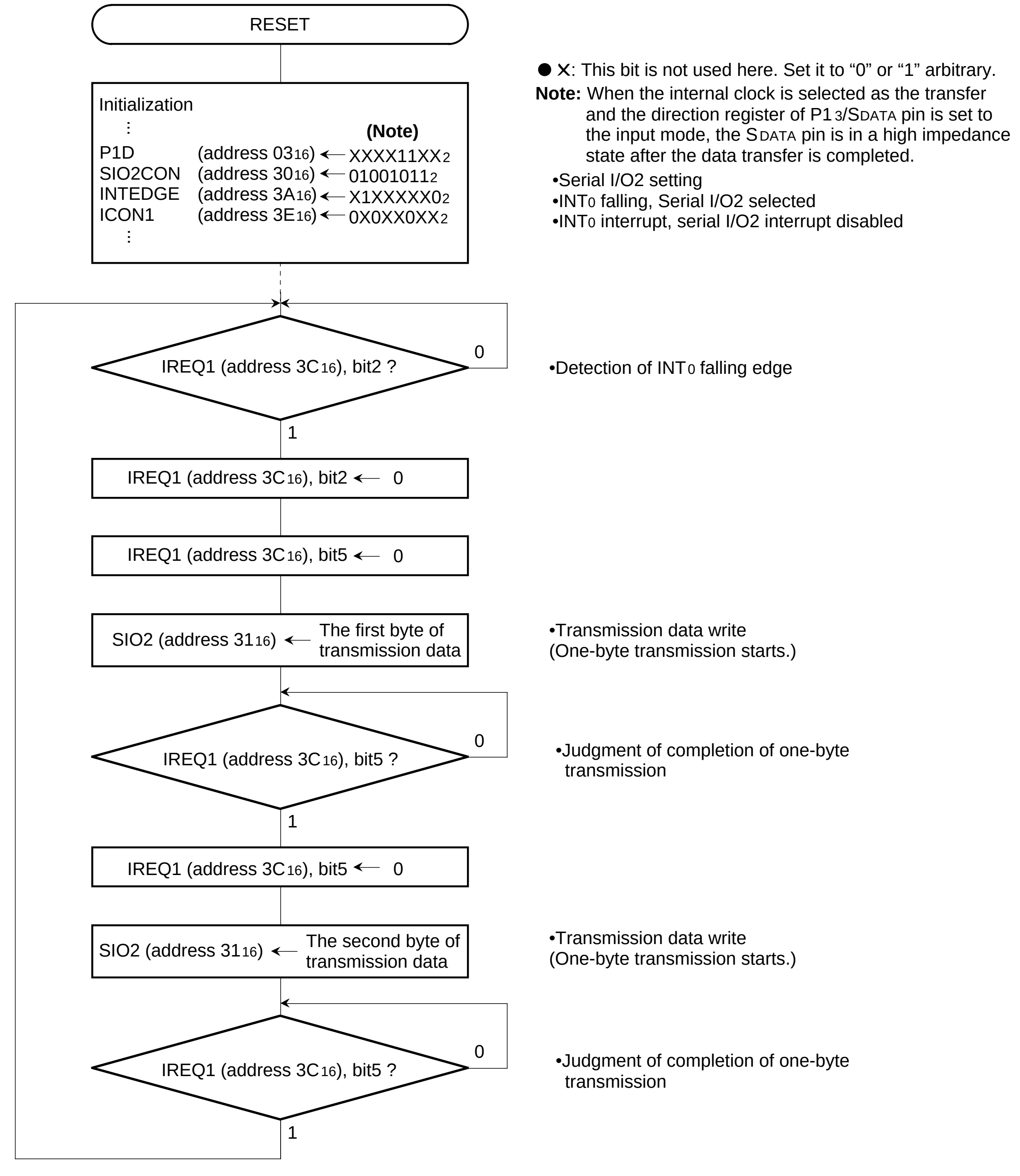


Fig. 2.3.20 Control procedure of transmission side

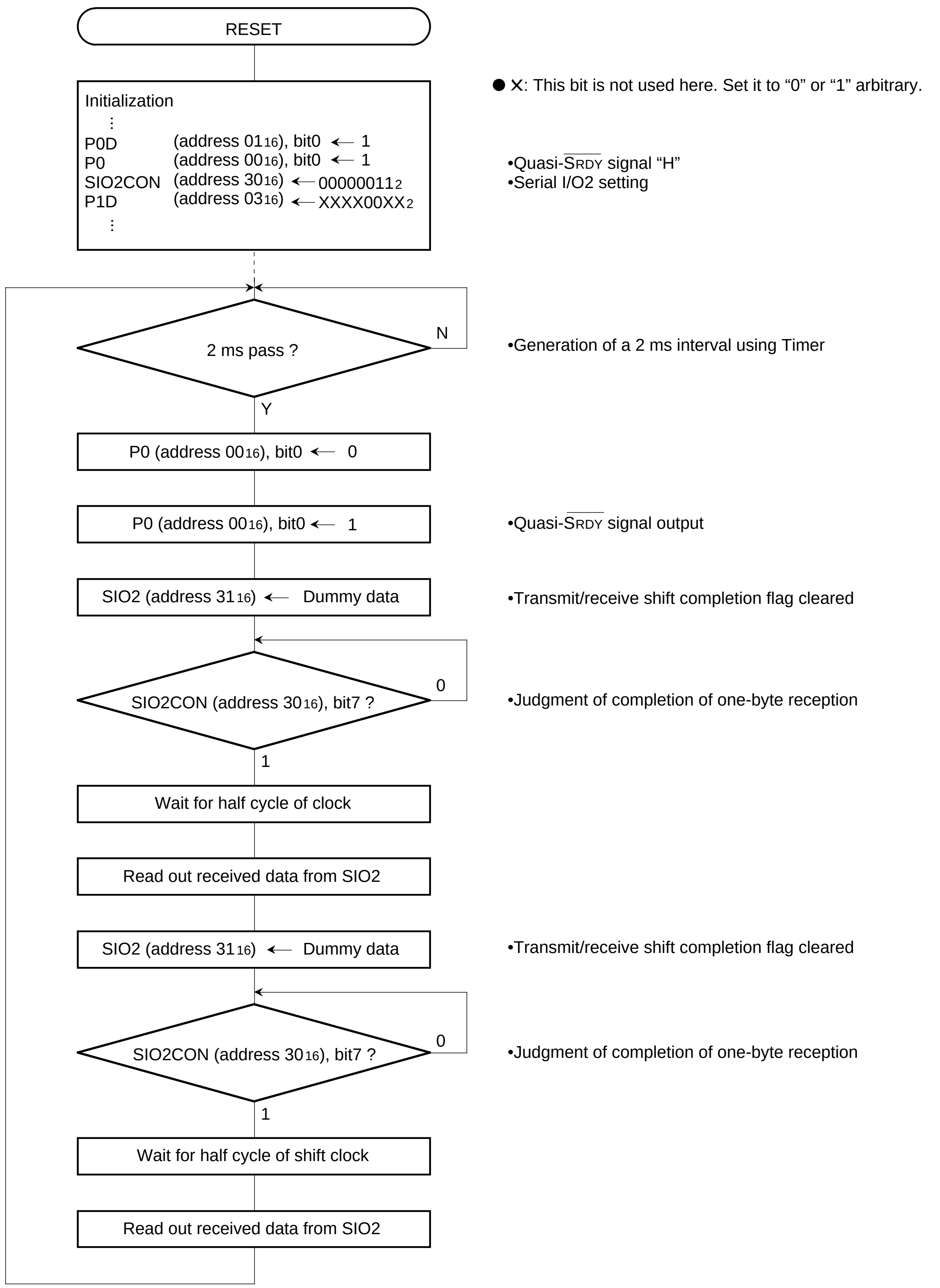


Fig. 2.3.21 Control procedure of reception side

(2) Communication using asynchronous serial I/O, UART (transmit/receive)

Outline : 2-byte data is transmitted and received, using the clock asynchronous serial I/O. Port $P0_0$ is used for communication control.

Figure 2.3.22 shows a connection diagram, and Figure 2.3.23 shows a timing chart.

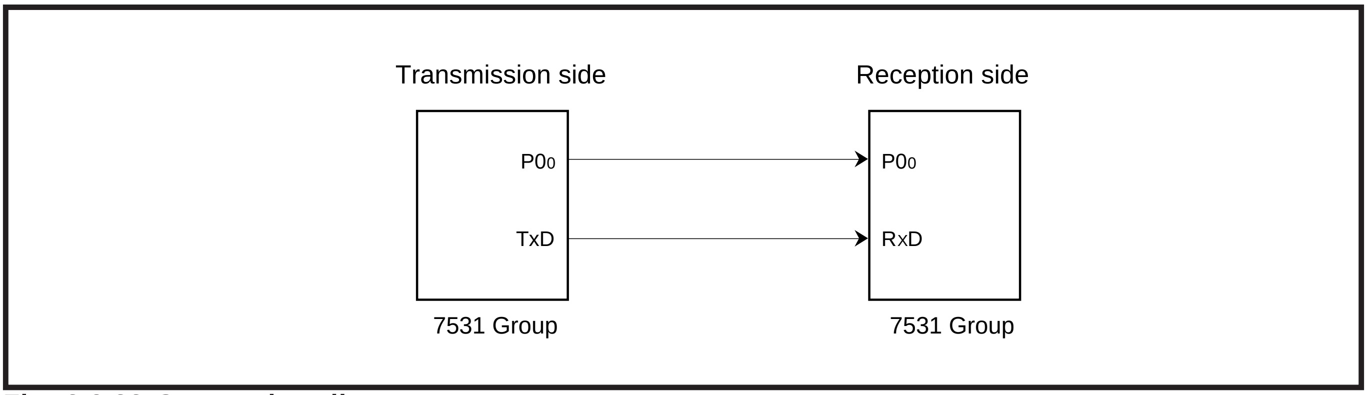


Fig. 2.3.22 Connection diagram

Specifications : •The Serial I/O1, asynchronous serial I/O, is used.
•Transfer bit rate : 9600 bps; f(X_{IN}) = 4.9152 MHz divided by 512
•Communication control using port $P0_0$; Port $P0_0$ output level is controlled by software.
•2-byte data is transferred from the transmission side to the reception side at 10 ms intervals which the timer generates

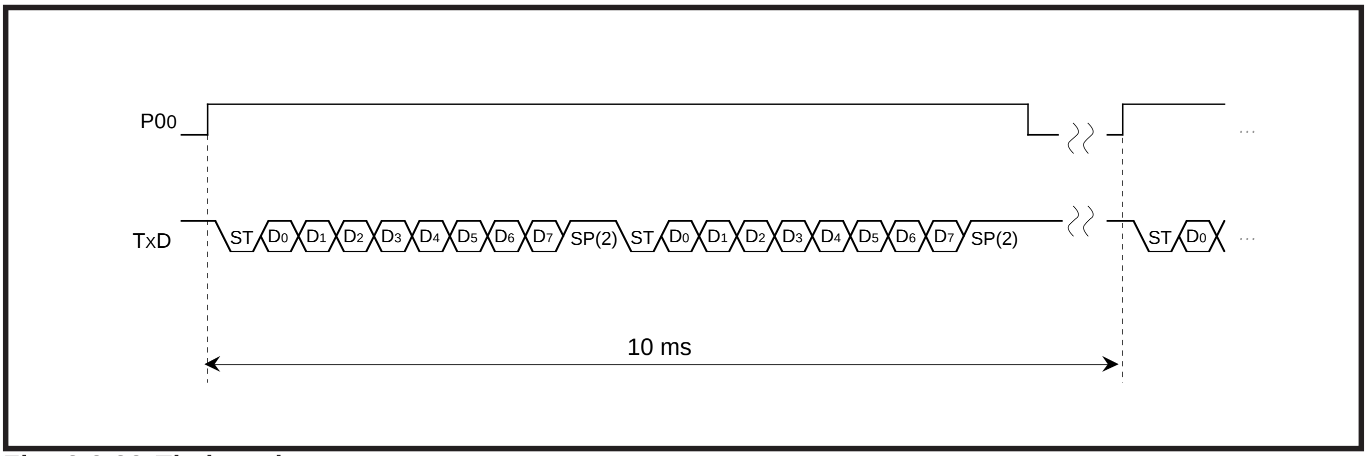


Fig. 2.3.23 Timing chart

Table 2.3.1 shows a setting example of the baud rate generator (BRG) and transfer bit rate values; Figure 2.3.23 shows the registers setting relevant to transmission side; Figure 2.3.24 shows the registers setting relevant to reception side

Table 2.3.1 Setting example of baud rate generator (BRG) and transfer bit rate values

BRG count source (**Note 1**)	BRG set value	Transfer bit rate (bps) (**Note 2**)	
		At $f(X_{IN})$ = 4.9152 MHz	At $f(X_{IN})$ = 8 MHz
$f(X_{IN})$ / 4	255 (FF_{16})	300	488.28125
$f(X_{IN})$ / 4	127 ($7F_{16}$)	600	976.5625
$f(X_{IN})$ / 4	63 ($3F_{16}$)	1200	1953.125
$f(X_{IN})$ / 4	31 ($1F_{16}$)	2400	3906.25
$f(X_{IN})$ / 4	15 ($0F_{16}$)	4800	7812.5
$f(X_{IN})$ / 4	7 (07_{16})	9600	15625
$f(X_{IN})$ / 4	3 (03_{16})	19200	31250
$f(X_{IN})$ / 4	1 (01_{16})	38400	62500
$f(X_{IN})$	3 (03_{16})	76800	125000
$f(X_{IN})$	1 (01_{16})	153600	250000
$f(X_{IN})$	0 (00_{16})	307200	500000

Notes 1: Select the BRG count source with bit 0 of the serial I/O1 control register (address $1A_{16}$).
2: Equation of transfer bit rate:

$$\text{Transfer bit rate (bps)} = \frac{f(X_{IN})}{(\text{BRG set value} + 1) \times 16 \times m^*}$$

m*: m = 1 in the case of bit 0 of the serial I/O1 control register (address $001A_{16}$) = “0”
m = 4 in the case of bit 0 of the serial I/O1 control register (address $001A_{16}$) = “1”

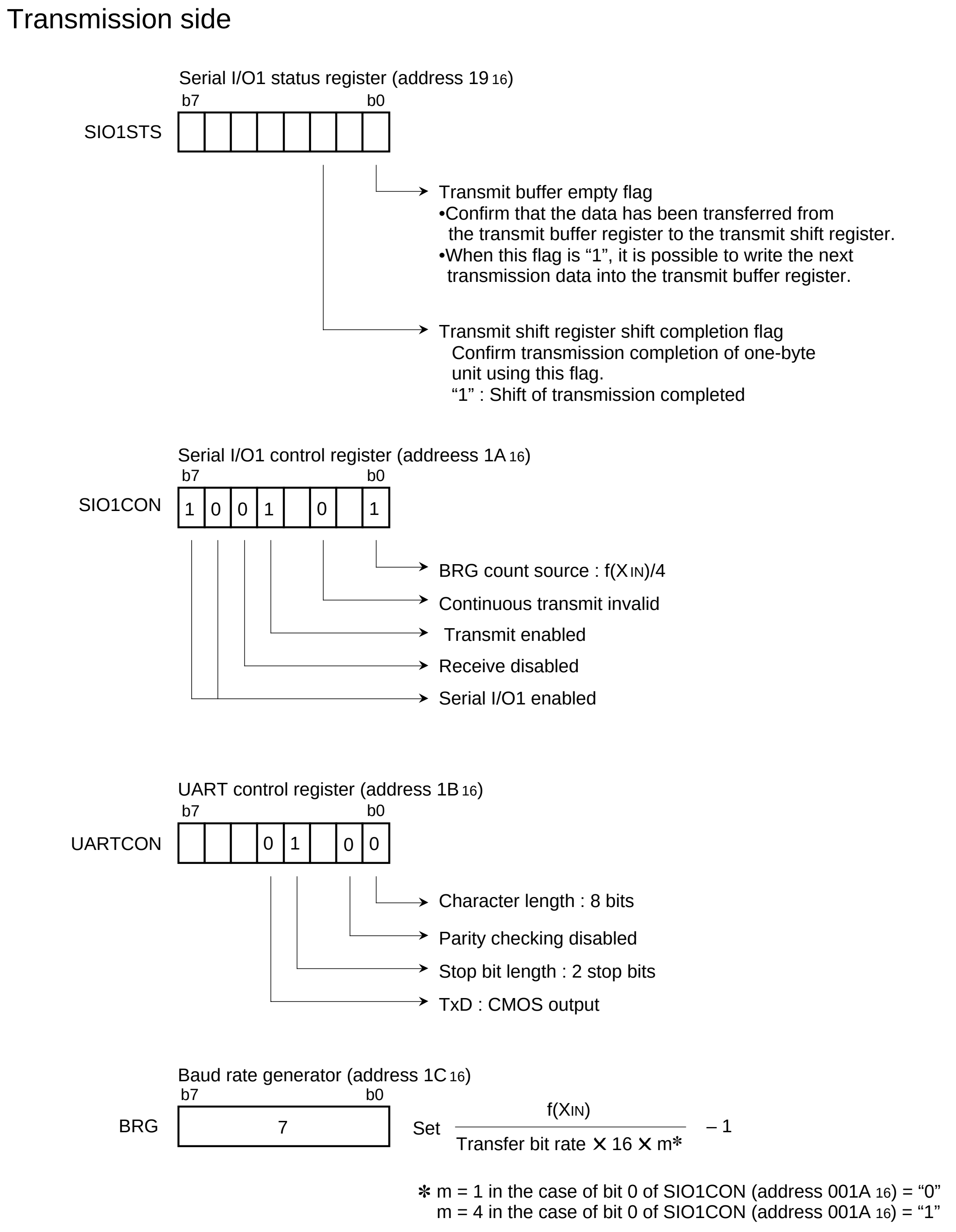


Fig. 2.3.24 Registers setting relevant to transmission side

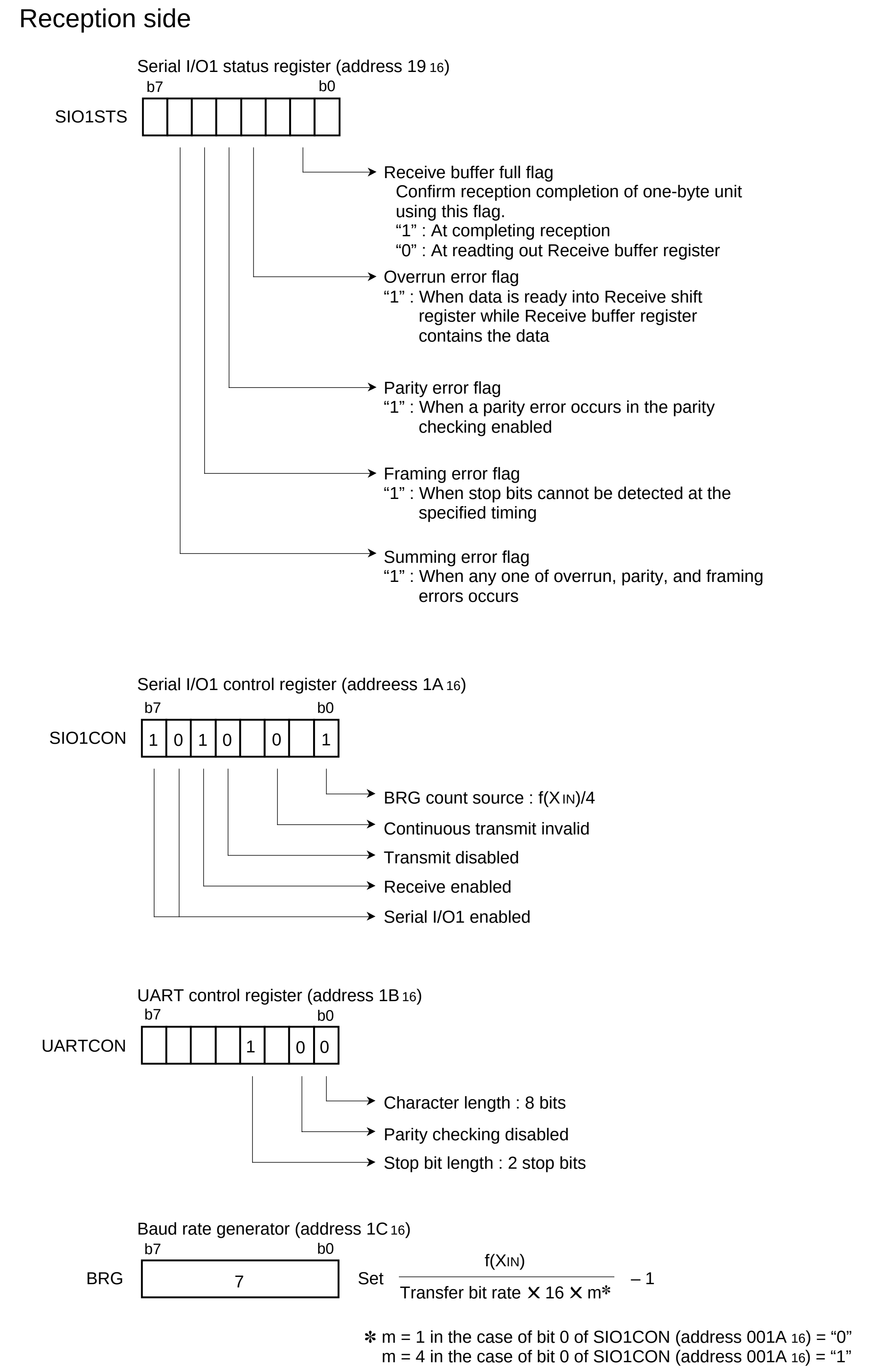


Fig. 2.3.25 Registers setting relevant to reception side

Figure 2.3.26 shows a control procedure of transmission side, and Figure 2.3.27 shows a control procedure of reception side.

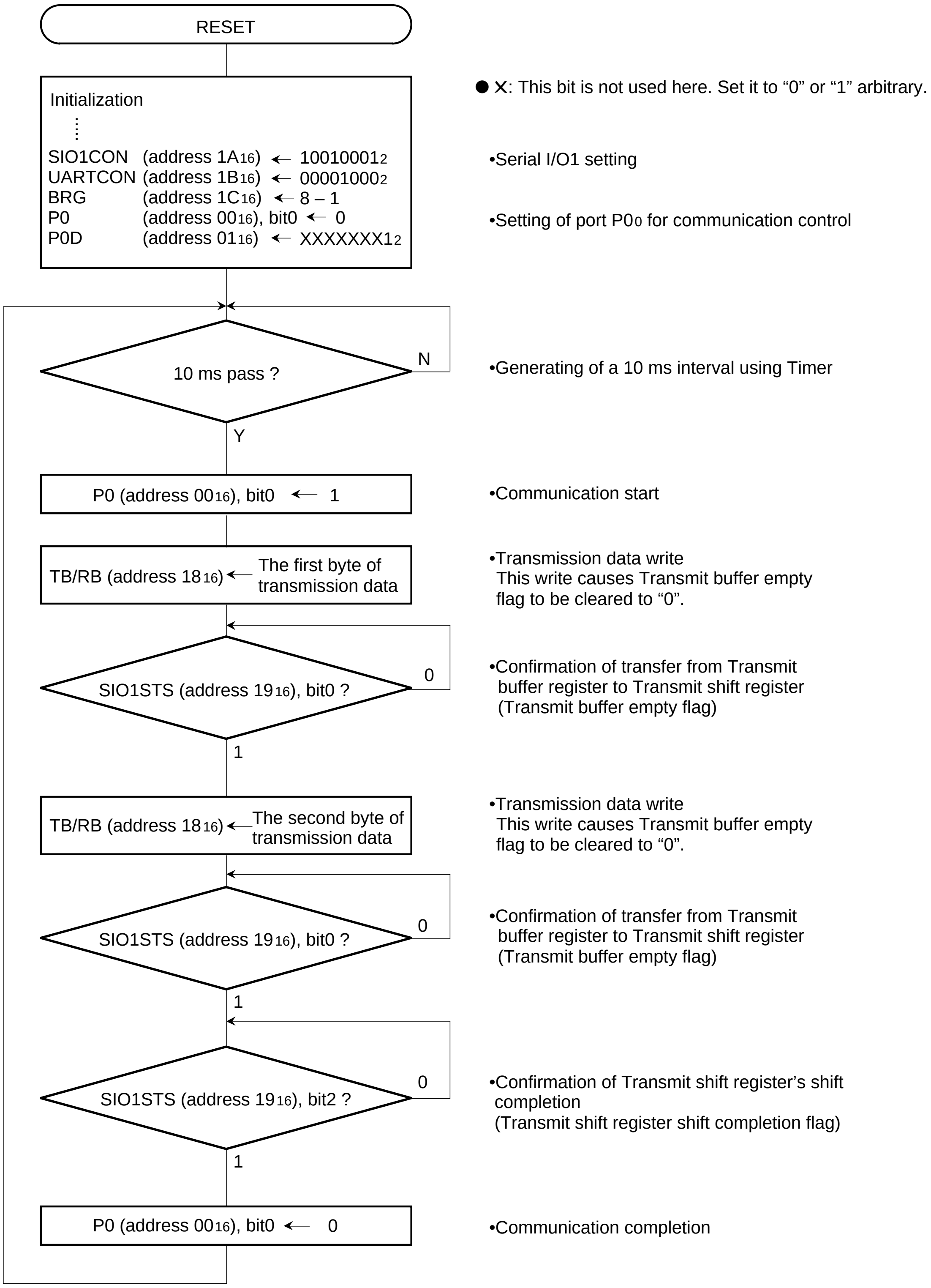


Fig. 2.3.26 Control procedure of transmission side

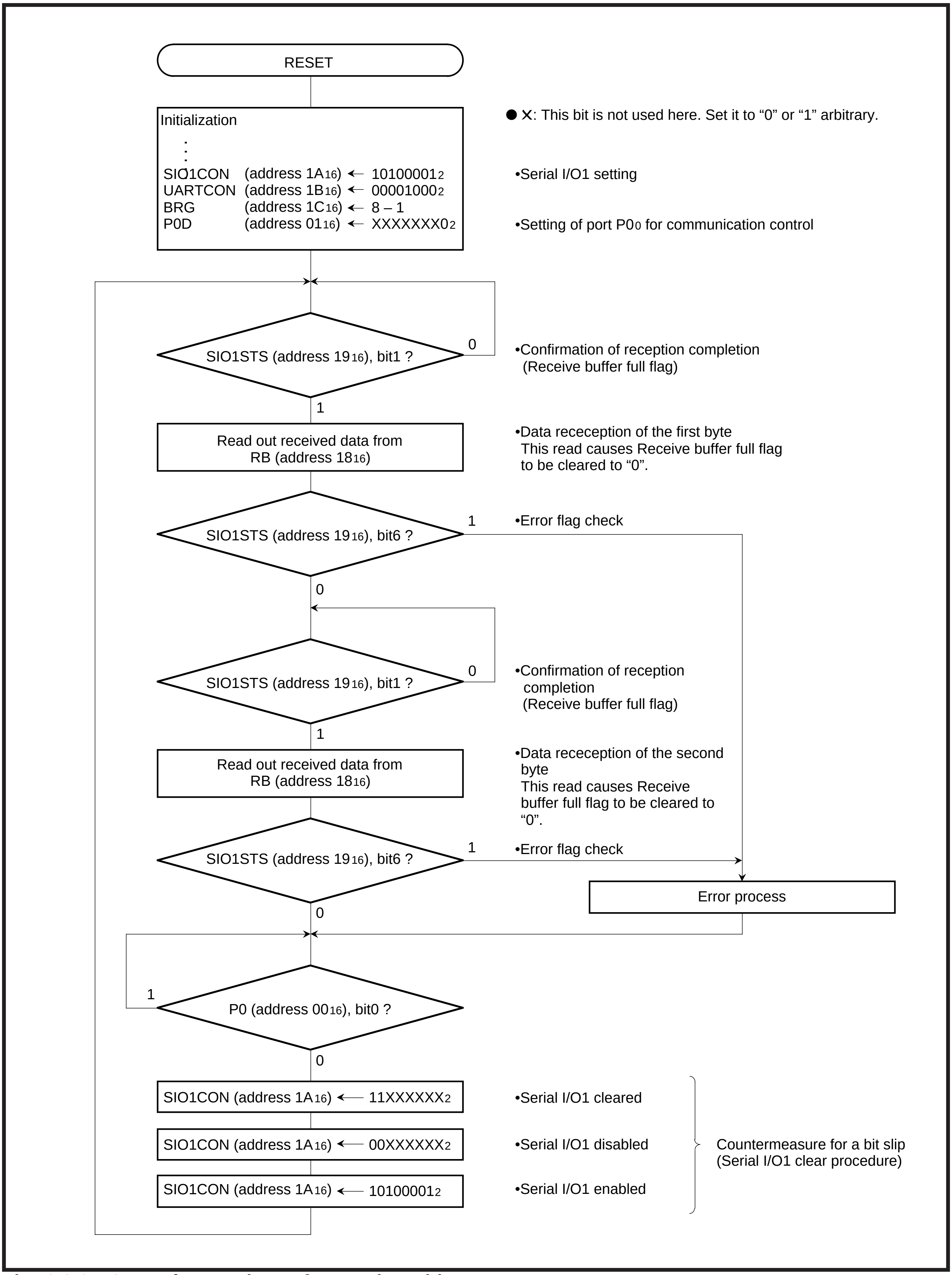
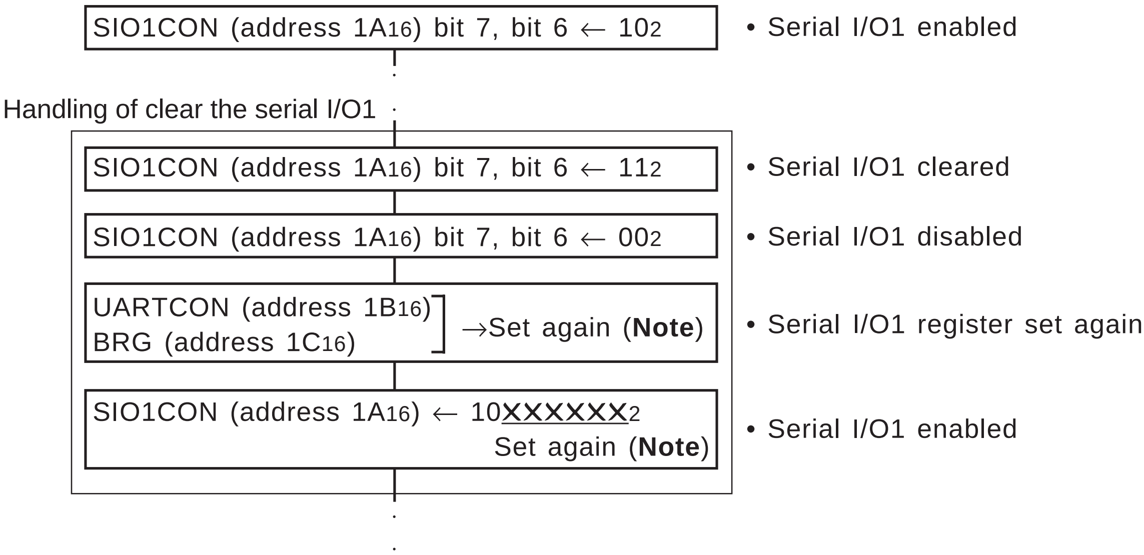


Fig. 2.3.27 Control procedure of reception side

2.3.6 Notes on serial I/O

(1) Handling of clear the serial I/O1

When serial I/O1 is set again or the transmit/receive operation is stopped/restarted while serial I/O1 is operating, clear the serial I/O1 as shown in Figure 2.3.28.



Note: When the contents of register is not changed, setting again is not necessary.

Fig. 2.3.28 Sequence of clearing serial I/O

(2) Data transmission control with referring to transmit shift register completion flag

The transmit shift register completion flag changes from "1" to "0" with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

(3) Writing transmit data

When an external clock is used as the synchronous clock for the clock synchronous serial I/O, write the transmit data to the transmit buffer register (serial I/O shift register) at "H" of the transfer clock input level.

(4) Serial I/O2 transmit/receive shift completion flag

- The transmit/receive shift completion flag of the serial I/O2 control register is set to "1" after completing transmit/receive shift. In order to set this flag to "0", write data (dummy data at reception) to the serial I/O2 register by program.
- Bit 7 of the serial I/O2 control register is set to "1" a half cycle (of the shift clock) earlier than completion of shift operation. Accordingly, when using this bit to confirm shift completion, a half cycle or more of the shift clock must pass after confirming that this bit is set to "1", before performing read/write to the serial I/O2 register.

2.4 A-D converter

This paragraph explains the registers setting method and the notes relevant to the A-D converter.

2.4.1 Memory map

Address	Register
0034_{16}	A-D control register (ADCON)
0035_{16}	A-D conversion register (low-order); (ADL)
0036_{16}	A-D conversion register (high-order); (ADH)
$003A_{16}$	Interrupt edge selection register (INTEDGE)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003E_{16}$	Interrupt control register 1 (ICON1)

Fig. 2.4.1 Memory map of registers relevant to A-D converter

2.4.2 Relevant registers

A-D control register

b7 b6 b5 b4 b3 b2 b1 b0

A-D control register (ADCON) [Address : 34_{16}]

B	Name	Function	At reset	R	W
0	Analog input pin selection bits	b2 b1 b0 0 0 0 : $P2_0/AN_0$ 0 0 1 : $P2_1/AN_1$ 0 1 0 : $P2_2/AN_2$ 0 1 1 : $P2_3/AN_3$ 1 0 0 : $P2_4/AN_4$ 1 0 1 : $P2_5/AN_5$ 1 1 0 : $P2_6/AN_6$ (**Note**) 1 1 1 : $P2_7/AN_7$ (**Note**)	0	○	○
1			0	○	○
2			0	○	○
3	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0".		0	○	×
4	AD conversion completion bit	0 : Conversion in progress 1 : Conversion completed	1	○	✻
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".		0	○	×
6			0	○	×
7			0	○	×

Note: These can be used only for the 36-pin package versions.
✻: This bit can be cleared to "0" by program, but cannot be set to "1".

Fig. 2.4.2 Structure of A-D control register

A-D conversion register (high-order)

b7 b6 b5 b4 b3 b2 b1 b0

A-D conversion register (high-order) (ADH) [Address : 36 16]

B	Function	At reset	R	W
0	The read-only register in which the A-D conversion's results are stored. < 10-bit read> b7 … b0: b9 b8 (b1, b0)	?	○	×
1		?	○	×
2	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".	?	○	×
3		?	○	×
4		?	○	×
5		?	○	×
6		?	○	×
7		?	○	×

Fig. 2.4.3 Structure of A-D conversion register (high-order)

A-D conversion register (low-order)

b7 b6 b5 b4 b3 b2 b1 b0

A-D conversion register (low-order) (ADL) [Address : 35 16]

B	Function	At reset	R	W
0	The read-only register in which the A-D conversion's results are stored. < 8-bit read> b7 … b0: b9 b8 b7 b6 b5 b4 b3 b2 < 10-bit read> b7 … b0: b7 b6 b5 b4 b3 b2 b1 b0	?	○	×
1		?	○	×
2		?	○	×
3		?	○	×
4		?	○	×
5		?	○	×
6		?	○	×
7		?	○	×

Fig. 2.4.4 Structure of A-D conversion register (low-order)

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt edge selection register (INTEDGE) [Address : 3A16]

B	Name	Function	At reset	R	W
0	INT_0 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
1	INT_1 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
2	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".		0	○	×
3			0	○	×
4	Serial I/O1 or INT_1 interrupt selection bit (**Note**)	0 : Serial I/O1 1 : INT_1	0	○	○
5	Timer X or key-on wake up interrupt selection bit	0 : Timer X 1 : Key-on wake up	0	○	○
6	Timer 2 or serial I/O2 interrupt selection bit	0 : Timer 2 1 : Serial I/O2	0	○	○
7	$CNTR_0$ or AD converter interrupt selection bit	0 : $CNTR_0$ 1 : AD converter	0	○	○

Note: Do not write "1" to bit 4 in the 32-pin package versions.

Fig. 2.4.5 Structure of Interrupt edge selection register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address : 3C16]

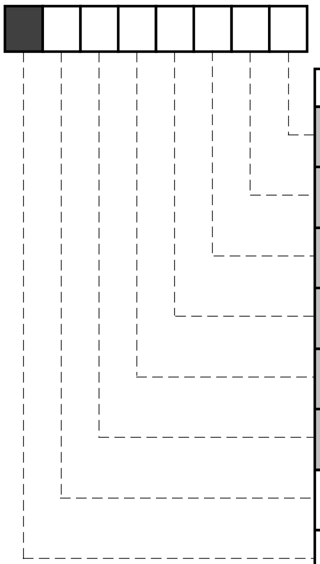
B	Name	Function	At reset	R	W
0	Serial I/O1 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
1	Serial I/O1 transmit or INT_1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
2	INT_0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
3	Timer X or key-on wake up interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
4	Timer 1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
5	Timer 2 or serial I/O2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
6	$CNTR_0$ or AD converter interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0".		0	○	×

✻: These bits can be cleared to "0" by program, but cannot be set to "1".

Fig. 2.4.6 Structure of Interrupt request register 1

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0



Interrupt control register 1 (ICON1) [Address : $3E_{16}$]

B	Name	Function	At reset	R	W
0	Serial I/O1 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Serial I/O1 transmit or INT_1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	INT_0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Timer X or key-on wake up interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Timer 2 or serial I/O2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	$CNTR_0$ or AD converter interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Nothing is allocated for this bit. Do not write “1” to this bit. When this bit is read out, the value is “0”.		0	○	×

Fig. 2.4.7 Structure of Interrupt control register 1

2.4.3 A-D converter application examples

(1) Conversion of analog input voltage

Outline : The analog input voltage input from a sensor is converted to digital values.

Figure 2.4.8 shows a connection diagram, and Figure 2.4.9 shows the relevant registers setting.

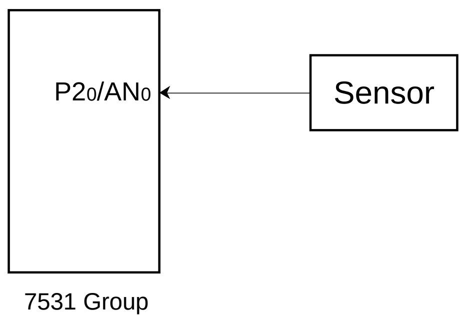


Fig. 2.4.8 Connection diagram

Specifications : •The analog input voltage input from a sensor is converted to digital values.
•$P2_0/AN_0$ pin is used as an analog input pin.

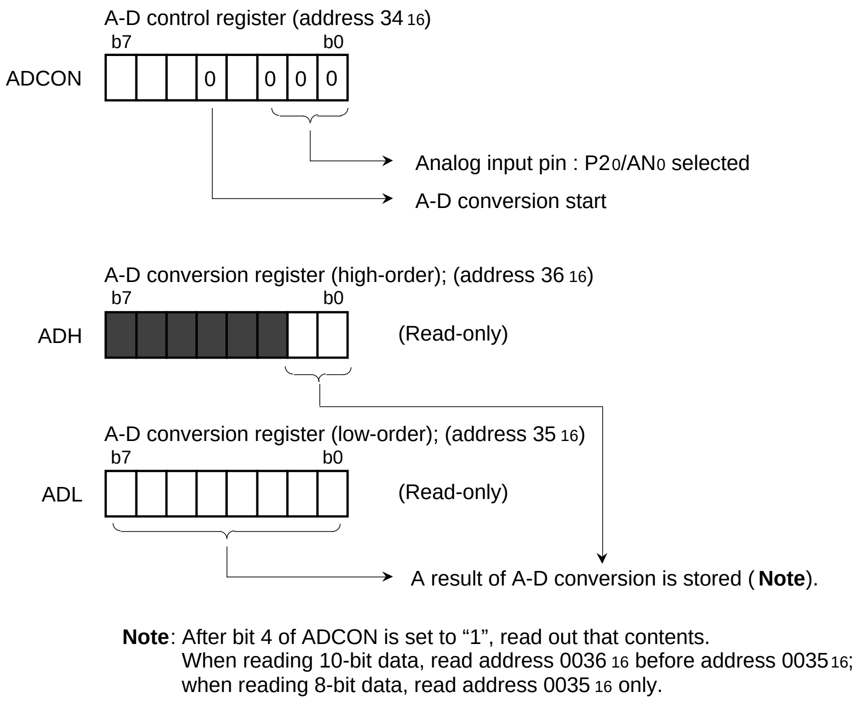


Fig. 2.4.9 Relevant registers setting

An analog input signal from a sensor is converted to the digital value according to the relevant registers setting shown by Figure 2.4.9. Figure 2.4.10 shows the control procedure for 8-bit read, and Figure 2.4.11 shows the control procedure for 10-bit read.

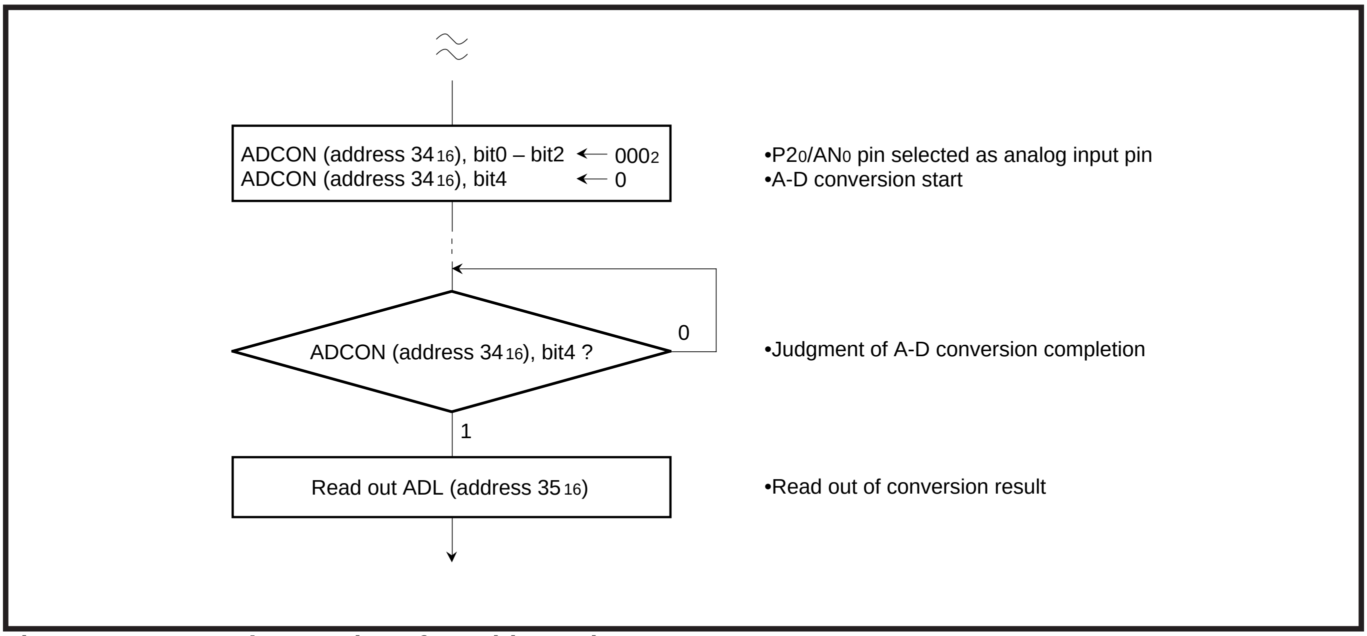


Fig. 2.4.10 Control procedure for 8-bit read

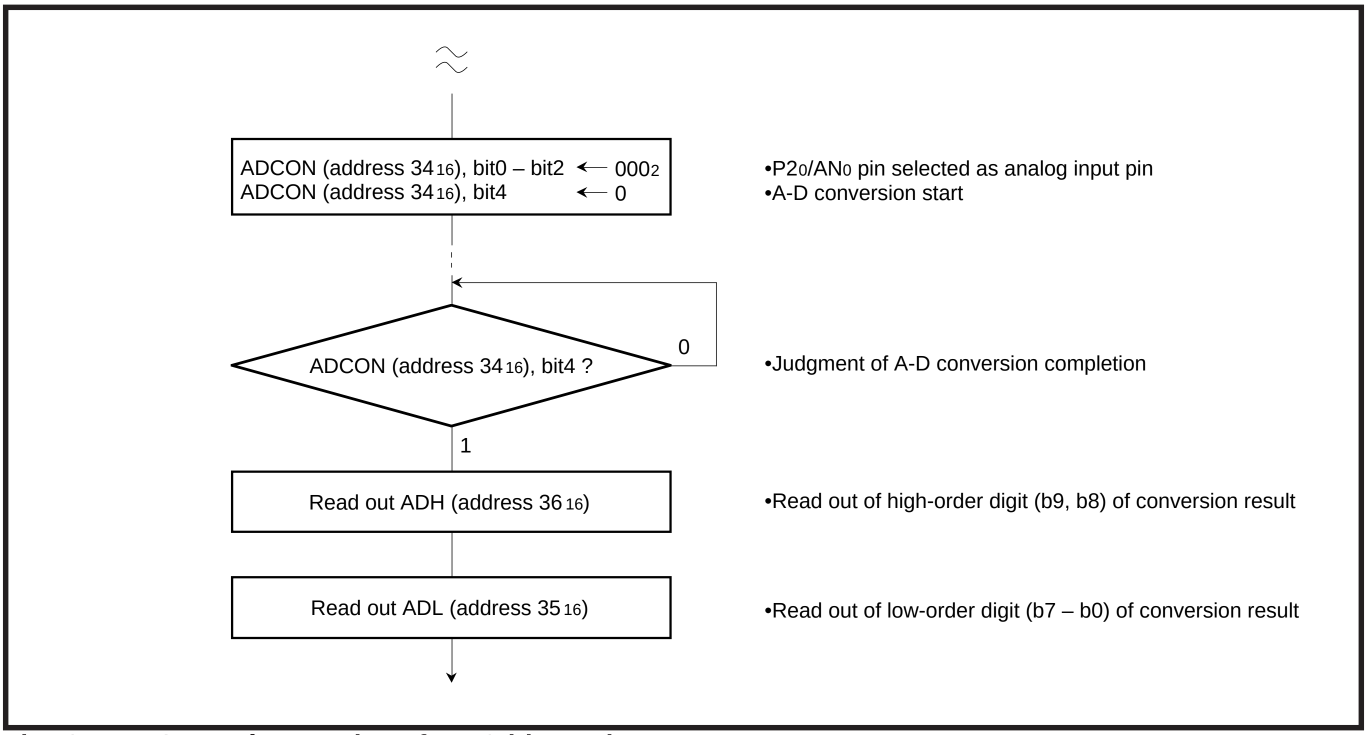


Fig. 2.4.11 Control procedure for 10-bit read

2.4.4 Notes on A-D converter

(1) Analog input pin

Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01µF to 1µF. Further, be sure to verify the operation of application products on the user side.

● **Reason**

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A-D conversion/comparison precision to be worse.

(2) Clock frequency during A-D conversion

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. Thus, make sure the following during an A-D conversion.

- $f(X_{IN})$ is 500 kHz or more
- Do not execute the **STP** instruction

2.5 Reset

2.5.1 Connection example of reset IC

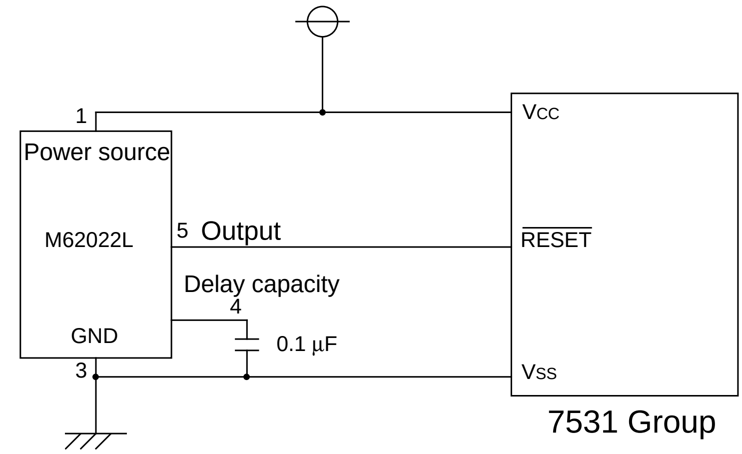


Fig. 2.5.1 Example of poweron reset circuit

Figure 2.5.2 shows the system example which switches to the RAM backup mode by detecting a drop of the system power source voltage with the INT interrupt.

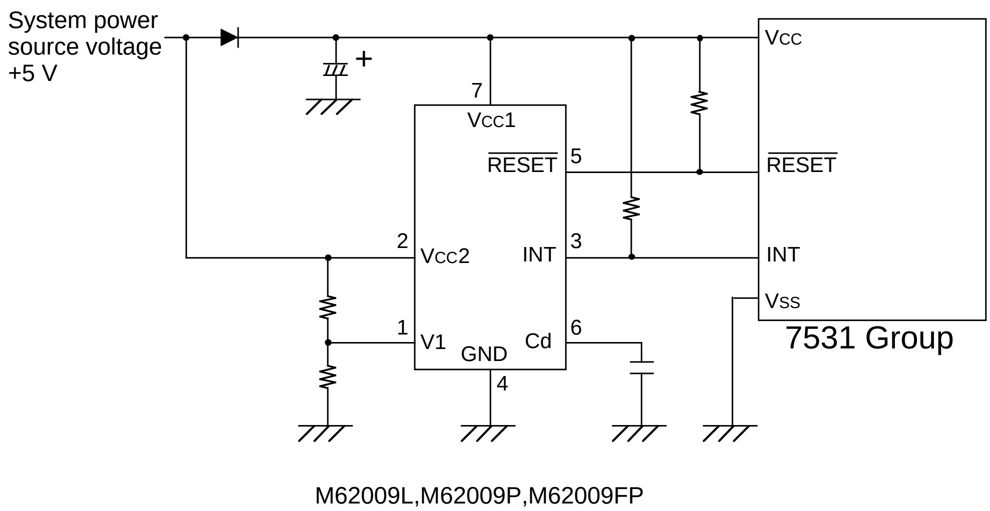


Fig. 2.5.2 RAM backup system

2.5.2 Notes on $\overline{\text{RESET}}$ pin

Connecting capacitor

In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and the V_{SS} pin. Use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following :

• Make the length of the wiring which is connected to a capacitor as short as possible.
• Be sure to verify the operation of application products on the user side.

● **Reason**

If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

MEMO

CHAPTER 3

APPENDIX

3.1 Electrical characteristics
3.2 Typical characteristics
3.3 Notes on use
3.4 Countermeasures against noise
3.5 List of registers
3.6 Mask ROM confirmation form
3.7 ROM programming confirmation form
3.8 Mark specification form
3.9 Package outline
3.10 Machine instructions
3.11 List of instruction code
3.12 SFR memory map
3.13 Pin configurations

3.1 Electrical characteristics

3.1.1 7531 Group (General purpose)

Applied to: M37531M4-XXXFP/SP/GP, M37531M8-XXXFP/SP/GP, M37531E4FP/SP/GP, M37531E8FP/SP

(1) Absolute maximum ratings (General purpose)

Table 3.1.1 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage		All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	CNV_{SS} (Note 1)		–0.3 to 13	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		Ta = 25°C	300 (Note 2)	mW
T_{opr}	Operating temperature			–20 to 85	°C
T_{stg}	Storage temperature			–40 to 125	°C

Note 1: It is a rating only for the One Time PROM version. Connect to V_{SS} for the mask ROM version.
2: 200 mW for the 32P6B package product.

(2) Recommended operating conditions (General purpose)

Table 3.1.2 Recommended operating conditions (1)
(V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (ceramic)	f(X_{IN}) = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 2 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
		f(X_{IN}) = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 1 MHz (Double-speed mode)	2.2	5.0	5.5	V
	Power source voltage (CR)	f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 1 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)	2.0		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$, X_{IN}	$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	0		$0.3V_{CC}$	V
V_{IL}	"L" input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)	0		0.8	V
V_{IL}	"L" input voltage	$\overline{RESET}$, CNV_{SS}	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage	X_{IN}	0		$0.16V_{CC}$	V
$\Sigma I_{OH(peak)}$	"H" total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 2)	$P3_0$–$P3_6$			60	mA
$\Sigma I_{OH(avg)}$	"H" total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 2)	$P3_0$–$P3_6$			30	mA

Note 1: Vcc = 4.0 to 5.5V
2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

3.1 Electrical characteristics

Table 3.1.3 Recommended operating conditions (2)
(V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
$I_{OH(peak)}$	"H" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P3_0$–$P3_6$			30	mA
$I_{OH(avg)}$	"H" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P3_0$–$P3_6$			15	mA
$f(X_{IN})$	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V Double-speed mode			4	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V Double-speed mode			2	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.2 to 5.5 V Double-speed mode			1	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.2 to 5.5 V High-, Middle-speed mode			2	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.2 to 5.5 V High-, Middle-speed mode			1	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50 %.

(3) Electrical characteristics (General purpose)

Table 3.1.4 Electrical characteristics
(V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ (Note 1)	I_{OH} = –5 mA V_{CC} = 4.0 to 5.5 V	V_{CC}–1.5			V
			I_{OH} = –1.0 mA V_{CC} = 2.2 to 5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$	I_{OL} = 5 mA V_{CC} = 4.0 to 5.5 V			1.5	V
			I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
			I_{OL} = 1.0 mA V_{CC} = 2.2 to 5.5 V			1.0	V
V_{OL}	"L" output voltage	$P3_0$–$P3_6$	I_{OL} = 15 mA V_{CC} = 4.0 to 5.5 V			2.0	V
			I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
			I_{OL} = 10 mA V_{CC} = 2.2 to 5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis	$CNTR_0$, INT_0, INT_1(Note 2) $P0_0$–$P0_7$ (Note 3)			0.4		V
V_{T+}–V_{T-}	Hysteresis	R_XD, S_{CLK}, S_{DATA} (Note 2)			0.5		V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$			0.5		V
I_{IH}	"H" input current	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{CC} (Pin floating. Pull up transistors "off")			5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pin floating. Pull up transistors "off")			–5.0	µA
I_{IL}	"L" input current	$\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}		–4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pull up transistors "on")		–0.2	–0.5	mA
V_{RAM}	RAM hold voltage		When clock stopped	2.0		5.5	V
I_{CC}	Power source current		High-speed mode, f(X_{IN}) = 8 MHz Output transistors "off"		5.0	8.0	mA
			High-speed mode, f(X_{IN}) = 2 MHz, V_{CC} = 2.2 V Output transistors "off"		0.5	1.5	mA
			Double-speed mode, f(X_{IN}) = 4 MHz Output transistors "off"		5.0	8.0	mA
			Middle-speed mode, f(X_{IN}) = 8 MHz Output transistors "off"		2.0	5.0	mA
			f(X_{IN}) = 8 MHz (in WIT state) Functions except timers 1 and 2 stop Output transistors "off"		1.6	3.2	mA
			f(X_{IN}) = 2 MHz, V_{CC} = 2.2 V (in WIT state) Output transistors "off"		0.2		mA
			Increment when A-D conversion is executed f(X_{IN}) = 8 MHz, V_{CC} = 5 V		0.5		mA
			All oscillation stopped (in STP state) Output transistors "off" — Ta = 25 °C		0.1	1.0	µA
			All oscillation stopped (in STP state) Output transistors "off" — Ta = 85 °C			10	µA

Notes 1: $P1_1$ is measured when the $P1_1$/T_XD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: R_XD, S_{CLK}, S_{DATA}, INT_0, and INT_1 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake up.

3.1 Electrical characteristics

(4) A-D converter characteristics (General purpose)

Table 3.1.5 A-D Converter characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±0.9	LSB
V_{OT}	Zero transition voltage	V_{CC} = V_{REF} = 5.12 V	0	5	20	mV
		V_{CC} = V_{REF} = 3.072 V	0	3	15	mV
V_{FST}	Full scale transition voltage	V_{CC} = V_{REF} = 5.12 V	5105	5115	5125	mV
		V_{CC} = V_{REF} = 3.072 V	3060	3069	3075	mV
t_{CONV}	Conversion time				122	tc(X_{IN})
R_{LADDER}	Ladder resistor			55		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	150	200	µA
		V_{REF} = 3.0 V	30	70	120	
$I_{I(AD)}$	A-D port input current				5.0	µA

(5) Timing requirements (General purpose)

Table 3.1.6 Timing requirements (1)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input “L” pulse width	15			µs
$t_C(X_{IN})$	External clock input cycle time	125			ns
$t_{WH}(X_{IN})$	External clock input “H” pulse width	50			ns
$t_{WL}(X_{IN})$	External clock input “L” pulse width	50			ns
$t_C(CNTR)$	$CNTR_0$ input cycle time	200			ns
$t_{WH}(CNTR)$	$CNTR_0$, INT_0, INT_1, input “H” pulse width	80			ns
$t_{WL}(CNTR)$	$CNTR_0$, INT_0, INT_1, input “L” pulse width	80			ns
$t_C(S_{CLK})$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH}(S_{CLK})$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL}(S_{CLK})$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su}(S_{CLK}–S_{DATA})$	Serial I/O2 input set up time	200			ns
$t_h(S_{CLK}–S_{DATA})$	Serial I/O2 input hold time	200			ns

Table 3.1.7 Timing requirements (2)
(V_{CC} = 2.2 to 5.5 V or 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input “L” pulse width	V_{CC} = 2.2 to 5.5 V	45			µs
		V_{CC} = 2.4 to 5.5 V	35			µs
$t_C(X_{IN})$	External clock input cycle time	V_{CC} = 2.2 to 5.5 V	500			ns
		V_{CC} = 2.4 to 5.5 V	250			ns
$t_{WH}(X_{IN})$	External clock input “H” pulse width	V_{CC} = 2.2 to 5.5 V	200			ns
		V_{CC} = 2.4 to 5.5 V	100			ns
$t_{WL}(X_{IN})$	External clock input “L” pulse width	V_{CC} = 2.2 to 5.5 V	200			ns
		V_{CC} = 2.4 to 5.5 V	100			ns
$t_C(CNTR)$	$CNTR_0$ input cycle time	V_{CC} = 2.2 to 5.5 V	1000			ns
		V_{CC} = 2.4 to 5.5 V	500			ns
$t_{WH}(CNTR)$	$CNTR_0$, INT_0, INT_1, input “H” pulse width	V_{CC} = 2.2 to 5.5 V	460			ns
		V_{CC} = 2.4 to 5.5 V	230			ns
$t_{WL}(CNTR)$	$CNTR_0$, INT_0, INT_1, input “L” pulse width	V_{CC} = 2.2 to 5.5 V	460			ns
		V_{CC} = 2.4 to 5.5 V	230			ns
$t_C(S_{CLK})$	Serial I/O2 clock input cycle time	V_{CC} = 2.2 to 5.5 V	4000			ns
		V_{CC} = 2.4 to 5.5 V	2000			ns
$t_{WH}(S_{CLK})$	Serial I/O2 clock input “H” pulse width	V_{CC} = 2.2 to 5.5 V	1900			ns
		V_{CC} = 2.4 to 5.5 V	950			ns
$t_{WL}(S_{CLK})$	Serial I/O2 clock input “L” pulse width	V_{CC} = 2.2 to 5.5 V	1900			ns
		V_{CC} = 2.4 to 5.5 V	950			ns
$t_{su}(S_{CLK}–S_{DATA})$	Serial I/O2 input set up time		400			ns
$t_h(S_{CLK}–S_{DATA})$	Serial I/O2 input hold time		400			ns

(6) Switching characteristics (General purpose)

Table 3.1.8 Switching characteristics (1)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH}(SCLK)	Serial I/O2 clock output “H” pulse width	t_C(SCLK)/2–30			ns
t_{WL}(SCLK)	Serial I/O2 clock output “L” pulse width	t_C(SCLK)/2–30			ns
t_d(SCLK–SDATA)	Serial I/O2 output delay time			140	ns
t_v(SCLK–SDATA)	Serial I/O2 output valid time	0			ns
t_r(SCLK)	Serial I/O2 clock output rising time			30	ns
t_f(SCLK)	Serial I/O2 clock output falling time			30	ns
t_r(CMOS)	CMOS output rising time (Note 1)		10	30	ns
t_f(CMOS)	CMOS output falling time (Note 1)		10	30	ns

Note 1: Pin XOUT is excluded.

Table 3.1.9 Switching characteristics (2)
(V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH}(SCLK)	Serial I/O2 clock output “H” pulse width	t_C(SCLK)/2–50			ns
t_{WL}(SCLK)	Serial I/O2 clock output “L” pulse width	t_C(SCLK)/2–50			ns
t_d(SCLK–SDATA)	Serial I/O2 output delay time			350	ns
t_v(SCLK–SDATA)	Serial I/O2 output valid time	0			ns
t_r(SCLK)	Serial I/O2 clock output rising time			50	ns
t_f(SCLK)	Serial I/O2 clock output falling time			50	ns
t_r(CMOS)	CMOS output rising time (Note 1)		20	50	ns
t_f(CMOS)	CMOS output falling time (Note 1)		20	50	ns

Note 1: Pin XOUT is excluded.

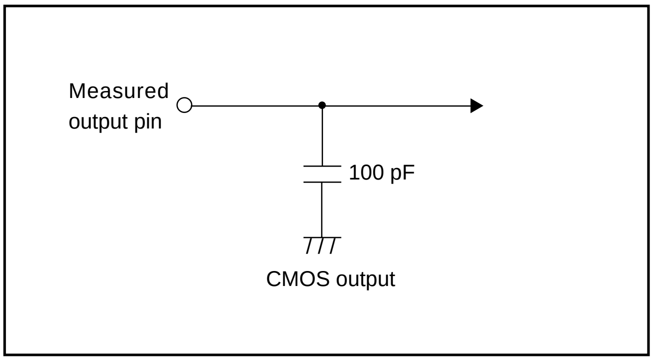


Fig. 3.1.1 Switching characteristics measurement circuit diagram (General purpose)

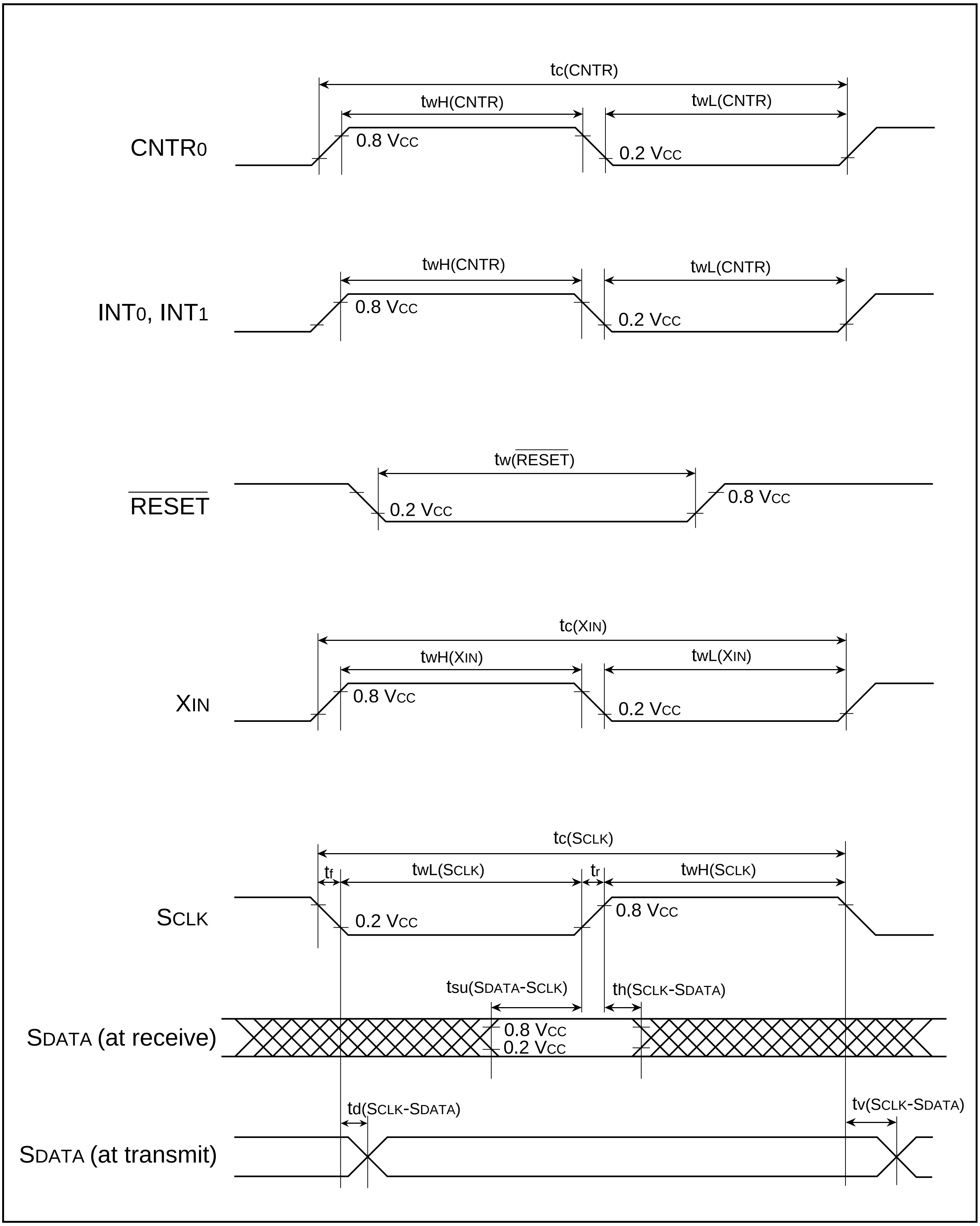


Fig. 3.1.2 Timing chart (General purpose)

3.1.2 7531 Group (Extended operating temperature version)

Applied to: M37531M4T-XXXFP/SP/GP, M37531E4T-XXXGP

(1) Absolute maximum ratings (Extended operating temperature version)

Table 3.1.10 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage		All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	CNV_{SS} (Note 1)		–0.3 to 13	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		Ta = 25°C	300 (Note 2)	mW
T_{opr}	Operating temperature			–40 to 85	°C
T_{stg}	Storage temperature			–65 to 150	°C

Notes 1: It is a rating only for the One Time PROM version. Connect to V_{SS} for the mask ROM version.
2: 200 mW for the 32P6B package version.

(2) Recommended operating conditions (Extended operating temperature version)

Table 3.1.11 Recommended operating conditions (1)
(V_{CC} = 2.4 to 5.5 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Power source voltage (ceramic)	$f(X_{IN})$ = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		$f(X_{IN})$ = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		$f(X_{IN})$ = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		$f(X_{IN})$ = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
	Power source voltage (CR)	$f(X_{IN})$ = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		$f(X_{IN})$ = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)	2.0		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$, X_{IN}	$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	0		$0.3V_{CC}$	V
V_{IL}	"L" input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)	0		0.8	V
V_{IL}	"L" input voltage	$\overline{RESET}$, CNV_{SS}	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage	X_{IN}	0		$0.16V_{CC}$	V
$\Sigma I_{OH(peak)}$	"H" total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 2)	$P3_0$–$P3_6$			60	mA
$\Sigma I_{OH(avg)}$	"H" total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 2)	$P3_0$–$P3_6$			30	mA

Note 1: Vcc = 4.0 to 5.5V
2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Table 3.1.12 Recommended operating conditions (2)
(V_{CC} = 2.4 to 5.5 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	“H” peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–10	mA
$I_{OL(peak)}$	“L” peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			10	mA
$I_{OL(peak)}$	“L” peak output current (Note 1)	$P3_0$–$P3_6$			30	mA
$I_{OH(avg)}$	“H” average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–5	mA
$I_{OL(avg)}$	“L” average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			5	mA
$I_{OL(avg)}$	“L” average output current (Note 2)	$P3_0$–$P3_6$			15	mA
$f(X_{IN})$	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V Double-speed mode			4	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V Double-speed mode			2	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50 %.

(3) Electrical characteristics (Extended operating temperature version)

Table 3.1.13 Electrical characteristics
(Vcc = 2.4 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
VOH	"H" output voltage	P00–P07, P10–P14, P20–P27, P30–P37 (Note 1)	IOH = –5 mA VCC = 4.0 to 5.5 V	VCC–1.5			V
			IOH = –1.0 mA VCC = 2.4 to 5.5 V	VCC–1.0			V
VOL	"L" output voltage	P00–P07, P10–P14, P20–P27, P37	IOL = 5 mA VCC = 4.0 to 5.5 V			1.5	V
			IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
			IOL = 1.0 mA VCC = 2.4 to 5.5 V			1.0	V
VOL	"L" output voltage	P30–P36	IOL = 15 mA VCC = 4.0 to 5.5 V			2.0	V
			IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
			IOL = 10 mA VCC = 2.4 to 5.5 V			1.0	V
VT+–VT–	Hysteresis	CNTR0, INT0, INT1 (Note 2) P00–P07 (Note 3)			0.4		V
VT+–VT–	Hysteresis	RXD, SCLK, SDATA (Note 2)			0.5		V
VT+–VT–	Hysteresis	$\overline{\text{RESET}}$			0.5		V
IIH	"H" input current	P00–P07, P10–P14, P20–P27, P30–P37	VI = VCC (Pin floating. Pull up transistors "off")			5.0	µA
IIH	"H" input current	$\overline{\text{RESET}}$	VI = VCC			5.0	µA
IIH	"H" input current	XIN	VI = VCC		4.0		µA
IIL	"L" input current	P00–P07, P10–P14, P20–P27, P30–P37	VI = VSS (Pin floating. Pull up transistors "off")			–5.0	µA
IIL	"L" input current	$\overline{\text{RESET}}$, CNVSS	VI = VSS			–5.0	µA
IIL	"L" input current	XIN	VI = VSS		–4.0		µA
IIL	"L" input current	P00–P07, P30–P37	VI = VSS (Pull up transistors "on")		–0.2	–0.5	mA
VRAM	RAM hold voltage		When clock stopped	2.0		5.5	V
ICC	Power source current	High-speed mode, f(XIN) = 8 MHz Output transistors "off"			5.0	8.0	mA
		High-speed mode, f(XIN) = 2 MHz, VCC = 2.4 V Output transistors "off"			0.5	1.5	mA
		Double-speed mode, f(XIN) = 4 MHz Output transistors "off"			5.0	8.0	mA
		Middle-speed mode, f(XIN) = 8 MHz, Output transistors "off"			2.0	5.0	mA
		f(XIN) = 8 MHz (in WIT state) Functions except Timer 1 and Timer 2 stop Output transistors "off"			1.6	3.2	mA
		f(XIN) = 2 MHz, VCC = 2.4 V (in WIT state) Output transistors "off"			0.2		mA
		Increment when A-D conversion is executed f(XIN) = 8 MHz, VCC = 5 V			0.5		mA
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

Notes 1: P11 is measured when the P11/TXD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".
2: RXD, SCLK, SDATA, INT0 and INT1 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake up.

(4) A-D converter characteristics (Extended operating temperature version)

Table 3.1.14 A-D Converter characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±0.9	LSB
V_{OT}	Zero transition voltage	V_{CC} = V_{REF} = 5.12 V	0	5	20	mV
		V_{CC} = V_{REF} = 3.072 V	0	3	15	mV
V_{FST}	Full scale transition voltage	V_{CC} = V_{REF} = 5.12 V	5105	5115	5125	mV
		V_{CC} = V_{REF} = 3.072 V	3060	3069	3075	mV
t_{CONV}	Conversion time				122	tc(X_{IN})
R_{LADDER}	Ladder resistor			55		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	150	200	µA
		V_{REF} = 3.0 V	30	70	120	
$I_{I(AD)}$	A-D port input current				5.0	µA

(5) Timing requirements (Extended operating temperature version)

Table 3.1.15 Timing requirements (1)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input “L” pulse width	15			µs
$t_C(X_{IN})$	External clock input cycle time	125			ns
$t_{WH}(X_{IN})$	External clock input “H” pulse width	50			ns
$t_{WL}(X_{IN})$	External clock input “L” pulse width	50			ns
$t_C(CNTR)$	$CNTR_0$ input cycle time	200			ns
$t_{WH}(CNTR)$	$CNTR_0$, INT_0, INT_1 input “H” pulse width	80			ns
$t_{WL}(CNTR)$	$CNTR_0$, INT_0, INT_1 input “L” pulse width	80			ns
$t_C(S_{CLK})$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH}(S_{CLK})$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL}(S_{CLK})$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su}(S_{CLK}–S_{DATA})$	Serial I/O2 input set up time	200			ns
$t_h(S_{CLK}–S_{DATA})$	Serial I/O2 input hold time	200			ns

Table 3.1.16 Timing requirements (2)
(V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input “L” pulse width	35			µs
$t_C(X_{IN})$	External clock input cycle time	250			ns
$t_{WH}(X_{IN})$	External clock input “H” pulse width	100			ns
$t_{WL}(X_{IN})$	External clock input “L” pulse width	100			ns
$t_C(CNTR)$	$CNTR_0$ input cycle time	500			ns
$t_{WH}(CNTR)$	$CNTR_0$, INT_0, INT_1 input “H” pulse width	230			ns
$t_{WL}(CNTR)$	$CNTR_0$, INT_0, INT_1 input “L” pulse width	230			ns
$t_C(S_{CLK})$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH}(S_{CLK})$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{WL}(S_{CLK})$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su}(S_{CLK}–S_{DATA})$	Serial I/O2 input set up time	400			ns
$t_h(S_{CLK}–S_{DATA})$	Serial I/O2 input hold time	400			ns

(6) Switching characteristics (Extended operating temperature version)

Table 3.1.17 Switching characteristics (1)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH}(SCLK)	Serial I/O2 clock output "H" pulse width	t_C(SCLK)/2–30			ns
t_{WL}(SCLK)	Serial I/O2 clock output "L" pulse width	t_C(SCLK)/2–30			ns
t_d(SCLK–SDATA)	Serial I/O2 output delay time			140	ns
t_v(SCLK–SDATA)	Serial I/O2 output valid time	0			ns
t_r(SCLK)	Serial I/O2 clock output rising time			30	ns
t_f(SCLK)	Serial I/O2 clock output falling time			30	ns
t_r(CMOS)	CMOS output rising time (Note 1)		10	30	ns
t_f(CMOS)	CMOS output falling time (Note 1)		10	30	ns

Note 1: Pin XOUT is excluded.

Table 3.1.18 Switching characteristics (2)
(V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH}(SCLK)	Serial I/O2 clock output "H" pulse width	t_C(SCLK)/2–50			ns
t_{WL}(SCLK)	Serial I/O2 clock output "L" pulse width	t_C(SCLK)/2–50			ns
t_d(SCLK–SDATA)	Serial I/O2 output delay time			350	ns
t_v(SCLK–SDATA)	Serial I/O2 output valid time	0			ns
t_r(SCLK)	Serial I/O2 clock output rising time			50	ns
t_f(SCLK)	Serial I/O2 clock output falling time			50	ns
t_r(CMOS)	CMOS output rising time (Note 1)		20	50	ns
t_f(CMOS)	CMOS output falling time (Note 1)		20	50	ns

Note 1: Pin XOUT is excluded.

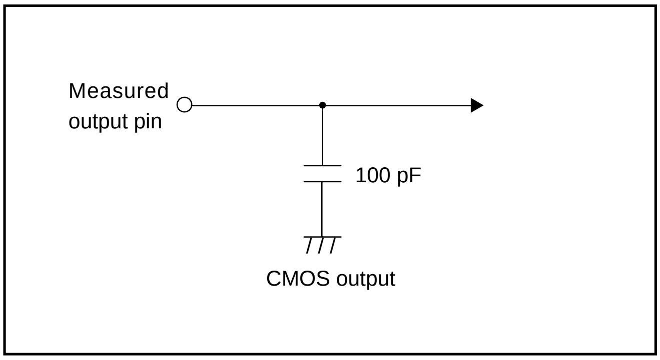


Fig. 3.1.3 Switching characteristics measurement circuit diagram (Extended operating temperature version)

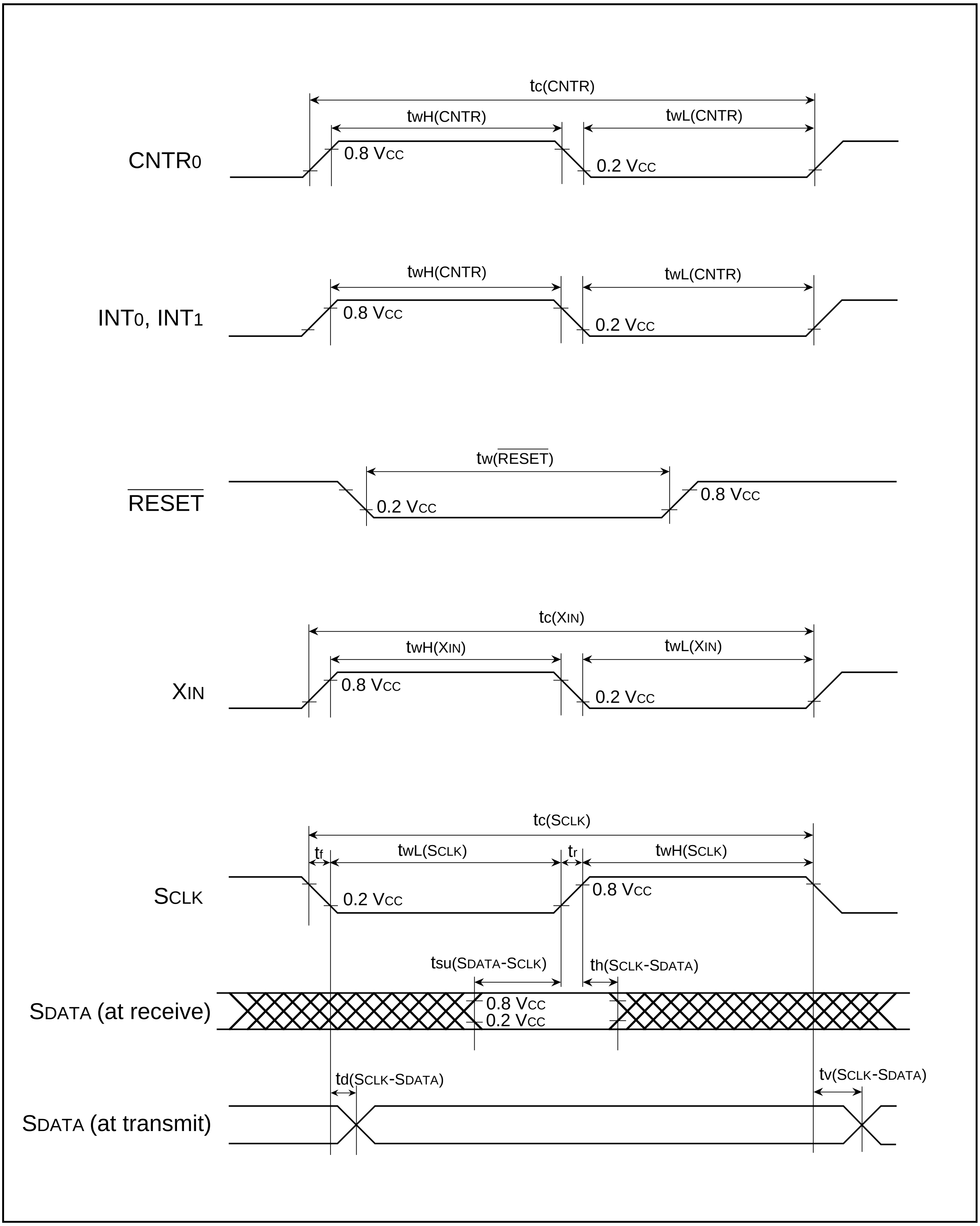


Fig. 3.1.4 Timing chart (Extended operating temperature version)

3.1 Electrical characteristics

3.1.3 7531 Group (Extended operating temperature 125 °C version)

Applied to: M37531M4V-XXXGP, M37531E4V-XXXGP

(1) Absolute maximum ratings (Extended operating temperature 125 °C version)

Table 3.1.19 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage		All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	CNV_{SS} (Note 1)		–0.3 to 13	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		Ta = 25°C	200	mW
T_{opr}	Operating temperature (Note 2)			–40 to 125	°C
T_{stg}	Storage temperature			–65 to 150	°C

Notes 1: It is a rating only for the One Time PROM version. Connect to V_{SS} for the mask ROM version.

2: The total time is limited as follows:
6000 hours at 55 to 85 °C, 1000 hours at 85 to 125 °C

(2) Recommended operating conditions (Extended operating temperature 125 °C version)

Table 3.1.20 Recommended operating conditions (1)
(V_{CC} = 2.4 to 5.5 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Typ.	Max.	Unit
V_{CC}	Power source voltage (ceramic)	$f(X_{IN})$ = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		$f(X_{IN})$ = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		$f(X_{IN})$ = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		$f(X_{IN})$ = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
	Power source voltage (CR)	$f(X_{IN})$ = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		$f(X_{IN})$ = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_7$ (Note 1)	2.0		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$, X_{IN}	$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$	0		$0.3V_{CC}$	V
V_{IL}	"L" input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_7$ (Note 1)	0		0.8	V
V_{IL}	"L" input voltage	$\overline{RESET}$, CNV_{SS}	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage	X_{IN}	0		$0.16V_{CC}$	V
$\Sigma I_{OH(peak)}$	"H" total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_7$			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 2)	$P3_0$–$P3_4$			60	mA
$\Sigma I_{OH(avg)}$	"H" total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_7$			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 2)	$P3_0$–$P3_4$			30	mA

Note 1: Vcc = 4.0 to 5.5V
2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

3.1 Electrical characteristics

Table 3.1.21 Recommended operating conditions (2)
(V_{CC} = 2.4 to 5.5 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
$I_{OH(peak)}$	“H” peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$			–10	mA
$I_{OL(peak)}$	“L” peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_7$			10	mA
$I_{OL(peak)}$	“L” peak output current (Note 1)	$P3_0$–$P3_4$			30	mA
$I_{OH(avg)}$	“H” average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$			–5	mA
$I_{OL(avg)}$	“L” average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_7$			5	mA
$I_{OL(avg)}$	“L” average output current (Note 2)	$P3_0$–$P3_4$			15	mA
$f(X_{IN})$	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V Double-speed mode			4	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V Double-speed mode			2	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50 %.

(3) Electrical characteristics (Extended operating temperature 125 °C version)

Table 3.1.22 Electrical characteristics
(V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits Min.	Typ.	Max.	Unit
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$ (Note 1)	I_{OH} = –5 mA V_{CC} = 4.0 to 5.5 V	V_{CC}–1.5			V
			I_{OH} = –1.0 mA V_{CC} = 2.4 to 5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_7$	I_{OL} = 5 mA V_{CC} = 4.0 to 5.5 V			1.5	V
			I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
			I_{OL} = 1.0 mA V_{CC} = 2.4 to 5.5 V			1.0	V
V_{OL}	"L" output voltage	$P3_0$–$P3_4$	I_{OL} = 15 mA V_{CC} = 4.0 to 5.5 V			2.0	V
			I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
			I_{OL} = 10 mA V_{CC} = 2.4 to 5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis	$CNTR_0$, INT_0, (Note 2) $P0_0$–$P0_7$ (Note 3)			0.4		V
V_{T+}–V_{T-}	Hysteresis	R_XD, S_{CLK}, S_{DATA} (Note 2)			0.5		V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$			0.5		V
I_{IH}	"H" input current	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$	V_I = V_{CC} (Pin floating. Pull up transistors "off")			5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_5$, $P3_0$–$P3_4$, $P3_7$	V_I = V_{SS} (Pin floating. Pull up transistors "off")			–5.0	µA
I_{IL}	"L" input current	$\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}		–4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P3_0$–$P3_4$, $P3_7$	V_I = V_{SS} (Pull up transistors "on")		–0.2	–0.5	mA
V_{RAM}	RAM hold voltage		When clock stopped	2.0		5.5	V
I_{CC}	Power source current		High-speed mode, f(X_{IN}) = 8 MHz Output transistors "off"		5.0	8.0	mA
			High-speed mode, f(X_{IN}) = 2 MHz, V_{CC} = 2.4 V Output transistors "off"		0.5	1.5	mA
			Double-speed mode, f(X_{IN}) = 4 MHz Output transistors "off"		5.0	8.0	mA
			Middle-speed mode, f(X_{IN}) = 8 MHz, Output transistors "off"		2.0	5.0	mA
			f(X_{IN}) = 8 MHz (in WIT state) Functions except Timer 1 and Timer 2 stop Output transistors "off"		1.6	3.2	mA
			f(X_{IN}) = 2 MHz, V_{CC} = 2.4 V (in WIT state) Output transistors "off"		0.2		mA
			Increment when A-D conversion is executed f(X_{IN}) = 8 MHz, V_{CC} = 5 V		0.5		mA
			All oscillation stopped (in STP state) Output transistors "off" — Ta = 25 °C		0.1	1.0	µA
			All oscillation stopped (in STP state) Output transistors "off" — Ta = 125 °C			50	µA

Notes 1: $P1_1$ is measured when the $P1_1$/T_XD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: R_XD, S_{CLK}, S_{DATA}, and INT_0 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake up.

(4) A-D converter characteristics (Extended operating temperature 125 °C version)

Table 3.1.23 A-D Converter characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±0.9	LSB
V_{OT}	Zero transition voltage	V_{CC} = V_{REF} = 5.12 V	0	5	20	mV
		V_{CC} = V_{REF} = 3.072 V	0	3	15	mV
V_{FST}	Full scale transition voltage	V_{CC} = V_{REF} = 5.12 V	5105	5115	5125	mV
		V_{CC} = V_{REF} = 3.072 V	3060	3069	3075	mV
t_{CONV}	Conversion time				122	tc(X_{IN})
R_{LADDER}	Ladder resistor			55		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	150	200	µA
		V_{REF} = 3.0 V	30	70	120	
$I_{I(AD)}$	A-D port input current				5.0	µA

(5) Timing requirements (Extended operating temperature 125 °C version)

Table 3.1.24 Timing requirements (1)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input "L" pulse width	15			µs
$t_C(X_{IN})$	External clock input cycle time	125			ns
$t_{WH}(X_{IN})$	External clock input "H" pulse width	50			ns
$t_{WL}(X_{IN})$	External clock input "L" pulse width	50			ns
$t_C(CNTR)$	$CNTR_0$ input cycle time	200			ns
$t_{WH}(CNTR)$	$CNTR_0$, INT_0 input "H" pulse width	80			ns
$t_{WL}(CNTR)$	$CNTR_0$, INT_0 input "L" pulse width	80			ns
$t_C(S_{CLK})$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH}(S_{CLK})$	Serial I/O2 clock input "H" pulse width	400			ns
$t_{WL}(S_{CLK})$	Serial I/O2 clock input "L" pulse width	400			ns
$t_{su}(S_{CLK}–S_{DATA})$	Serial I/O2 input set up time	200			ns
$t_h(S_{CLK}–S_{DATA})$	Serial I/O2 input hold time	200			ns

Table 3.1.25 Timing requirements (2)
(V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input "L" pulse width	35			µs
$t_C(X_{IN})$	External clock input cycle time	250			ns
$t_{WH}(X_{IN})$	External clock input "H" pulse width	100			ns
$t_{WL}(X_{IN})$	External clock input "L" pulse width	100			ns
$t_C(CNTR)$	$CNTR_0$ input cycle time	500			ns
$t_{WH}(CNTR)$	$CNTR_0$, INT_0, input "H" pulse width	230			ns
$t_{WL}(CNTR)$	$CNTR_0$, INT_0, input "L" pulse width	230			ns
$t_C(S_{CLK})$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH}(S_{CLK})$	Serial I/O2 clock input "H" pulse width	950			ns
$t_{WL}(S_{CLK})$	Serial I/O2 clock input "L" pulse width	950			ns
$t_{su}(S_{CLK}–S_{DATA})$	Serial I/O2 input set up time	400			ns
$t_h(S_{CLK}–S_{DATA})$	Serial I/O2 input hold time	400			ns

(6) Switching characteristics (Extended operating temperature 125 °C version)

Table 3.1.26 Switching characteristics (1)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK})$	Serial I/O2 clock output "H" pulse width	$t_C(S_{CLK})/2–50$			ns
$t_{WL}(S_{CLK})$	Serial I/O2 clock output "L" pulse width	$t_C(S_{CLK})/2–50$			ns
$t_d(S_{CLK}–S_{DATA})$	Serial I/O2 output delay time			200	ns
$t_v(S_{CLK}–S_{DATA})$	Serial I/O2 output valid time	0			ns
$t_r(S_{CLK})$	Serial I/O2 clock output rising time			50	ns
$t_f(S_{CLK})$	Serial I/O2 clock output falling time			50	ns
$t_r(CMOS)$	CMOS output rising time (Note 1)		10	50	ns
$t_f(CMOS)$	CMOS output falling time (Note 1)		10	50	ns

Note 1: Pin X_{OUT} is excluded.

Table 3.1.27 Switching characteristics (2)
(V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 125 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK})$	Serial I/O2 clock output "H" pulse width	$t_C(S_{CLK})/2–80$			ns
$t_{WL}(S_{CLK})$	Serial I/O2 clock output "L" pulse width	$t_C(S_{CLK})/2–80$			ns
$t_d(S_{CLK}–S_{DATA})$	Serial I/O2 output delay time			400	ns
$t_v(S_{CLK}–S_{DATA})$	Serial I/O2 output valid time	0			ns
$t_r(S_{CLK})$	Serial I/O2 clock output rising time			80	ns
$t_f(S_{CLK})$	Serial I/O2 clock output falling time			80	ns
$t_r(CMOS)$	CMOS output rising time (Note 1)		20	80	ns
$t_f(CMOS)$	CMOS output falling time (Note 1)		20	80	ns

Note 1: Pin X_{OUT} is excluded.

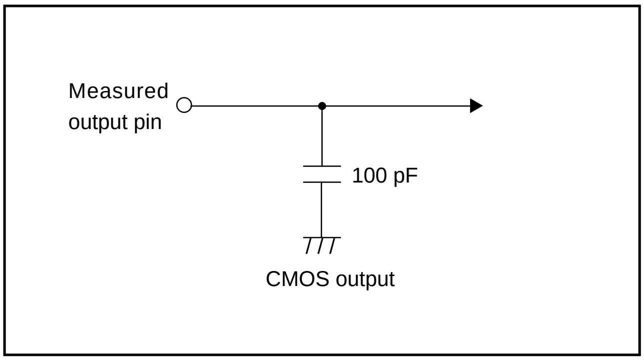


Fig. 3.1.5 Switching characteristics measurement circuit diagram (Extended operating temperature 125 °C version)

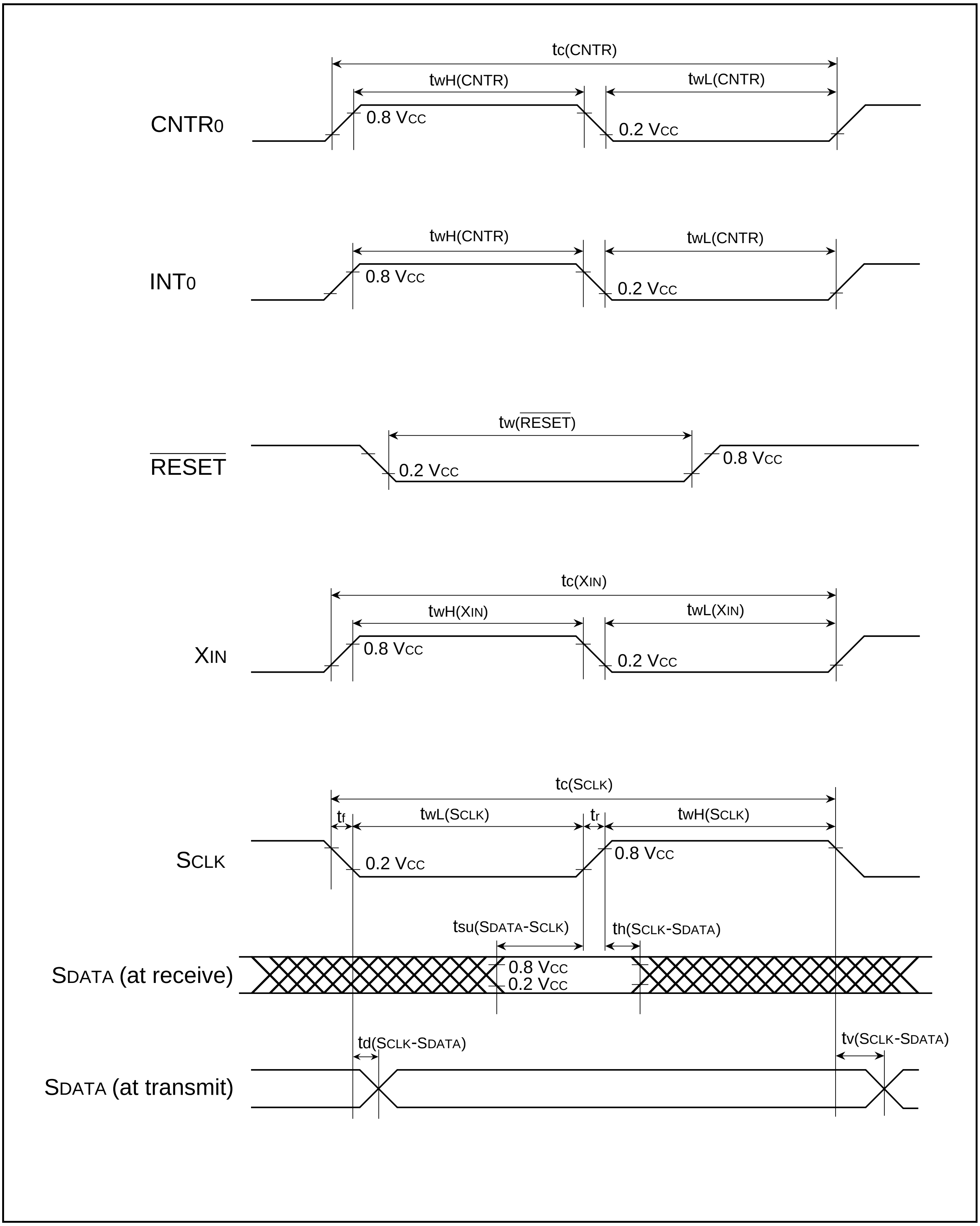


Fig. 3.1.6 Timing chart (Extended operating temperature 125 °C version)

3.2 Typical characteristics

3.2.1 Power source current characteristic example (I_{CC}-V_{CC} characteristic)

Measurement condition: Typical sample, Ta = 25 °C, ceramic oscillation, when operating system in double-speed mode (A-D conversion not executed)

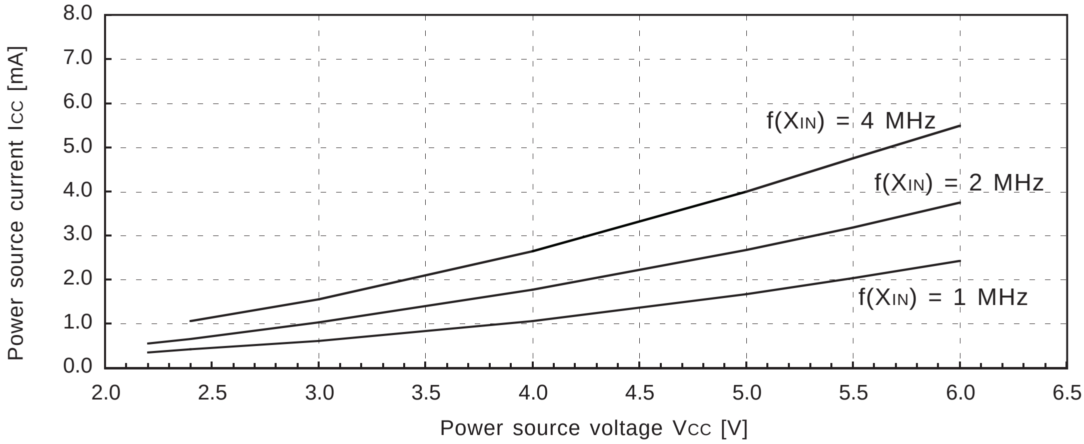


Fig. 3.2.1 I_{CC}-V_{CC} characteristic example (in double-speed mode)

Measurement condition: Typical sample, Ta = 25 °C, ceramic oscillation, when operating system in high-speed mode (A-D conversion not executed)

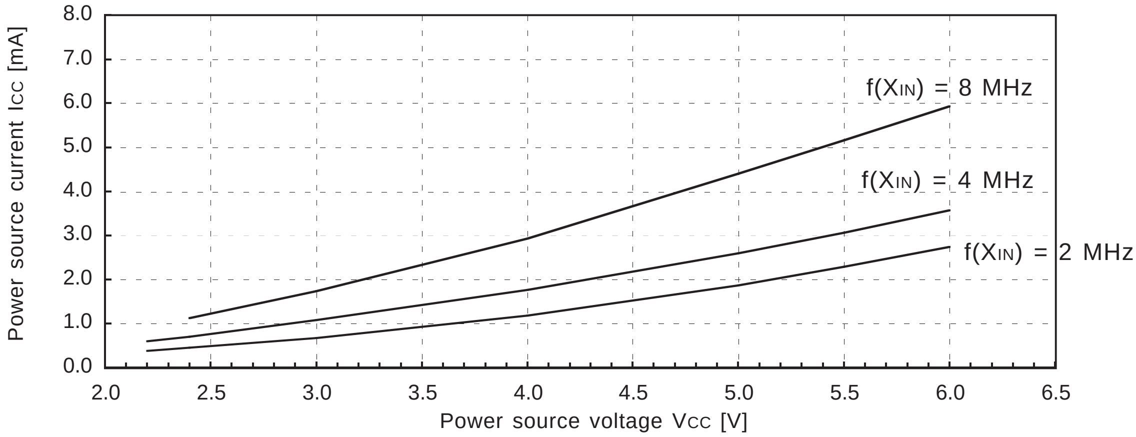


Fig. 3.2.2 I_{CC}-V_{CC} characteristic example (in high-speed mode)

Measurement condition: Typical sample, Ta = 25 °C, ceramic oscillation, when operating system in middle-speed mode (A-D conversion not executed)

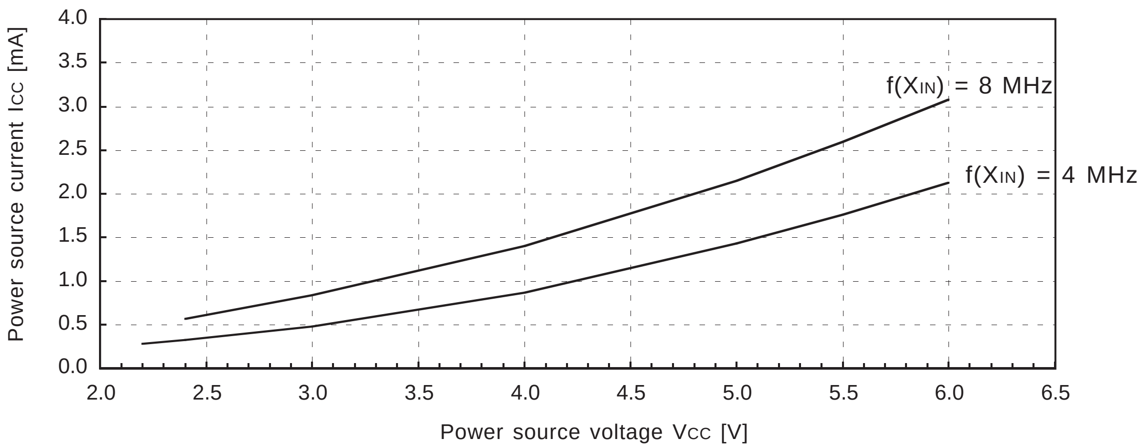


Fig. 3.2.3 I_{CC}-V_{CC} characteristic example (in middle-speed mode)

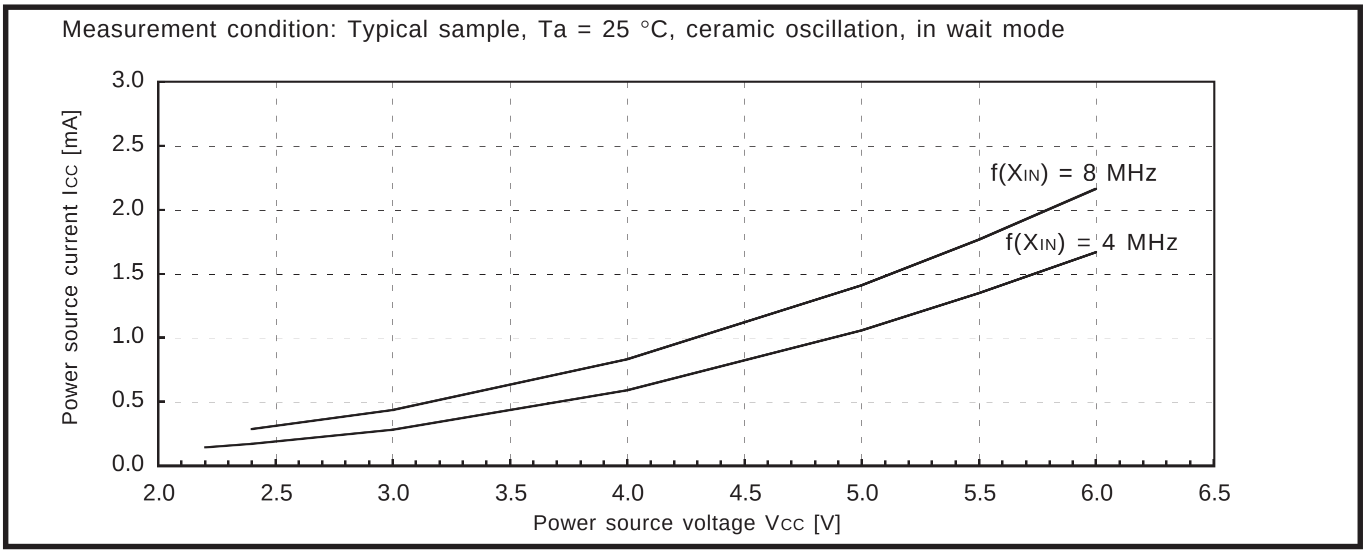


Fig. 3.2.4 ICC-VCC characteristic example (in wait mode)

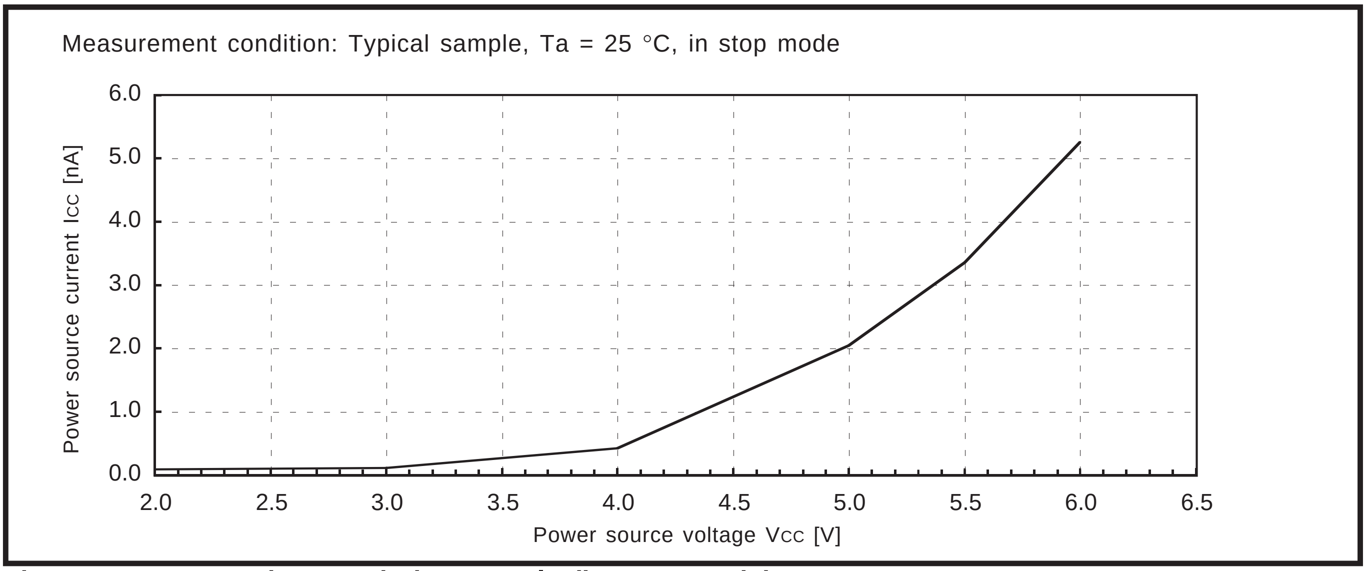


Fig. 3.2.5 ICC-VCC characteristic example (in stop mode)

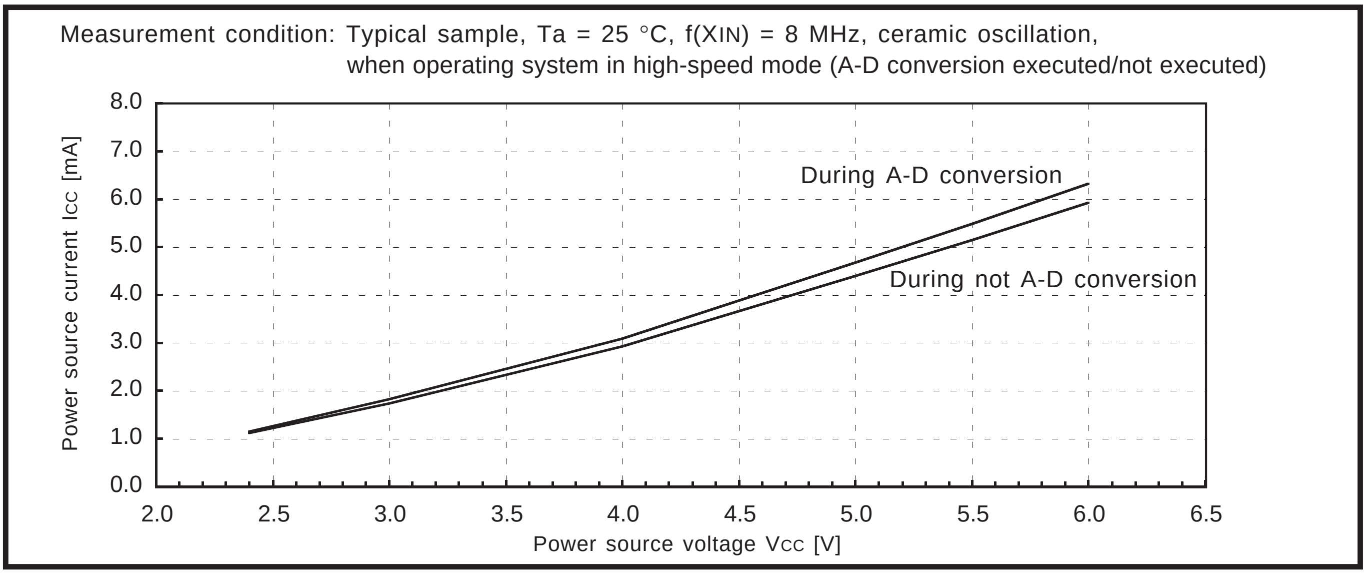


Fig. 3.2.6 ICC-VCC characteristic example (addition when operating A-D conversion, A-D conversion executed/not executed, f(XIN) = 8MHz, in high-speed mode)

3.2.2 Power source current frequency characteristic example (ICC-f(XIN) characteristic)

Measurement condition: Typical sample, Ta = 25 °C, ceramic oscillation, when operating system in double-speed mode (A-D conversion not executed)

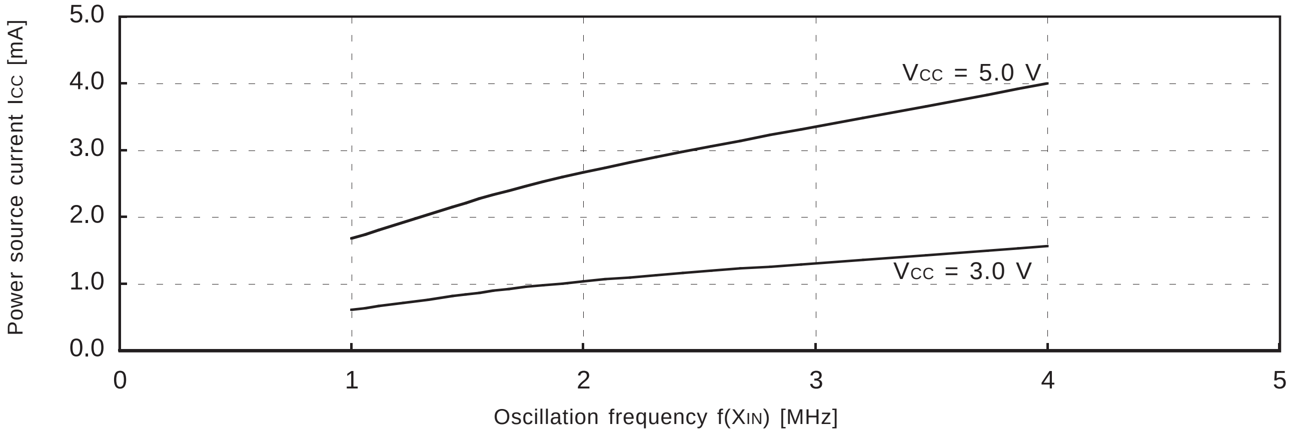


Fig. 3.2.7 ICC-f(XIN) characteristic example (in double-speed mode)

Measurement condition: Typical sample, Ta = 25 °C, ceramic oscillation, when operating system in high-speed mode (A-D conversion not executed)

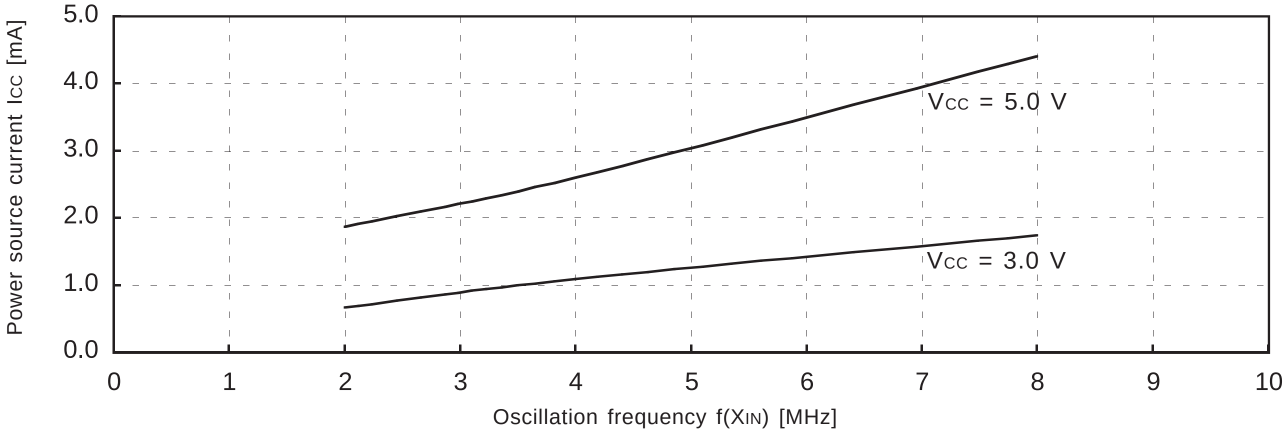


Fig. 3.2.8 ICC-f(XIN) characteristic example (in high-speed mode)

Measurement condition: Typical sample, Ta = 25 °C, ceramic oscillation, when operating system in middle-speed mode (A-D conversion not executed)

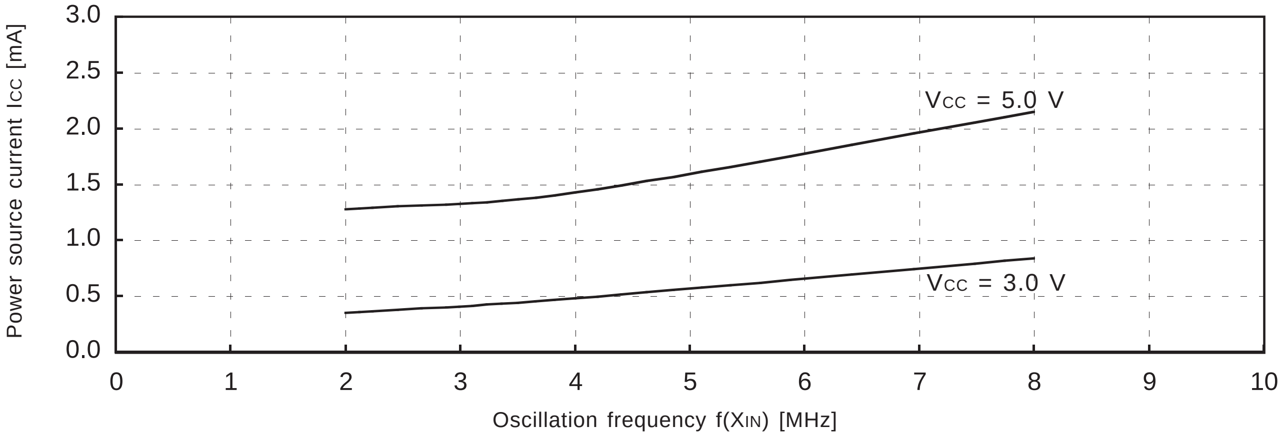


Fig. 3.2.9 ICC-f(XIN) characteristic example (in middle-speed mode)

Measurement condition: Typical sample, Ta = 25 °C, ceramic oscillation, in wait mode

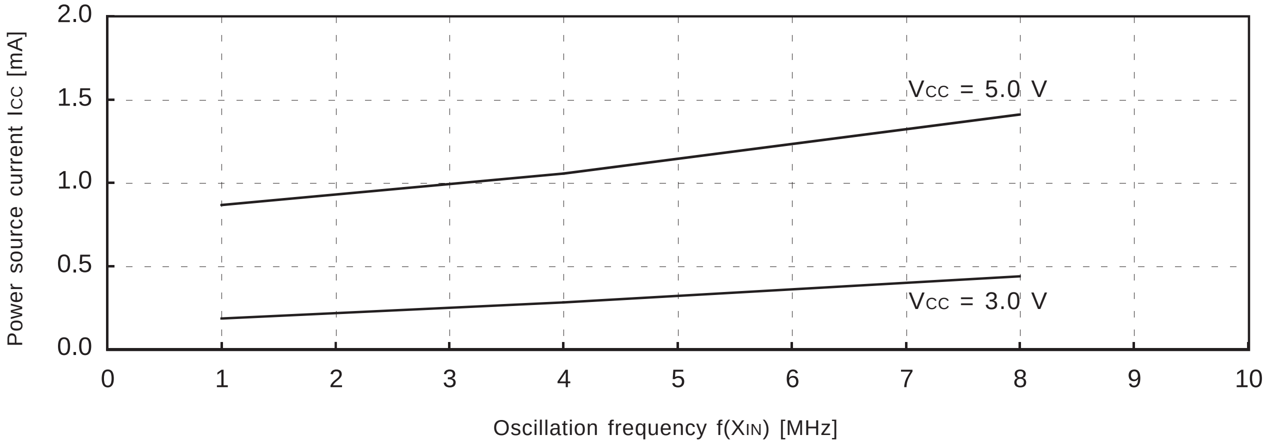


Fig. 3.2.10 ICC-f(XIN) characteristic example (in wait mode)

3.2.3 Port typical characteristic example

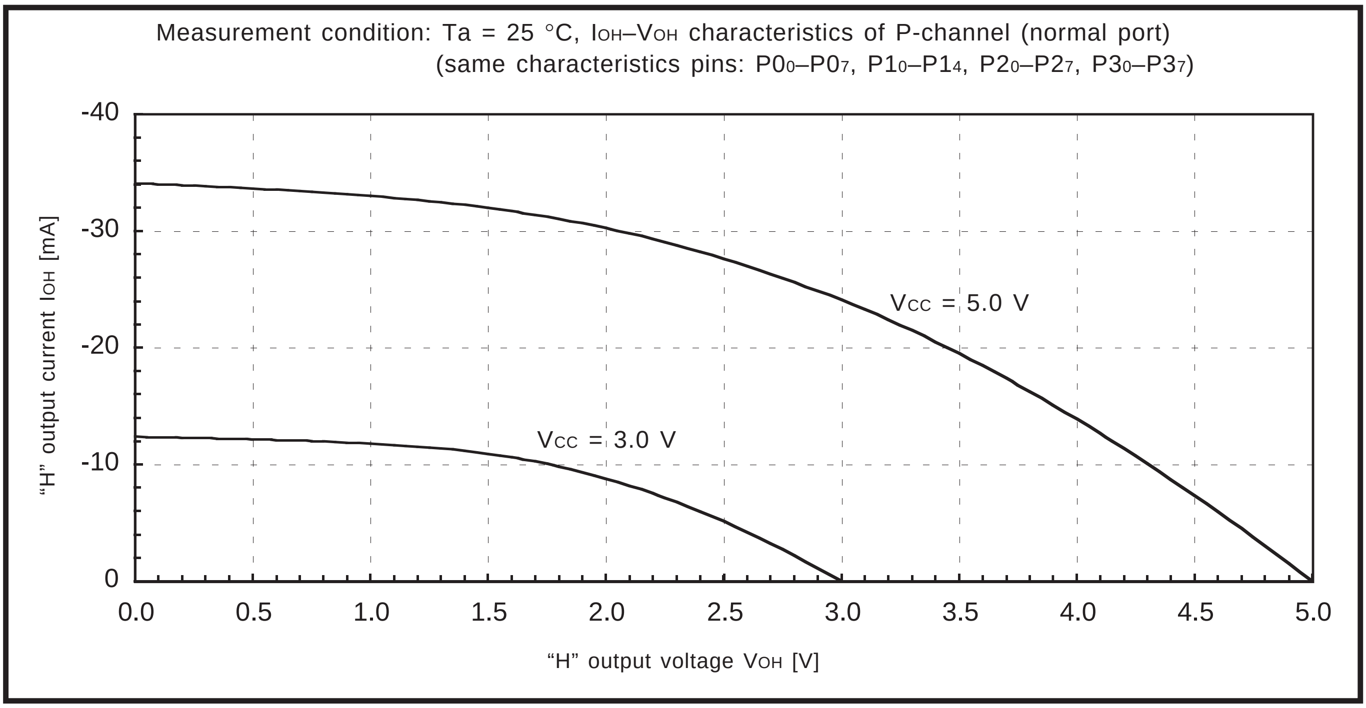


Fig. 3.2.11 VOH-IOH characteristic example of P-channel (Ta = 25 °C): normal port

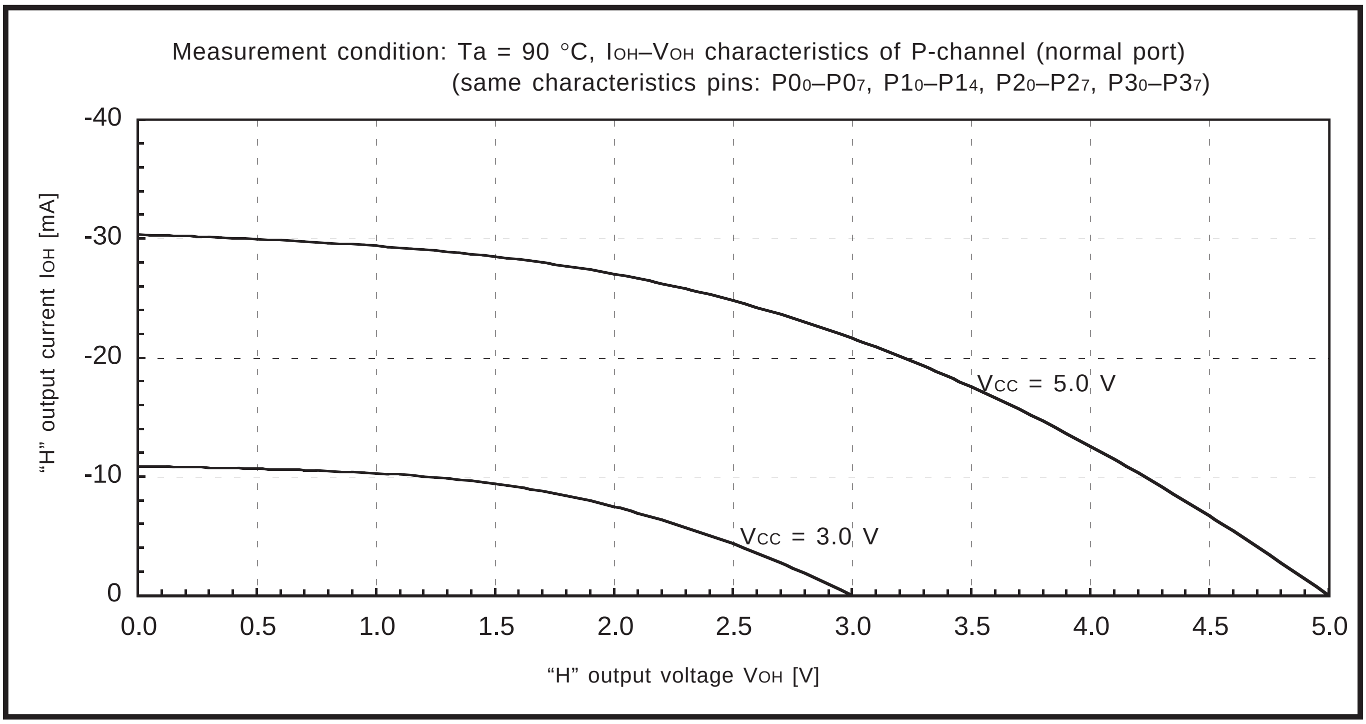


Fig. 3.2.12 VOH-IOH characteristic example of P-channel (Ta = 90 °C): normal port

Measurement condition: Ta = 25 °C, V_{OL}–I_{OL} characteristics of N-channel (normal port)
(same characteristics pins: $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$)

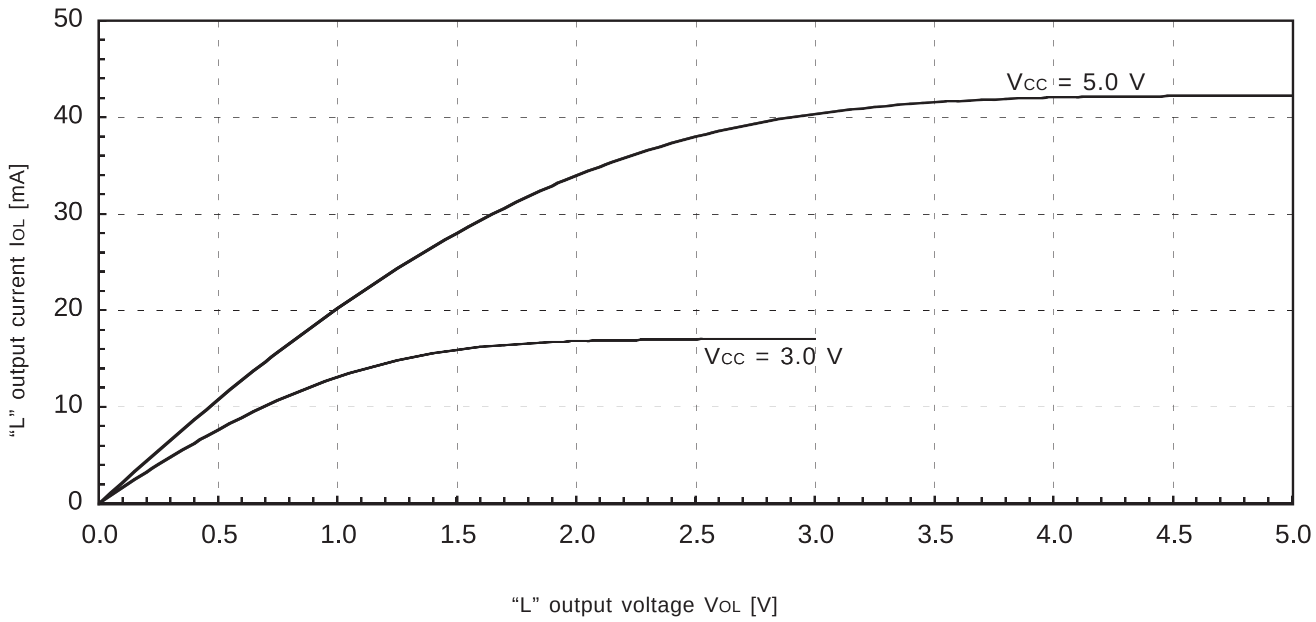


Fig. 3.2.13 V_{OL}-I_{OL} characteristic example of N-channel (Ta = 25 °C): normal port

Measurement condition: Ta = 90 °C, V_{OL}–I_{OL} characteristics of N-channel (normal port)
(same characteristics pins: $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$)

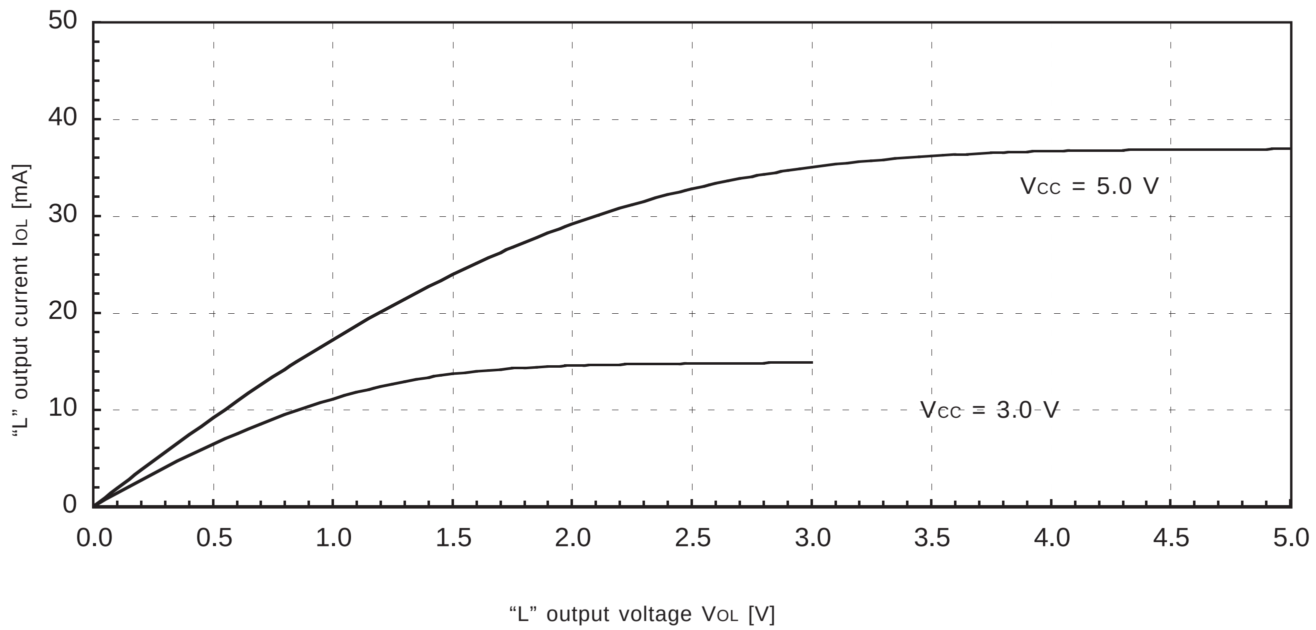


Fig. 3.2.14 V_{OL}-I_{OL} characteristic example of N-channel (Ta = 90 °C): normal port

3.2 Typical characteristics

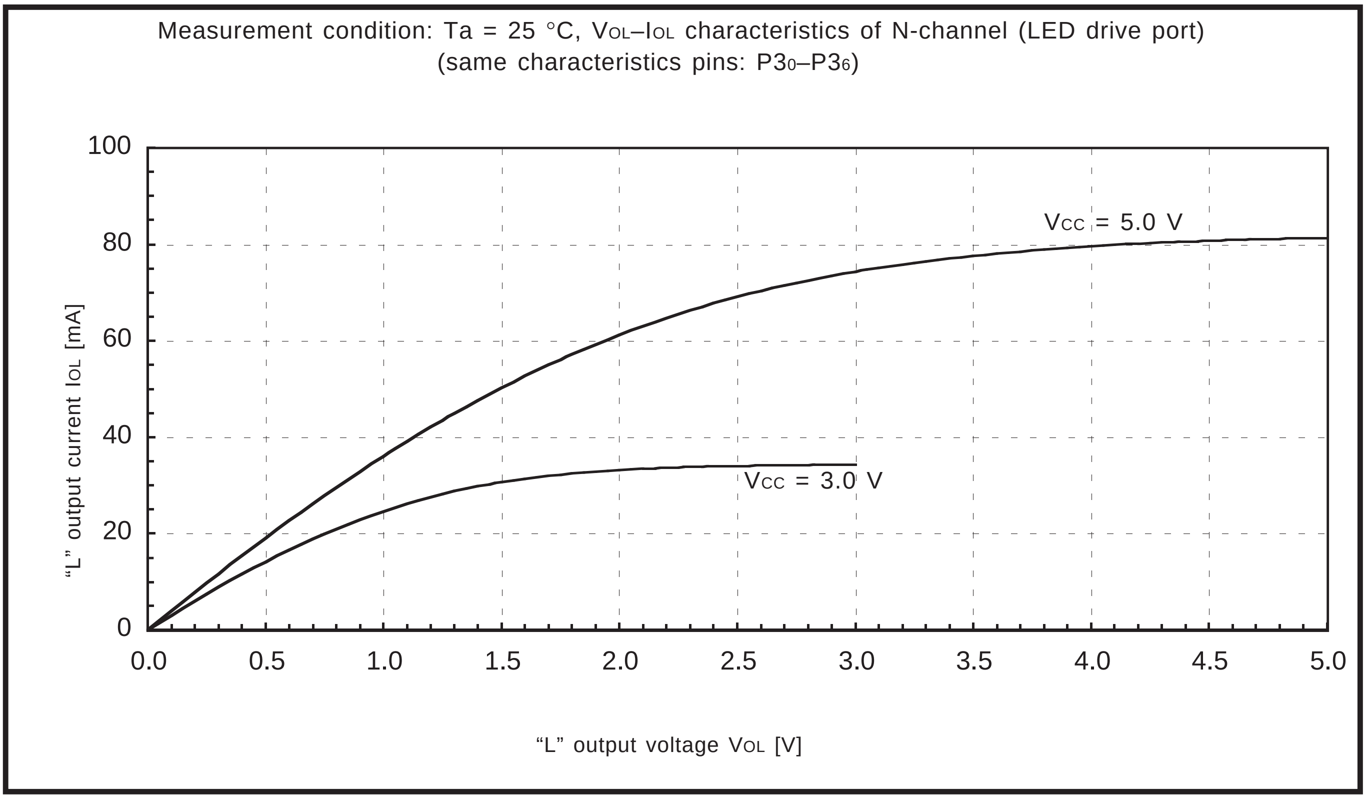


Fig. 3.2.15 VOL-IOL characteristic example of N-channel (Ta = 25 °C): LED drive port

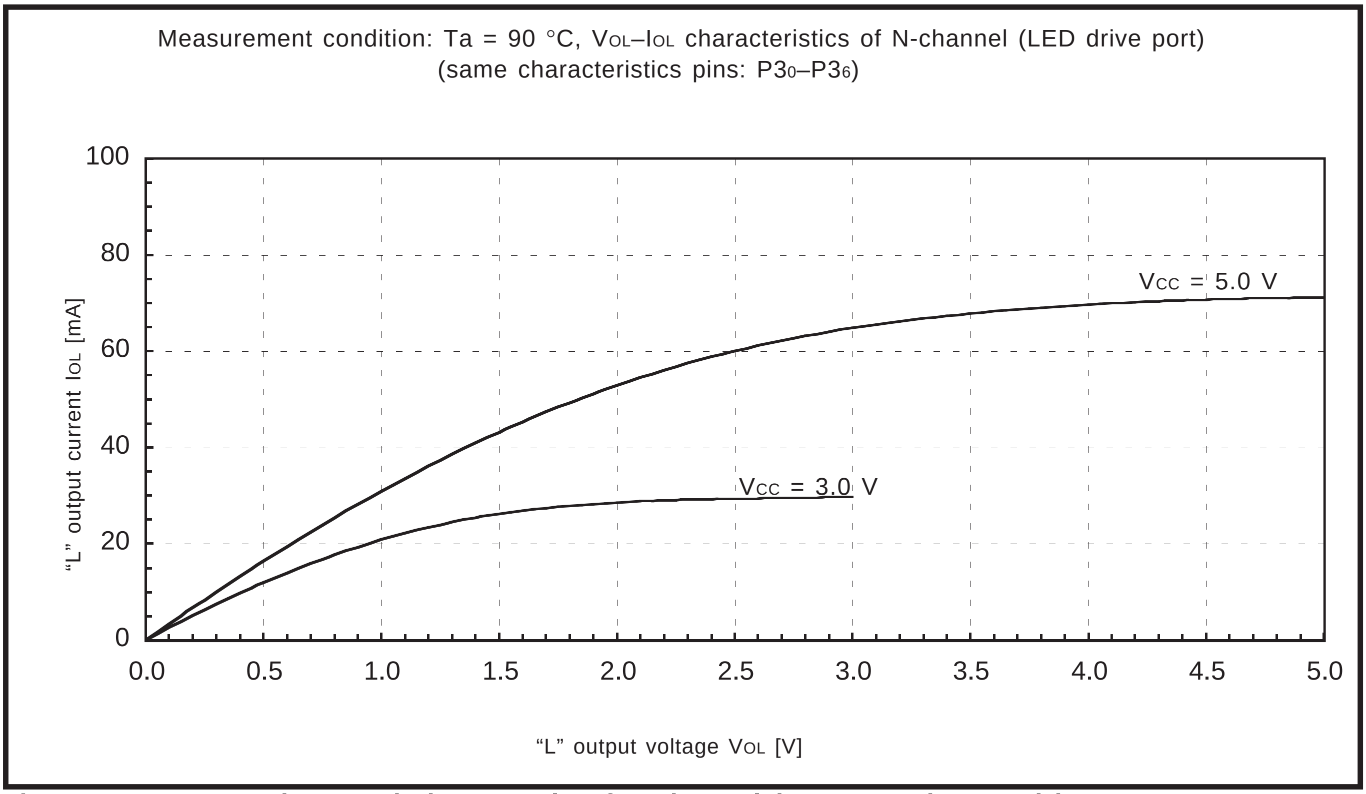


Fig. 3.2.16 VOL-IOL characteristic example of N-channel (Ta = 90 °C): LED drive port

Measurement condition: Typical sample, pull-up transistor connected
(same characteristics pins: $P0_0$–$P0_7$, $P3_0$–$P3_7$)

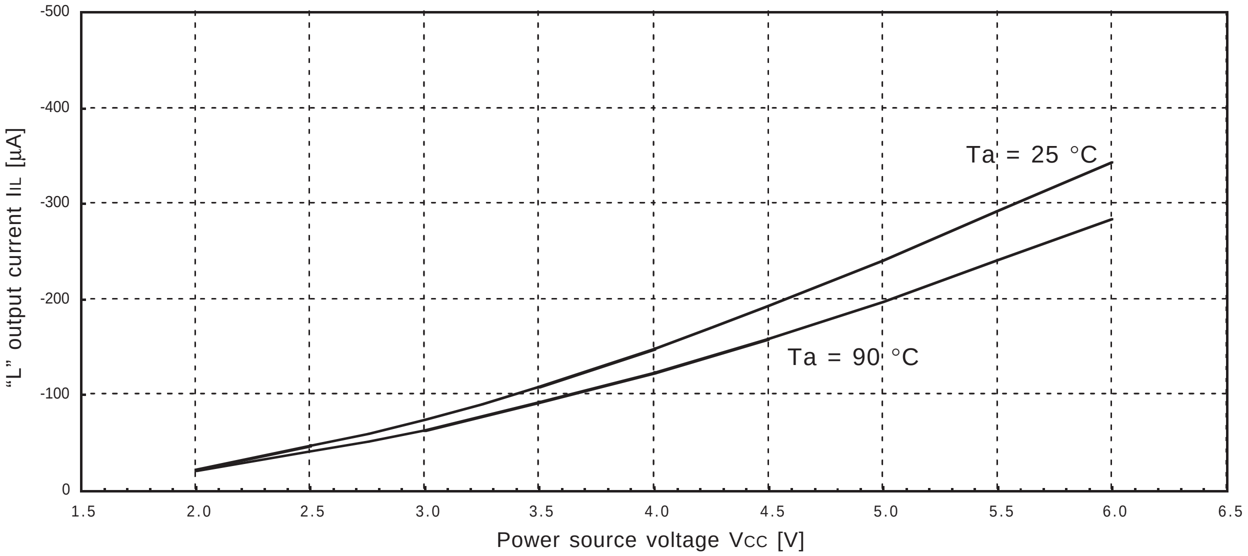


Fig. 3.2.17 "L" input current when connecting pull-up transistor

3.2.4 RC oscillation characteristic example

Measurement condition: Ta = 25 °C, Typical sample, C = 33 pF

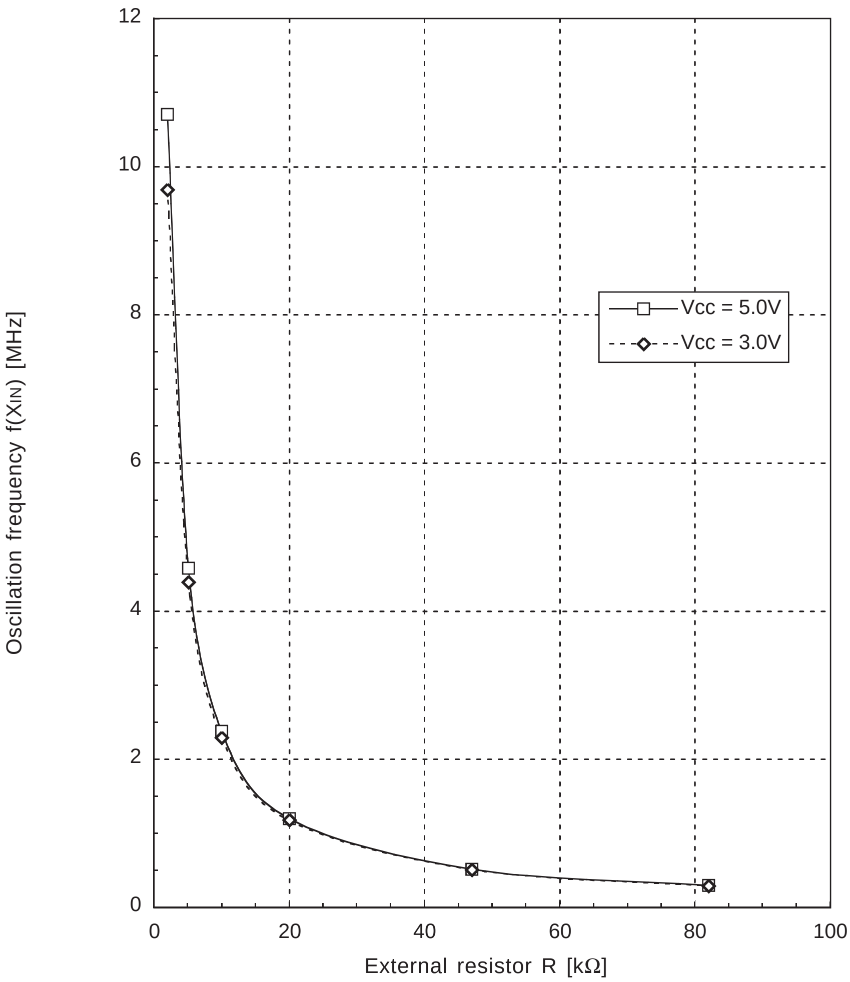


Fig. 3.2.18 RC oscillation characteristic example

3.2.5 A-D conversion typical characteristic example

(1) Definition of A-D conversion accuracy

The A-D conversion accuracy is defined below (refer to Fig. 3.2.14).

●Relative accuracy

① Zero transition voltage (V_{OT})

This means an analog input voltage when the actual A-D conversion output data changes from "0" to "1."

② Full-scale transition voltage (V_{FST})

This means an analog input voltage when the actual A-D conversion output data changes from "1023" to "1022."

③ Linearity error

This means a deviation from the line between V_{OT} and V_{FST} of a converted value between V_{OT} and V_{FST}.

④ Differential non-linearity error

This means a deviation from the input potential difference required to change a converted value between V_{OT} and V_{FST} by 1 LSB of the 1 LSB at the relative accuracy.

●Absolute accuracy

This means a deviation from the ideal characteristics between 0 to V_{REF} of actual A-D conversion characteristics.

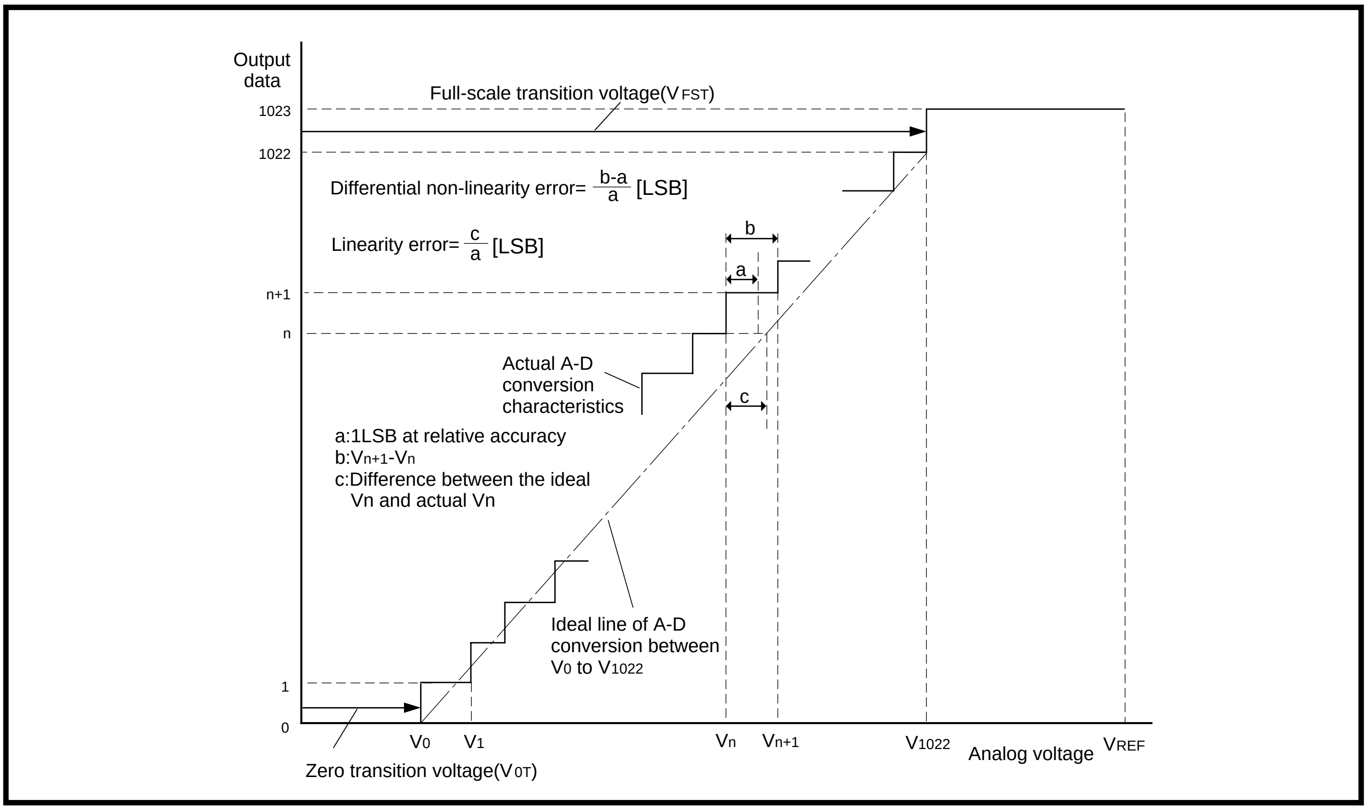


Fig. 3.2.19 Definition of A-D conversion accuracy

Vn: Analog input voltage when the output data changes from "n" to "n + 1" (n = 0 to 1022)

• 1 LSB at relative accuracy → $\dfrac{V_{FST} - V_{OT}}{1022}$ (V)

• 1 LSB at absolute accuracy → $\dfrac{V_{REF}}{1024}$ (V)

(2) A-D conversion accuracy characteristic example-1

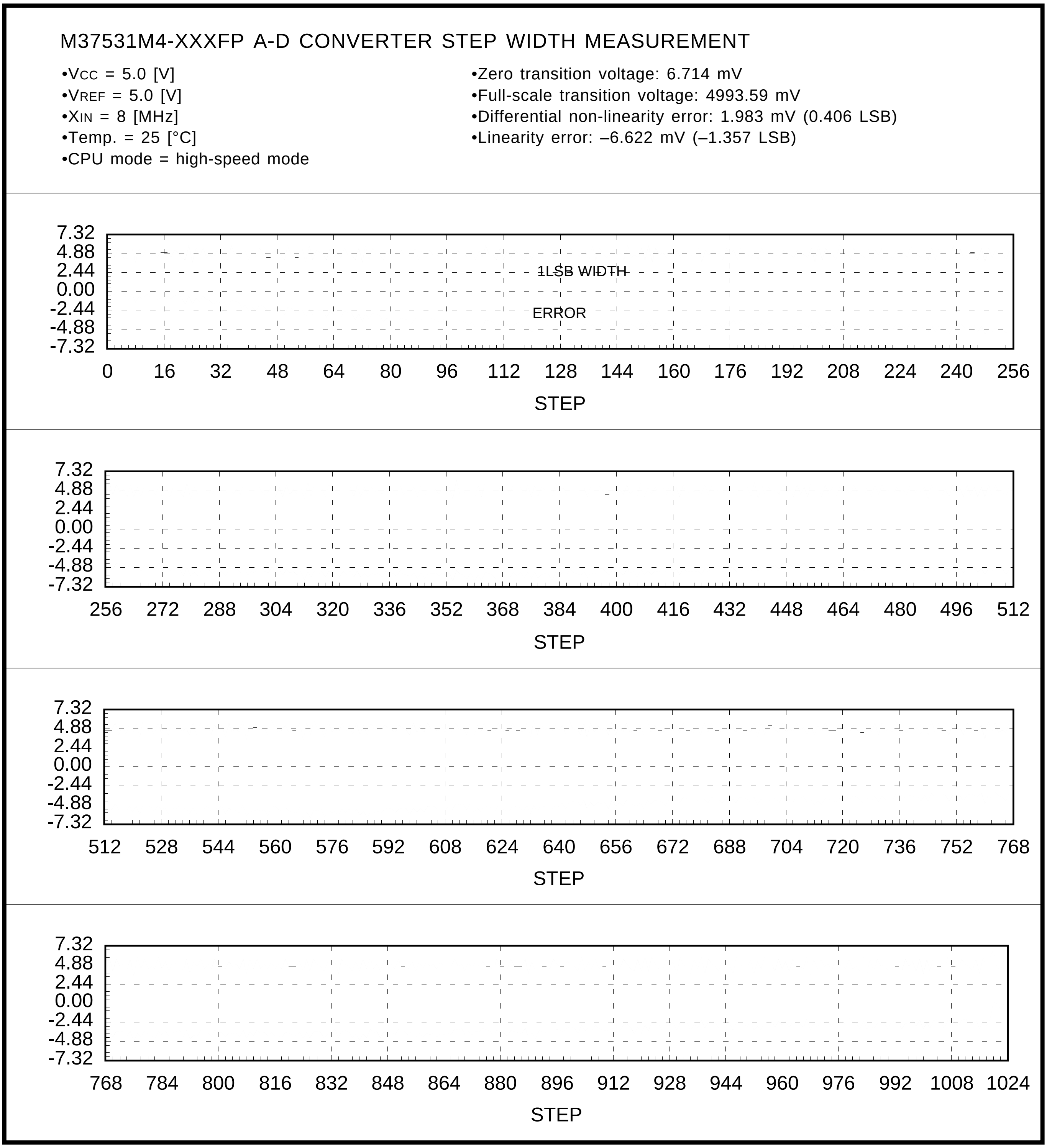


Fig. 3.2.20 A-D conversion accuracy typical characteristic example-1

(3) A-D conversion accuracy characteristic example-2

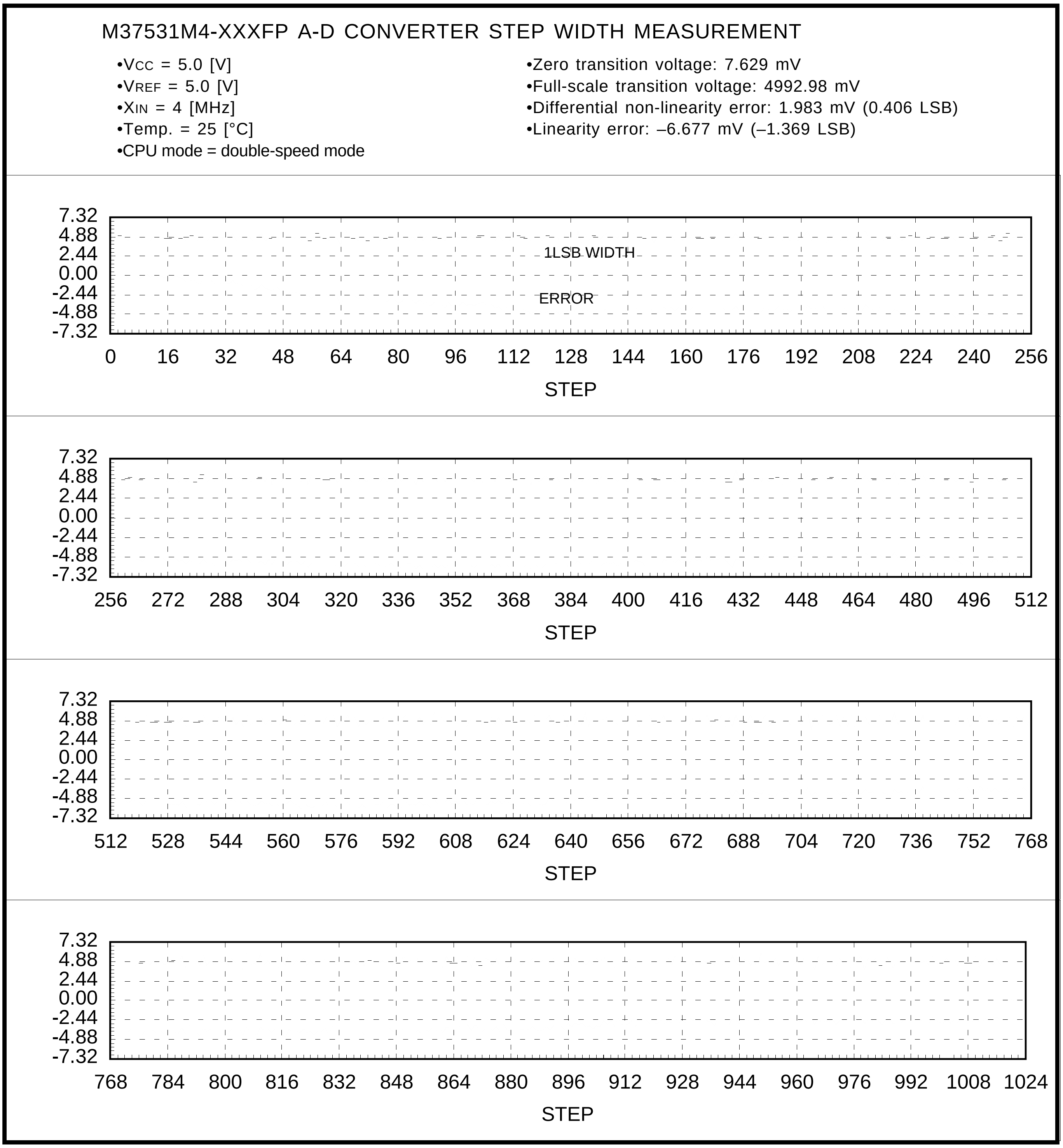


Fig. 3.2.21 A-D conversion accuracy typical characteristic example-2

3.3 Notes on use

3.3.1 Notes on interrupts

(1) Setting of interrupt request bit and interrupt enable bit

To set an interrupt request bit and an interrupt enable bit for interrupts, execute as the following sequence :
① Clear an interrupt request bit to “0” (no interrupt request issued).
② Set an interrupt enable bit to “1” (interrupts enabled).

● **Reason**

If the above setting ①, ② are performed simultaneously with one instruction, an unnecessary interrupt processing routine is executed. Because an interrupt enable bit is set to “1” (interrupts enabled) before an interrupt request bit is cleared to “0”.

(2) Switching external interrupt detection edge

For the products able to switch the external interrupt detection edge, switch it as the following sequence.

Clear an interrupt enable bit to “0” (interrupt disabled)
↓
Switch the detection edge
↓
Clear an interrupt request bit to “0”
(no interrupt request issued)
↓
Set the interrupt enable bit to “1” (interrupt enabled)

Fig. 3.3.1 Sequence of switch the detection edge

● **Reason**

The interrupt circuit recognizes the switching of the detection edge as the change of external input signals. This may cause an unnecessary interrupt.

(3) Check of interrupt request bit

When executing the **BBC** or **BBS** instruction to an interrupt request bit of an interrupt request register immediately after this bit is set to “0” by using a data transfer instruction, execute one or more instructions before executing the **BBC** or **BBS** instruction.

Clear the interrupt request bit to “0” (no interrupt issued)
↓
NOP (one or more instructions)
↓
Execute the **BBC** or **BBS** instruction

Data transfer instruction:
LDM, LDA, STA, STX, and STY instructions

Fig. 3.3.2 Sequence of check of interrupt request bit

● **Reason**

If the **BBC** or **BBS** instruction is executed immediately after an interrupt request bit of an interrupt request register is cleared to “0”, the value of the interrupt request bit before being cleared to “0” is read.

(4) Structure of interrupt control register 1

Fix the bit 7 of the interrupt control register 1 to “0”. Figure 3.3.3 shows the structure of the interrupt control register 1.

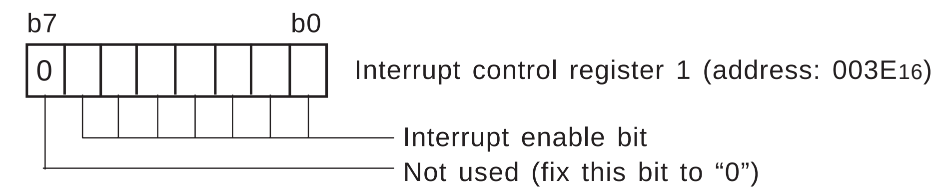
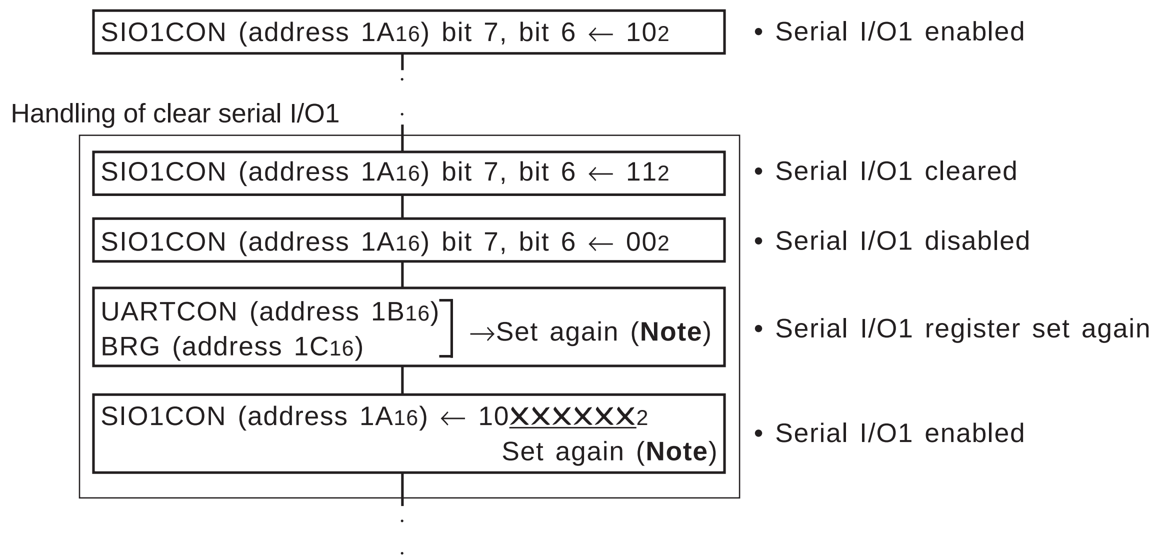


Fig. 3.3.3 Structure of interrupt control register 1

3.3.2 Notes on serial I/O

(1) Handling of serial I/O1 clear

When serial I/O1 is set again or the transmit/receive operation is stopped/restarted while serial I/O1 is operating, clear the serial I/O1 as shown in Figure 3.3.4.



Note: When the contents of register is not changed, setting again is not necessary.

Fig. 3.3.4 Sequence of clearing serial I/O

(2) Data transmission control with referring to transmit shift register completion flag

The transmit shift register completion flag changes from “1” to “0” with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

(3) Writing transmit data

When an external clock is used as the synchronous clock for the clock synchronous serial I/O, write the transmit data to the transmit buffer register (serial I/O shift register) at “H” of the transfer clock input level.

(4) Serial I/O2 transmit/receive shift completion flag

- The transmit/receive shift completion flag of the serial I/O2 control register is set to "1" after completing transmit/receive shift. In order to set this flag to "0", write data (dummy data at reception) to the serial I/O2 register by program.
- Bit 7 of the serial I/O2 control register is set to "1" a half cycle (of the shift clock) earlier than completion of shift operation. Accordingly, when using this bit to confirm shift completion, a half cycle or more of the shift clock must pass after confirming that this bit is set to "1", before performing read/write to the serial I/O2 register.

3.3.3 Notes on A-D converter

(1) Analog input pin

Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01μF to 1μF. Further, be sure to verify the operation of application products on the user side.

● **Reason**

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A-D conversion precision to be worse.

(2) Clock frequency during A-D conversion

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. Thus, make sure the following during an A-D conversion.

- f(X_{IN}) is 500 kHz or more
- Do not execute the **STP** instruction

3.3.4 Notes on $\overline{\text{RESET}}$ pin

(1) Connecting capacitor

In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and the V_{SS} pin. And use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following :

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

● **Reason**

If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

3.3.5 Notes on input and output pins

(1) Notes in stand-by state

In stand-by state*[1] for low-power dissipation, do not make input levels of an input port and an I/O port “undefined”.
Pull-up (connect the port to V_{CC}) or pull-down (connect the port to V_{SS}) these ports through a resistor.
When determining a resistance value, note the following points:
• External circuit
• Variation of output levels during the ordinary operation

When using built-in pull-up or pull-down resistor, note on varied current values:
• When setting as an input port : Fix its input level
• When setting as an output port : Prevent current from flowing out to external

● **Reason**

The output transistor becomes the OFF state, which causes the ports to be the high-impedance state. Note that the level becomes “undefined” depending on external circuits.
Accordingly, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of a input port and an I/O port are “undefined”. This may cause power source current.

*[1] stand-by state : the stop mode by executing the **STP** instruction
the wait mode by executing the **WIT** instruction

(2) Modifying output data with bit managing instruction

When the port latch of an I/O port is modified with the bit managing instruction*[2], the value of the unspecified bit may be changed.

● **Reason**

The bit managing instructions are read-modify-write form instructions for reading and writing data by a byte unit. Accordingly, when these instructions are executed on a bit of the port latch of an I/O port, the following is executed to all bits of the port latch.
• As for a bit which is set for an input port :
The pin state is read in the CPU, and is written to this bit after bit managing.
• As for a bit which is set for an output port :
The bit value of the port latch is read in the CPU, and is written to this bit after bit managing.

Note the following :
• Even when a port which is set as an output port is changed for an input port, its port latch holds the output data.
• As for a bit of the port latch which is set for an input port, its value may be changed even when not specified with a bit managing instruction in case where the pin state differs from its port latch contents.

*[2] bit managing instructions : **SEB**, and **CLB** instructions

3.3.6 Notes on programming

(1) Processor status register

① **Initializing of processor status register**
Flags which affect program execution must be initialized after a reset.
In particular, it is essential to initialize the T and D flags because they have an important effect on calculations.

● **Reason**
After a reset, the contents of the processor status register (PS) are undefined except for the I flag which is “1”.

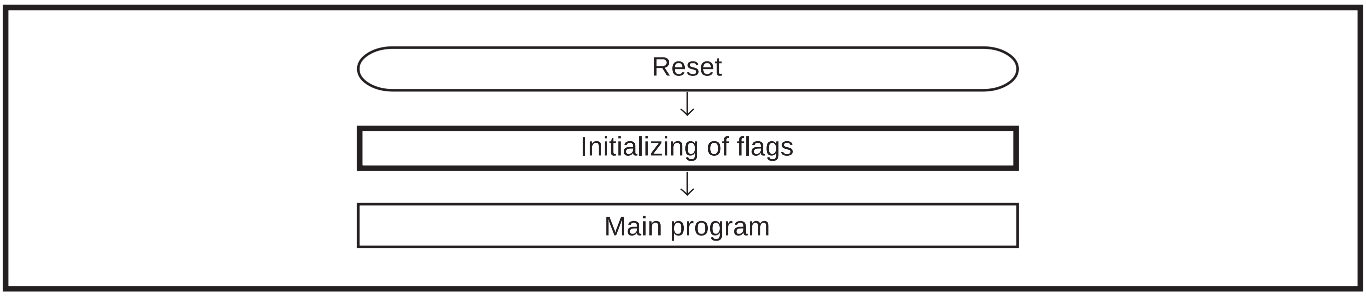


Fig. 3.3.5 Initialization of processor status register

② **How to reference the processor status register**
To reference the contents of the processor status register (PS), execute the **PHP** instruction once then read the contents of (S+1). If necessary, execute the **PLP** instruction to return the PS to its original status.
A **NOP** instruction should be executed after every **PLP** instruction.

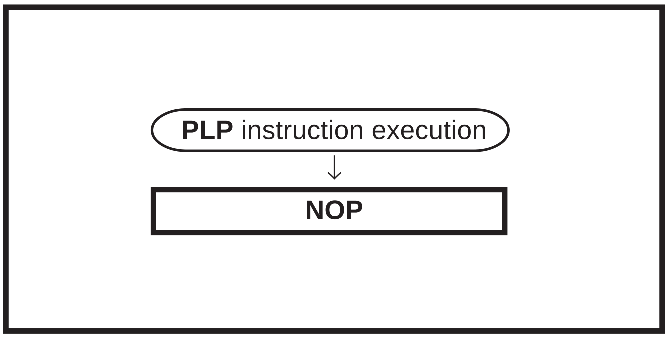


Fig. 3.3.6 Sequence of PLP instruction execution

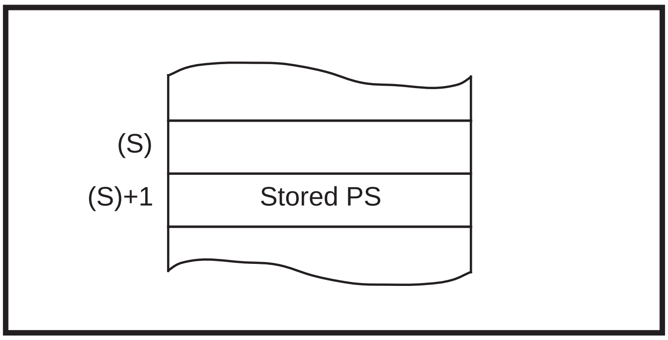


Fig. 3.3.7 Stack memory contents after PHP instruction execution

(2) Decimal calculations

① **Execution of decimal calculations**

The **ADC** and **SBC** are the only instructions which will yield proper decimal notation, set the decimal mode flag (D) to “1” with the **SED** instruction. After executing the **ADC** or **SBC** instruction, execute another instruction before executing the **SEC**, **CLC**, or **CLD** instruction.

② **Notes on status flag in decimal mode**

When decimal mode is selected, the values of three of the flags in the status register (the N, V, and Z flags) are invalid after a **ADC** or **SBC** instruction is executed.
The carry flag (C) is set to “1” if a carry is generated as a result of the calculation, or is cleared to “0” if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to “0” before each calculation. To check for a borrow, the C flag must be initialized to “1” before each calculation.

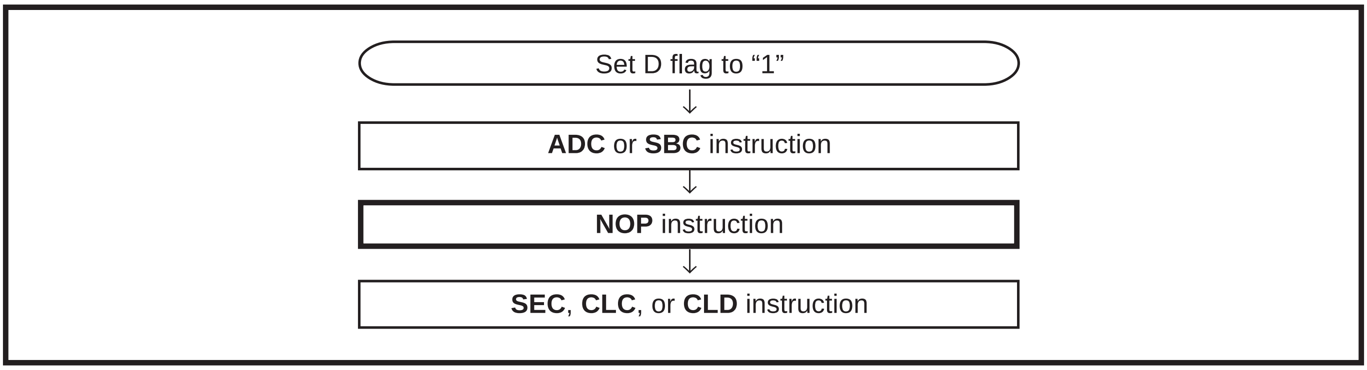


Fig. 3.3.8 Status flag at decimal calculations

(3) JMP instruction

When using the **JMP** instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

3.3.7 Programming and test of built-in PROM version

As for in the One Time PROM version (shipped in blank), its built-in PROM can be read or programmed with a general-purpose PROM programmer using a special programming adapter.
The built-in EPROM version is available only for program development and on-chip program evaluation.
The programming test and screening for PROM of the One Time PROM version (shipped in blank) are not performed in the assembly process and the following processes. To ensure reliability after programming, performing programming and test according to the Figure 3.3.9 before actual use are recommended.

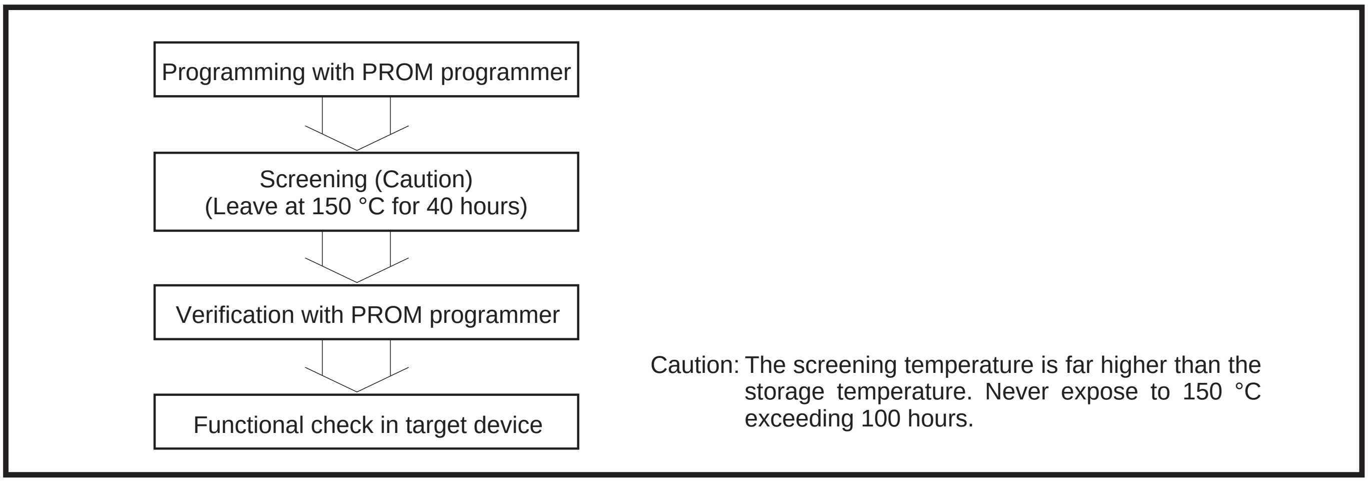


Fig. 3.3.9 Programming and testing of One Time PROM version

3.3.8 Notes on built-in PROM version

(1) Programming adapter

Use a special programming adapter shown in Table 3.3.1 and a general-purpose PROM programmer when reading from or programming to the built-in PROM in the built-in PROM version.

Table 3.3.1 Programming adapters

Microcomputer	Programming adapter
M37531E4SP (One Time PROM version shipped in blank)	PCA7435SP
M37531E8SP (One Time PROM version shipped in blank)	
M37531E4FP (One Time PROM version shipped in blank)	PCA7435FP
M37531E8FP (One Time PROM version shipped in blank)	
M37531E4GP (One Time PROM version shipped in blank)	PCA7435GP

(2) Programming/reading

In PROM mode, operation is the same as that of the M5M27C101AK, but programming conditions of PROM programmer are not set automatically because there are no internal device ID codes. Accurately set the following conditions for data programming /reading. Take care not to apply 21 V to V_{PP} pin (is also used as the CNV_{SS} pin), or the product may be permanently damaged.

- Programming voltage: 12.5 V
- Setting of PROM programmer switch: refer to Table 3.3.2.

Table 3.3.2 PROM programmer address setting

Product name format	PROM programmer start address	PROM programmer end address
M37531E4SP	Address $0E080_{16}$ (**Note 1**)	Address $0FFFD_{16}$ (**Note 1**)
M37531E4FP		
M37531E4GP		
M37531E8SP	Address $0C080_{16}$ (**Note 2**)	Address $0FFFD_{16}$ (**Note 2**)
M37531E8FP		

Notes 1: Addersses $E080_{16}$ to $FFFD_{16}$ in the built-in PROM corresponds to addresses $0E080_{16}$ to $0FFFD_{16}$ in the PROM programmer.

2: Addersses $C080_{16}$ to $FFFD_{16}$ in the built-in PROM corresponds to addresses $0C080_{16}$ to $0FFFD_{16}$ in the PROM programmer.

3.3.9 Termination of unused pins

(1) Terminate unused pins

① Output ports : Open

② Input ports :
Connect each pin to V_{CC} or V_{SS} through each resistor of 1 kΩ to 10 kΩ.
Ports that permit the selecting of a built-in pull-up or pull-down resistor can also use this resistor.
As for pins whose potential affects to operation modes such as pins CNV_{SS}, INT or others, select the V_{CC} pin or the V_{SS} pin according to their operation mode.

③ I/O ports :
- Set the I/O ports for the input mode and connect them to V_{CC} or V_{SS} through each resistor of 1 kΩ to 10 kΩ.
  Ports that permit the selecting of a built-in pull-up or pull-down resistor can also use this resistor.
  Set the I/O ports for the output mode and open them at “L” or “H”.
- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

(2) Termination remarks

① Input ports and I/O ports :
Do not open in the input mode.

● **Reason**
- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination ② and ③ shown on the above.

② I/O ports :
When setting for the input mode, do not connect to V_{CC} or V_{SS} directly.

● **Reason**
If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between a port and V_{CC} (or V_{SS}).

③ I/O ports :
When setting for the input mode, do not connect multiple ports in a lump to V_{CC} or V_{SS} through a resistor.

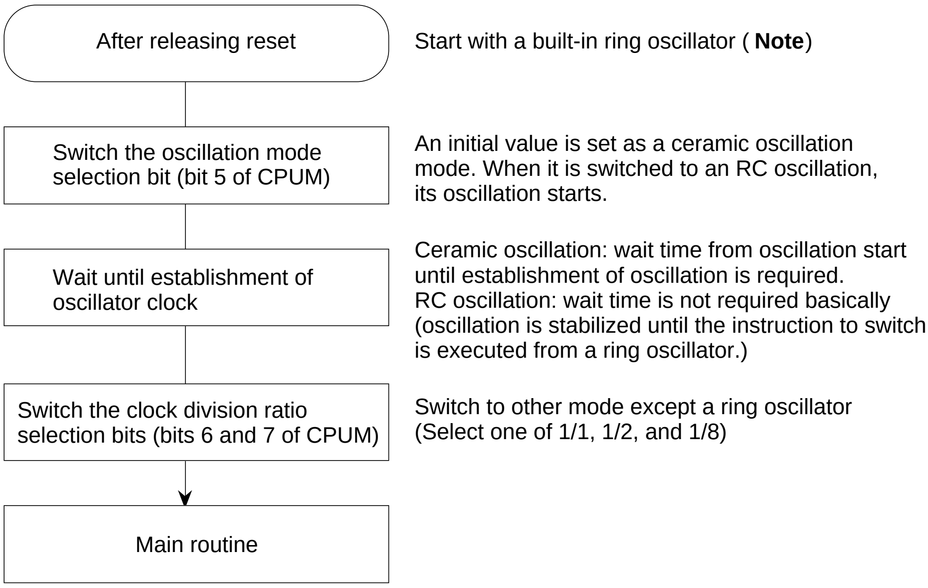
● **Reason**
If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

- At the termination of unused pins, perform wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

3.3.10 Notes on CPU mode register

(1) Switching method of CPU mode register after releasing reset

Switch the CPU mode register (CPUM) at the head of program after releasing reset in the following method.



Note. After releasing reset the operation starts by starting a ring oscillator automatically. Do not use a ring oscillator at ordinary operation.

Fig. 3.3.10 Switching method of CPU mode register

(2) Oscillation mode selection bit and clock division ratio selection bits

The oscillation mode selection bit can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit.

When a ceramic oscillation is selected, a double-speed mode of the clock division ratio selection bits can be used. Do not use it when an RC oscillation is selected.

3.3.11 Notes on using 32-pin version

- Do not change the $P3_5$, $P3_6$ pull-up control bit of the pull-up control register from the initial value “1”.
- Do not write to “1” to the serial I/O1 or INT_1 interrupt selection bit of the interrupt edge selection register.

3.4 Countermeasures against noise

3.4.1 Shortest wiring length

(1) Package

Select the smallest possible package to make the total wiring length short.

● **Reason**

The wiring length depends on a microcomputer package. Use of a small package, for example QFP and not DIP, makes the total wiring length short to reduce influence of noise.

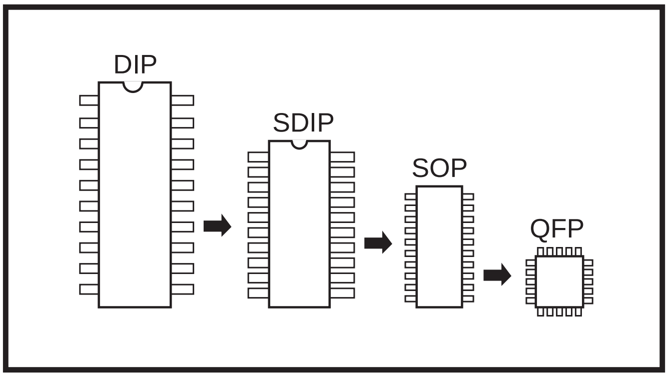


Fig. 3.4.1 Selection of packages

(2) Wiring for $\overline{\text{RESET}}$ pin

Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the Vss pin with the shortest possible wiring (within 20mm).

● **Reason**

The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

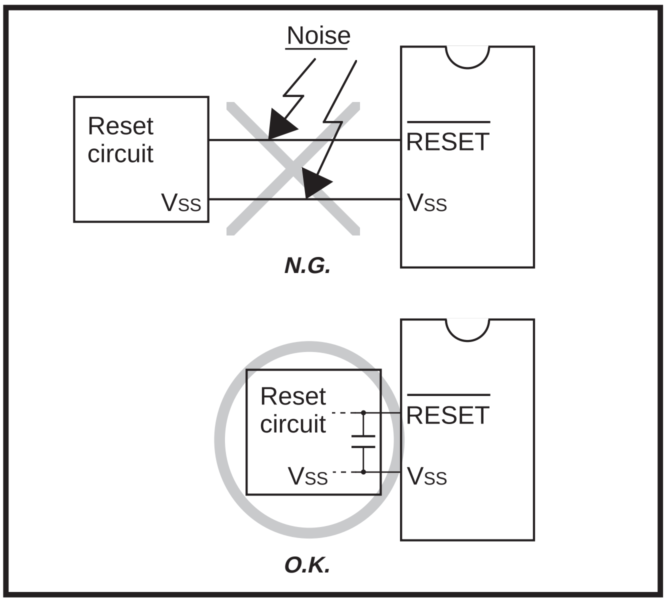


Fig. 3.4.2 Wiring for the $\overline{\text{RESET}}$ pin

(3) Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20mm) across the grounding lead of a capacitor which is connected to an oscillator and the VSS pin of a microcomputer as short as possible.
- Separate the VSS pattern only for oscillation from other VSS patterns.

● **Reason**

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the VSS level of a microcomputer and the VSS level of an oscillator, the correct clock will not be input in the microcomputer.

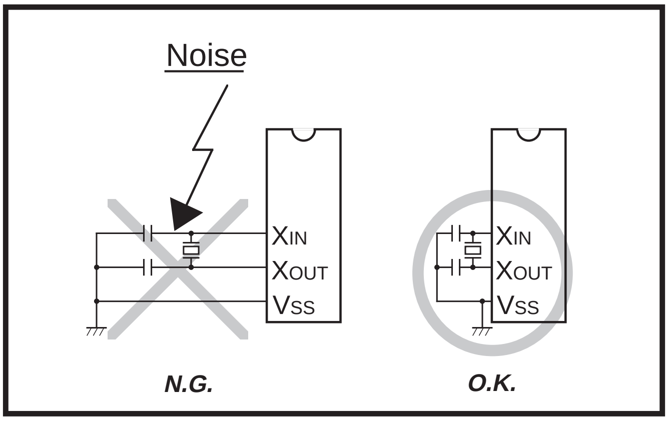


Fig. 3.4.3 Wiring for clock I/O pins

(4) Wiring to CNVss pin

Connect the CNVSS pin to the VSS pin with the shortest possible wiring.

● **Reason**

The processor mode of a microcomputer is influenced by a potential at the CNVSS pin. If a potential difference is caused by the noise between pins CNVSS and VSS, the processor mode may become unstable. This may cause a microcomputer malfunction or a program runaway.

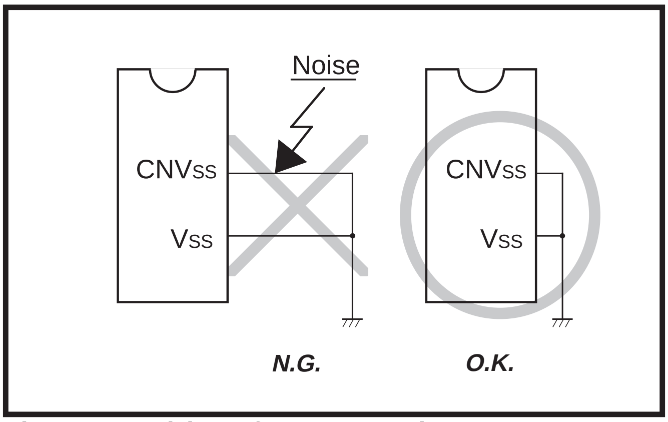


Fig. 3.4.4 Wiring for CNVss pin

(5) Wiring to VPP pin of One Time PROM version and EPROM version

Connect an approximately 5 kΩ resistor to the VPP pin the shortest possible in series and also to the VSS pin. When not connecting the resistor, make the length of wiring between the VPP pin and the VSS pin the shortest possible.

Note: Even when a circuit which included an approximately 5 kΩ resistor is used in the Mask ROM version, the microcomputer operates correctly.

● **Reason**

The VPP pin of the One Time PROM and the EPROM version is the power source input pin for the built-in PROM. When programming in the built-in PROM, the impedance of the VPP pin is low to allow the electric current for writing flow into the PROM. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the built-in PROM, which may cause a program runaway.

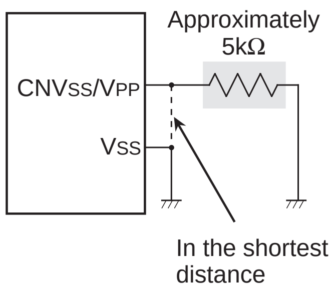


Fig. 3.4.5 Wiring for the VPP pin of the One Time PROM and the EPROM version

3.4.2 Connection of bypass capacitor across Vss line and Vcc line

Connect an approximately 0.1 μF bypass capacitor across the VSS line and the VCC line as follows:

- Connect a bypass capacitor across the VSS pin and the VCC pin at equal length.
- Connect a bypass capacitor across the VSS pin and the VCC pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for VSS line and VCC line.
- Connect the power source wiring via a bypass capacitor to the VSS pin and the VCC pin.

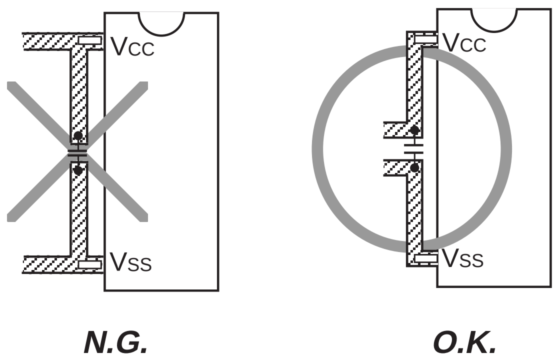


Fig. 3.4.6 Bypass capacitor across the VSS line and the VCC line

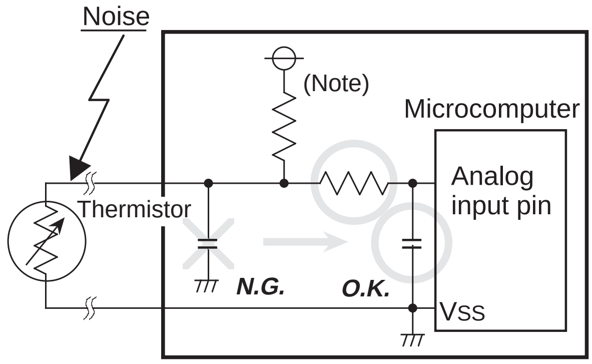
3.4.3 Wiring to analog input pins

- Connect an approximately 100 Ω to 1 kΩ resistor to an analog signal line which is connected to an analog input pin in series. Besides, connect the resistor to the microcomputer as close as possible.
- Connect an approximately 1000 pF capacitor across the Vss pin and the analog input pin. Besides, connect the capacitor to the Vss pin as close as possible. Also, connect the capacitor across the analog input pin and the Vss pin at equal length.

● Reason

Signals which is input in an analog input pin (such as an A-D converter/comparator input pin) are usually output signals from sensor. The sensor which detects a change of event is installed far from the printed circuit board with a microcomputer, the wiring to an analog input pin is longer necessarily. This long wiring functions as an antenna which feeds noise into the microcomputer, which causes noise to an analog input pin.

If a capacitor between an analog input pin and the Vss pin is grounded at a position far away from the Vss pin, noise on the GND line may enter a microcomputer through the capacitor.



Note : The resistor is used for dividing resistance with a thermistor.

Fig. 3.4.7 Analog signal line and a resistor and a capacitor

3.4.4 Oscillator concerns

Take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

(1) Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

● Reason

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

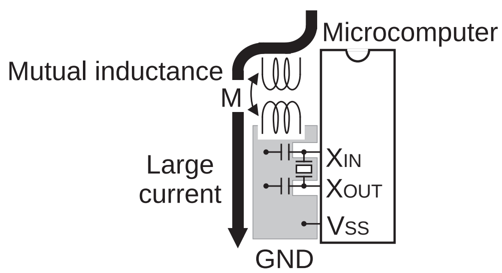


Fig. 3.4.8 Wiring for a large current signal line

(2) Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

● **Reason**

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

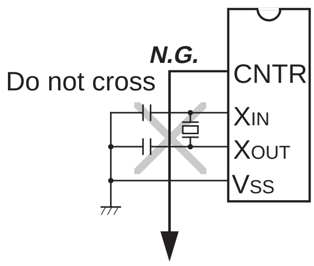


Fig. 3.4.9 Wiring of signal lines where potential levels change frequently

(3) Oscillator protection using Vss pattern

As for a two-sided printed circuit board, print a Vss pattern on the underside (soldering side) of the position (on the component side) where an oscillator is mounted.

Connect the Vss pattern to the microcomputer Vss pin with the shortest possible wiring. Besides, separate this Vss pattern from other Vss patterns.

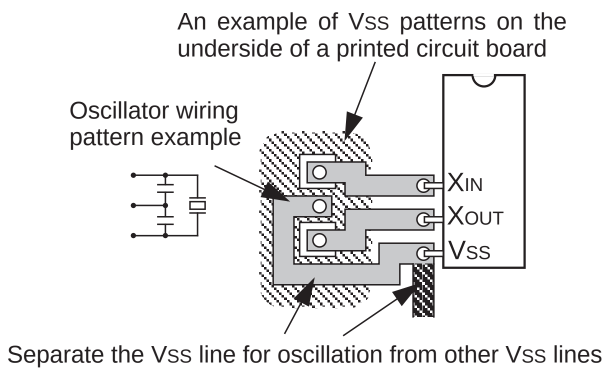


Fig. 3.4.10 Vss pattern on the underside of an oscillator

3.4.5 Setup for I/O ports
Setup I/O ports using hardware and software as follows:

<Hardware>
- Connect a resistor of 100 Ω or more to an I/O port in series.

<Software>
- As for an input port, read data several times by a program for checking whether input levels are equal or not.
- As for an output port, since the output data may reverse because of noise, rewrite data to its port latch at fixed periods.
- Rewrite data to direction registers and pull-up control registers at fixed periods.

Note: When a direction register is set for input port again at fixed periods, a several-nanosecond short pulse may be output from this port. If this is undesirable, connect a capacitor to this port to remove the noise pulse.

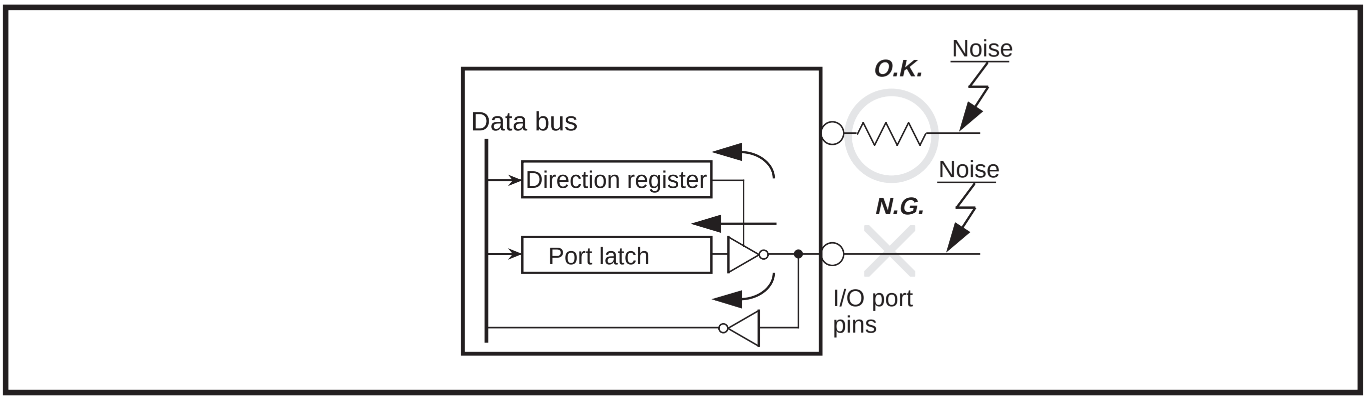


Fig. 3.4.11 Setup for I/O ports

3.4.6 Providing of watchdog timer function by software

If a microcomputer runs away because of noise or others, it can be detected by a software watchdog timer and the microcomputer can be reset to normal operation. This is equal to or more effective than program runaway detection by a hardware watchdog timer. The following shows an example of a watchdog timer provided by software.

In the following example, to reset a microcomputer to normal operation, the main routine detects errors of the interrupt processing routine and the interrupt processing routine detects errors of the main routine.

This example assumes that interrupt processing is repeated multiple times in a single main routine processing.

<The main routine>

- Assigns a single byte of RAM to a software watchdog timer (SWDT) and writes the initial value N in the SWDT once at each execution of the main routine. The initial value N should satisfy the following condition:
  N+1 ≥ (Counts of interrupt processing executed in each main routine)
  As the main routine execution cycle may change because of an interrupt processing or others, the initial value N should have a margin.
- Watches the operation of the interrupt processing routine by comparing the SWDT contents with counts of interrupt processing after the initial value N has been set.
- Detects that the interrupt processing routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
  If the SWDT contents do not change after interrupt processing.

<The interrupt processing routine>

- Decrements the SWDT contents by 1 at each interrupt processing.
- Determines that the main routine operates normally when the SWDT contents are reset to the initial value N at almost fixed cycles (at the fixed interrupt processing count).
- Detects that the main routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
  If the SWDT contents are not initialized to the initial value N but continued to decrement and if they reach 0 or less.

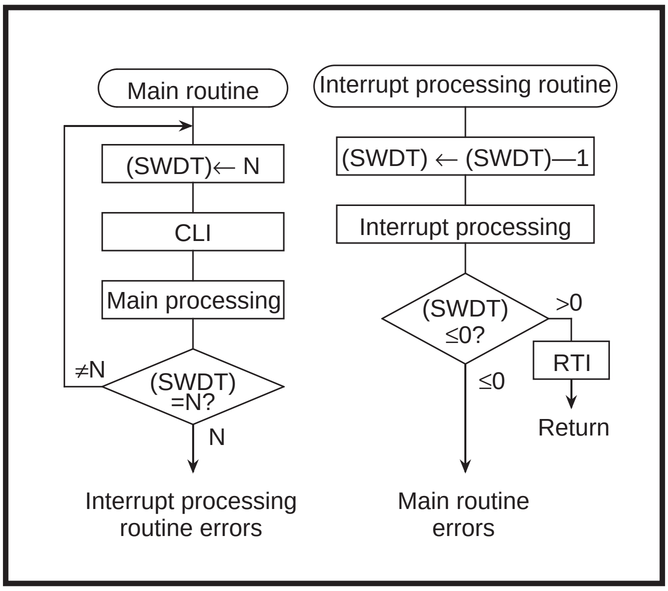


Fig. 3.4.12 Watchdog timer by software

3.5 List of registers

Port Pi

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi (Pi) (i = 0, 2, 3) [Address : 00_{16}, 04_{16}, 06_{16}]

B	Name	Function	At reset	R	W
0	Port Pi_0	● In output mode Write } Port latch Read } ● In input mode Write : Port latch Read : Value of pins	?	○	○
1	Port Pi_1		?	○	○
2	Port Pi_2		?	○	○
3	Port Pi_3		?	○	○
4	Port Pi_4		?	○	○
5	Port Pi_5		?	○	○
6	Port Pi_6		?	○	○
7	Port Pi_7		?	○	○

Note: The 32-pin package versions have nothing to be allocated for the following:
•Bits 6 and 7 of port P2
•Bits 5 and 6 of port P3.

Fig. 3.5.1 Structure of Port Pi (i = 0, 2, 3)

Port P1

b7 b6 b5 b4 b3 b2 b1 b0

Port P1 (P1) [Address : 02_{16}]

B	Name	Function	At reset	R	W
0	Port $P1_0$	● In output mode Write } Port latch Read } ● In input mode Write : Port latch Read : Value of pins	?	○	○
1	Port $P1_1$		?	○	○
2	Port $P1_2$		?	○	○
3	Port $P1_3$		?	○	○
4	Port $P1_4$		?	○	○
5	Nothing is allocated for these bits. When these bits are read out, the values are undefined.		?	×	×
6			?	×	×
7			?	×	×

Fig. 3.5.2 Structure of Port P1

Port Pi direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi direction register (PiD) (i = 0, 2, 3) [Address : 01_{16}, 05_{16}, 07_{16}]

B	Name	Function	At reset	R	W
0	Port Pi direction register	0 : Port Pi_0 input mode 1 : Port Pi_0 output mode	0	×	○
1		0 : Port Pi_1 input mode 1 : Port Pi_1 output mode	0	×	○
2		0 : Port Pi_2 input mode 1 : Port Pi_2 output mode	0	×	○
3		0 : Port Pi_3 input mode 1 : Port Pi_3 output mode	0	×	○
4		0 : Port Pi_4 input mode 1 : Port Pi_4 output mode	0	×	○
5		0 : Port Pi_5 input mode 1 : Port Pi_5 output mode	0	×	○
6		0 : Port Pi_6 input mode 1 : Port Pi_6 output mode	0	×	○
7		0 : Port Pi_7 input mode 1 : Port Pi_7 output mode	0	×	○

Note: The 32-pin package versions have nothing to be allocated for the following:
- Bits 6 and 7 of P2D
- Bits 5 and 6 of P3D.

Fig. 3.5.3 Structure of Port Pi direction register (i = 0, 2, 3)

Port P1 direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port P1 direction register (P1D) [Address : 03_{16}]

B	Name	Function	At reset	R	W
0	Port P1 direction register	0 : Port $P1_0$ input mode 1 : Port $P1_0$ output mode	0	×	○
1		0 : Port $P1_1$ input mode 1 : Port $P1_1$ output mode	0	×	○
2		0 : Port $P1_2$ input mode 1 : Port $P1_2$ output mode	0	×	○
3		0 : Port $P1_3$ input mode 1 : Port $P1_3$ output mode	0	×	○
4		0 : Port $P1_4$ input mode 1 : Port $P1_4$ output mode	0	×	○
5	Nothing is allocated for these bits. When these bits are read out, the values are undefined.		?	×	×
6			?	×	×
7			?	×	×

Fig. 3.5.4 Structure of Port P1 direction register

Pull-up control register

b7 b6 b5 b4 b3 b2 b1 b0

Pull-up control register (PULL) [Address : 16_{16}]

B	Name	Function	At reset	R	W
0	P0$_0$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
1	P0$_1$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
2	P0$_2$, P0$_3$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
3	P0$_4$ – P0$_7$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
4	P3$_0$ – P3$_3$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
5	P3$_4$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
6	P3$_5$, P3$_6$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○
7	P3$_7$ pull-up control bit	0 : Pull-up Off 1 : Pull-up On	1	○	○

Notes 1: Pins set to output are disconnected from the pull-up control.

2: Keep setting the P3$_5$, P3$_6$ pull-up control bit to “1” (initial value) for the 32-pin package versions.

Fig. 3.5.5 Structure of Pull-up control register

Port P1P3 control register

b7 b6 b5 b4 b3 b2 b1 b0

Port P1P3 control register (P1P3C) [Address : 17_{16}]

B	Name	Function	At reset	R	W
0	P3$_7$/INT$_0$ input level selection bit	0 : CMOS level 1 : TTL level	0	○	○
1	P3$_6$/INT$_1$ input level selection bit	0 : CMOS level 1 : TTL level	0	○	○
2	P1$_0$, P1$_2$,P1$_3$ input level selection bit	0 : CMOS level 1 : TTL level	0	○	○
3	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are “0”.		0	○	×
4			0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 3.5.6 Structure of Port P1P3 control register

Transmit/Receive buffer register

b7 b6 b5 b4 b3 b2 b1 b0

Transmit/Receive buffer register (TB/RB) [Address : 18_{16}]

B	Function	At reset	R	W
0	The transmission data is written to or the receive data is read out from this buffer register. • At writing: A data is written to the transmit buffer register. • At reading: The contents of the receive buffer register are read out.	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5		?	○	○
6		?	○	○
7		?	○	○

Note: The contents of transmit buffer register cannot be read out.
The data cannot be written to the receive buffer register.

Fig. 3.5.7 Structure of Transmit/Receive buffer register

Serial I/O1 status register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O1 status register (SIO1STS) [Address : 19_{16}]

B	Name	Function	At reset	R	W
0	Transmit buffer empty flag (TBE)	0 : Buffer full 1 : Buffer empty	1	○	×
1	Receive buffer full flag (RBF)	0 : Buffer empty 1 : Buffer full	0	○	×
2	Transmit shift register shift completion flag (TSC)	0 : Transmit shift in progress 1 : Transmit shift completed	0	○	×
3	Overrun error flag (OE)	0 : No error 1 : Overrun error	0	○	×
4	Parity error flag (PE)	0 : No error 1 : Parity error	0	○	×
5	Framing error flag (FE)	0 : No error 1 : Framing error	0	○	×
6	Summing error flag (SE)	0 : (OE) ∪ (PE) ∪ (FE) = 0 1 : (OE) ∪ (PE) ∪ (FE) = 1	0	○	×
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "1".		1	○	×

Fig. 3.5.8 Structure of Serial I/O1 status register

Serial I/O1 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O1 control register (SIO1CON) [Address : $1A_{16}$]

B	Name	Function	At reset	R	W
0	BRG count source selection bit (CSS)	0 : $f(X_{IN})$ 1 : $f(X_{IN})/4$	0	○	○
1	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is “1”.		1	○	×
2	Continuous transmit valid bit	0 : Continuous transmit invalid 1 : Continuous transmit valid	0	○	○
3	Transmit interrupt source selection bit (TIC)	0 : Interrupt when transmit buffer has emptied 1 : Interrupt when transmit shift operation is completed	0	○	○
4	Transmit enable bit (TE)	0 : Transmit disabled 1 : Transmit enabled	0	○	○
5	Receive enable bit (RE)	0 : Receive disabled 1 : Receive enabled	0	○	○
6	Serial I/O1 enable bit (SIOE)	b7 b6 0 0 : Serial I/O1 disabled 0 1 : Not available 1 0 : Serial I/O1 enabled 1 1 : Serial I/O1 cleared	0	○	○
7			0	○	○

Fig. 3.5.9 Structure of Serial I/O1 control register

UART control register

b7 b6 b5 b4 b3 b2 b1 b0

UART control register (UARTCON) [Address : $1B_{16}$]

B	Name	Function	At reset	R	W
0	Character length selection bit (CHAS)	0 : 8 bits 1 : 7 bits	0	○	○
1	Parity enable bit (PARE)	0 : Parity checking disabled 1 : Parity checking enabled	0	○	○
2	Parity selection bit (PARS)	0 : Even parity 1 : Odd parity	0	○	○
3	Stop bit length selection bit (STPS)	0 : 1 stop bit 1 : 2 stop bits	0	○	○
4	$P1_1$/TxD P-channel output disable bit (POFF)	In output mode 0 : CMOS output 1 : N-channel open-drain output	0	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are “1”.		1	○	×
6			1	○	×
7			1	○	×

Fig. 3.5.10 Structure of UART control register

Baud rate generator

b7 b6 b5 b4 b3 b2 b1 b0

Baud rate generator (BRG) [Address : 1C 16]

B	Function	At reset	R	W
0	Set a count value of baud rate generator.	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5		?	○	○
6		?	○	○
7		?	○	○

Fig. 3.5.11 Structure of Baud rate generator

Prescaler 12, Prescaler X

b7 b6 b5 b4 b3 b2 b1 b0

Prescaler 12 (PRE12) [Address : 28 16]
Prescaler X (PREX) [Address : 2C 16]

B	Function	At reset	R	W
0	•Set a count value of each prescaler. •The value set in this register is written to both each prescaler and the corresponding prescaler latch at the same time. •When this register is read out, the count value of the corresponding prescaler is read out.	1	○	○
1		1	○	○
2		1	○	○
3		1	○	○
4		1	○	○
5		1	○	○
6		1	○	○
7		1	○	○

Fig. 3.5.12 Structure of Prescaler 12, Prescaler X

Timer 1

b7 b6 b5 b4 b3 b2 b1 b0

Timer 1 (T1) [Address : 29_{16}]

B	Function	At reset	R	W
0	•Set a count value of timer 1. •The value set in this register is written to both timer 1 and timer 1 latch at the same time. •When this register is read out, the timer 1's count value is read out.	1	○	○
1		0	○	○
2		0	○	○
3		0	○	○
4		0	○	○
5		0	○	○
6		0	○	○
7		0	○	○

Fig. 3.5.13 Structure of Timer 1

Timer 2

b7 b6 b5 b4 b3 b2 b1 b0

Timer 2 (T2) [Address : $2A_{16}$]

B	Function	At reset	R	W
0	•Set a count value of timer 2. •The value set in this register is written to both timer 2 and timer 2 latch at the same time. •When this register is read out, the timer 2's count value is read out.	0	○	○
1		0	○	○
2		0	○	○
3		0	○	○
4		0	○	○
5		0	○	○
6		0	○	○
7		0	○	○

Fig. 3.5.14 Structure of Timer 2

Timer X mode register

b7 b6 b5 b4 b3 b2 b1 b0

Timer X mode register (TM) [Address : 2B $_{16}$]

B	Name	Function	At reset	R	W
0	Timer X operating mode bits	b1 b0 0 0 : Timer mode 0 1 : Pulse output mode 1 0 : Event counter mode 1 1 : Pulse width measurement mode	0	○	○
1			0	○	○
2	$CNTR_0$ active edge switch bit	The function depends on the operating mode. (Refer to Table 3.5.1)	0	○	○
3	Timer X count stop bit	0 : Count start 1 : Count stop	0	○	○
4	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".		0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 3.5.15 Structure of Timer X mode register

Table 3.5.1 $CNTR_0$ active edge switch bit function

Timer X operation modes		$CNTR_0$ active edge switch bit (bit 2 of address $2B_{16}$) contents
Timer mode	"0"	$CNTR_0$ interrupt request occurrence: Falling edge ; No influence to timer count
	"1"	$CNTR_0$ interrupt request occurrence: Rising edge ; No influence to timer count
Pulse output mode	"0"	Pulse output start: Beginning at "H" level $CNTR_0$ interrupt request occurrence: Falling edge
	"1"	Pulse output start: Beginning at "L" level $CNTR_0$ interrupt request occurrence: Rising edge
Event counter mode	"0"	Timer X: Rising edge count $CNTR_0$ interrupt request occurrence: Falling edge
	"1"	Timer X: Falling edge count $CNTR_0$ interrupt request occurrence: Rising edge
Pulse width measurement mode	"0"	Timer X: "H" level width measurement $CNTR_0$ interrupt request occurrence: Falling edge
	"1"	Timer X: "L" level width measurement $CNTR_0$ interrupt request occurrence: Rising edge

Timer X

b7 b6 b5 b4 b3 b2 b1 b0

Timer X (TX) [Address : 2D16]

B	Function	At reset	R	W
0	•Set a count value of timer X. •The value set in this register is written to both timer X and timer X latch at the same time. •When this register is read out, the timer X's count value is read out.	1	○	○
1		1	○	○
2		1	○	○
3		1	○	○
4		1	○	○
5		1	○	○
6		1	○	○
7		1	○	○

Fig. 3.5.16 Structure of Timer X

Timer count source set register

b7 b6 b5 b4 b3 b2 b1 b0

Timer count source set register (TCSS) [Address : 2E16]

B	Name	Function	At reset	R	W
0	Timer X count source selection bit (Note)	0 : f(XIN) / 16 1 : f(XIN) / 2	0	○	○
1	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".		0	○	×
2			0	○	×
3			0	○	×
4			0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Note: To switch the timer X count source selection bit, stop the timer X count operation before do that.

Fig. 3.5.17 Structure of Timer count source set register

Serial I/O2 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O2 control register (SIO2CON) [Address : 30 16]

B	Name	Function	At reset	R	W
0	Internal synchronous clock selection bits	b2 b1 b0 0 0 0 : f(XIN)/8 0 0 1 : f(XIN)/16 0 1 0 : f(XIN)/32 0 1 1 : f(XIN)/64 1 1 0 : f(XIN)/128 1 1 1 : f(XIN)/256	0	○	○
1			0	○	○
2			0	○	○
3	SDATA pin selection bit (**Note**)	0 : I/O port / SDATA input 1 : SDATA output	0	○	○
4	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0".		0	○	×
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○
6	SCLK pin selection bit	0 : External clock (SCLK is input) 1 : Internal clock (SCLK is output)	0	○	○
7	Transmit / receive shift completion flag	0 : shift in progress 1 : shift completed	0	○	×

Note: When using it as a SDATA input, set the port P13 direction register bit to "0".

Fig. 3.5.18 Structure of Serial I/O2 control register

Serial I/O2 register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O2 register (SIO2) [Address : 31 16]

B	Function	At reset	R	W
0	A shift register for serial transmission and reception. • At transmitting : Set a transmission data. • At receiving : A reception data is stored.	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5		?	○	○
6		?	○	○
7		?	○	○

Fig. 3.5.19 Structure of Serial I/O2 register

A-D control register

b7	b6	b5	b4	b3	b2	b1	b0

A-D control register (ADCON) [Address : 34_{16}]

B	Name	Function	At reset	R	W
0	Analog input pin selection bits	b2 b1 b0 0 0 0 : $P2_0/AN_0$ 0 0 1 : $P2_1/AN_1$ 0 1 0 : $P2_2/AN_2$ 0 1 1 : $P2_3/AN_3$ 1 0 0 : $P2_4/AN_4$ 1 0 1 : $P2_5/AN_5$ 1 1 0 : $P2_6/AN_6$ (**Note**) 1 1 1 : $P2_7/AN_7$ (**Note**)	0	○	○
1			0	○	○
2			0	○	○
3	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0".		0	○	×
4	AD conversion completion bit	0 : Conversion in progress 1 : Conversion completed	1	○	✻
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".		0	○	×
6			0	○	×
7			0	○	×

Note: These can be used only for the 36-pin package versions.

✻**:** This bit can be cleared to "0" by program, but cannot be set to "1".

Fig. 3.5.20 Structure of A-D control register

A-D conversion register (low-order)

b7	b6	b5	b4	b3	b2	b1	b0

A-D conversion register (low-order) (ADL) [Address : 35_{16}]

B	Function	At reset	R	W
0	The read-only register in which the A-D conversion's results are stored.	?	○	×
1		?	○	×
2		?	○	×
3		?	○	×
4		?	○	×
5		?	○	×
6		?	○	×
7		?	○	×

< 8-bit read>

b7 → b0

b9	b8	b7	b6	b5	b4	b3	b2

< 10-bit read>

b7 → b0

b7	b6	b5	b4	b3	b2	b1	b0

Fig. 3.5.21 Structure of A-D conversion register (low-order)

A-D conversion register (high-order)

b7 b6 b5 b4 b3 b2 b1 b0

A-D conversion register (high-order) (ADH) [Address : 36_{16}]

B	Function	At reset	R	W
0	The read-only register in which the A-D conversion's results are stored. < 10-bit read> b7 … b0: b9 b8	?	○	×
1		?	○	×
2	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".	?	○	×
3		?	○	×
4		?	○	×
5		?	○	×
6		?	○	×
7		?	○	×

Fig. 3.5.22 Structure of A-D conversion register (high-order)

MISRG

b7 b6 b5 b4 b3 b2 b1 b0

MISRG [Address : 38_{16}]

B	Name	Function	At reset	R	W
0	Oscillation stabilization time set bit after release of the STP instruction	0 : Set "01_{16}" in timer 1, and "FF_{16}" in prescaler 12 automatically 1 : Not set automatically	0	○	○
1	These are reserved bits. Do not write "1" to these bits.		0	○	×
2			0	○	×
3			0	○	×
4	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".		0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 3.5.23 Structure of MISRG

Watchdog timer control register

b7 b6 b5 b4 b3 b2 b1 b0

Watchdog timer control register (WDTCON) [Address : 39_{16}]

B	Name	Function	At reset	R	W
0	Watchdog timer H (The high-order 6 bits are read-only bits.)		1	○	×
1			1	○	×
2			1	○	×
3			1	○	×
4			1	○	×
5			1	○	×
6	STP instruction disable bit	0 : STP instruction enabled 1 : STP instruction disabled	0	○	○
7	Watchdog timer H count source selection bit	0 : Watchdog timer L underflow 1 : $f(X_{IN})/16$	0	○	○

Fig. 3.5.24 Structure of Watchdog timer control register

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt edge selection register (INTEDGE) [Address : $3A_{16}$]

B	Name	Function	At reset	R	W
0	INT_0 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
1	INT_1 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
2	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0".		0	○	×
3			0	○	×
4	Serial I/O1 or INT_1 interrupt selection bit (**Note**)	0 : Serial I/O1 1 : INT_1	0	○	○
5	Timer X or key-on wake up interrupt selection bit	0 : Timer X 1 : Key-on wake up	0	○	○
6	Timer 2 or serial I/O2 interrupt selection bit	0 : Timer 2 1 : Serial I/O2	0	○	○
7	$CNTR_0$ or AD converter interrupt selection bit	0 : $CNTR_0$ 1 : AD converter	0	○	○

Note: Do not write "1" to bit 4 in the 32-pin package versions.

Fig. 3.5.25 Structure of Interrupt edge selection register

CPU mode register

b7 b6 b5 b4 b3 b2 b1 b0

CPU mode register (CPUM) [Address : $3B_{16}$]

B	Name	Function	At reset	R	W
0	Processor mode bits	b1 b0 0 0 : Single-chip mode 0 1 : Not available 1 0 : Not available 1 1 : Not available	0	○	○
1			0	○	○
2	Stack page selection bit	0 : 0 page 1 : 1 page	0	○	○
3	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0". (Do not write "1".)		0	○	×
4			0	○	×
5	Oscillation mode selection bit	0 : Ceramic oscillation 1 : RC oscillation	0	○	○
6	Clock division ratio selection bits	b7 b6 0 0 : ϕ = f(X_{IN})/2 (high-speedmode) 0 1 : ϕ = f(X_{IN})/8 (middle-speed mode) 1 0 : Applied from ring oscillator 1 1 : ϕ = f(X_{IN}) (double-speed mode)	0	○	○
7			1	○	○

Fig. 3.5.26 Structure of CPU mode register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address : $3C_{16}$]

B	Name	Function	At reset	R	W
0	Serial I/O1 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
1	Serial I/O1 transmit or INT_1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
2	INT_0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
3	Timer X or key-on wake up interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
4	Timer 1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
5	Timer 2 or serial I/O2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
6	$CNTR_0$ or AD converter interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	✻
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0".		0	○	×

✻: These bits can be cleared to "0" by program, but cannot be set to "1".

Fig. 3.5.27 Structure of Interrupt request register 1

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address : 3E$_{16}$]

B	Name	Function	At reset	R	W
0	Serial I/O1 receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Serial I/O1 transmit or INT$_1$ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	INT$_0$ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Timer X or key-on wake up interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Timer 2 or serial I/O2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	CNTR$_0$ or AD converter interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Nothing is allocated for this bit. Do not write “1” to this bit. When this bit is read out, the value is “0”.		0	○	×

Fig. 3.5.28 Structure of Interrupt control register 1

3.6 Mask ROM confirmation form

GZZ-SH52-89B<85B0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER
M37531M4-XXXFP/GP/SP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ❋.

❋ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

❋ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37531M4-XXXFP ☐ M37531M4-XXXGP ☐ M37531M4-XXXSP

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27C256		☐ 27C512	
EPROM address		EPROM address	
0000$_{16}$ – 000F$_{16}$	Area for ASCII codes of the name of the product 'M37531M4–'	0000$_{16}$ – 000F$_{16}$	Area for ASCII codes of the name of the product 'M37531M4–'
0010$_{16}$ – 607F$_{16}$	(shaded)	0010$_{16}$ – E07F$_{16}$	(shaded)
6080$_{16}$ – 7FFD$_{16}$	Data ROM (8K–130) bytes	E080$_{16}$ – FFFD$_{16}$	Data ROM (8K–130) bytes
7FFE$_{16}$ – 7FFF$_{16}$	(shaded)	FFFE$_{16}$ – FFFF$_{16}$	(shaded)

In the address space of the microcomputer, the internal ROM area is from addresses E080$_{16}$ to FFFD$_{16}$. The reset vector is stored in addresses FFFC$_{16}$ and FFFD$_{16}$.

(1) Set "FF$_{16}$" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37531M4–' to addresses 0000$_{16}$ to 000F$_{16}$. ASCII codes 'M37531M4–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000$_{16}$	'M' = 4D$_{16}$	0008$_{16}$	'–' = 2D$_{16}$
0001$_{16}$	'3' = 33$_{16}$	0009$_{16}$	FF$_{16}$
0002$_{16}$	'7' = 37$_{16}$	000A$_{16}$	FF$_{16}$
0003$_{16}$	'5' = 35$_{16}$	000B$_{16}$	FF$_{16}$
0004$_{16}$	'3' = 33$_{16}$	000C$_{16}$	FF$_{16}$
0005$_{16}$	'1' = 31$_{16}$	000D$_{16}$	FF$_{16}$
0006$_{16}$	'M' = 4D$_{16}$	000E$_{16}$	FF$_{16}$
0007$_{16}$	'4' = 34$_{16}$	000F$_{16}$	FF$_{16}$

(1 / 2)

GZZ-SH52-89B<85B0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37531M4-XXXFP/GP/SP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27C256	27C512
The pseudo-command	△✻=△$8000 △.BYTE△'M37531M4-'	△✻=△$0000 △.BYTE△'M37531M4-'

ASCII codes, that indicates the name of the product, are written in addresses 0000_{16} to 0008_{16} of the EPROM by programming the above pseudo-command, which depends on a type of EPROM to be written, at beginning of the source program.

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

❋ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (36P2R for M37531M4-XXXFP, 32P6B for M37531M4-XXXGP, 32P4B for M37531M4-XXXSP) and attach to the mask ROM confirmation form.

❋ 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the XIN-XOUT oscillator?

☐ Ceramic resonator

☐ External clock input ☐ Other (   )

At what frequency? f(XIN) = ☐ MHz

❋ 4. Comments

(2 / 2)

GZZ-SH52-90B<85C0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER
M37531M4T-XXXSP/FP/GP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ❋.

❋ Customer			Issuance signature	Submitted by	Supervisor
	Company name	TEL ( )			
	Date issued	Date:			

❋ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name: ☐ M37531M4T-XXXSP ☐ M37531M4T-XXXFP ☐ M37531M4T-XXXGP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27C256		☐ 27C512	
EPROM address		EPROM address	
0000_{16} – $000F_{16}$	Area for ASCII codes of the name of the product 'M37531M4T–'	0000_{16} – $000F_{16}$	Area for ASCII codes of the name of the product 'M37531M4T–'
0010_{16} – $607F_{16}$	(shaded)	0010_{16} – $E07F_{16}$	(shaded)
6080_{16} – $7FFD_{16}$	Data ROM (8K–130) bytes	$E080_{16}$ – $FFFD_{16}$	Data ROM (8K–130) bytes
$7FFE_{16}$ – $7FFF_{16}$	(shaded)	$FFFE_{16}$ – $FFFF_{16}$	(shaded)

In the address space of the microcomputer, the internal ROM area is from addresses $E080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37531M4T–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37531M4T–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'T' = 54_{16}
0001_{16}	'3' = 33_{16}	0009_{16}	'–' = $2D_{16}$
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'5' = 35_{16}	$000B_{16}$	FF_{16}
0004_{16}	'3' = 33_{16}	$000C_{16}$	FF_{16}
0005_{16}	'1' = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'4' = 34_{16}	$000F_{16}$	FF_{16}

(1 / 2)

GZZ-SH52-90B<85C0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37531M4T-XXXSP/FP/GP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27C256	27C512
The pseudo-command	△✻=△$8000 △.BYTE△'M37531M4T-'	△✻=△$0000 △.BYTE△'M37531M4T-'

ASCII codes, that indicates the name of the product, are written in addresses 0000_{16} to 0008_{16} of the EPROM by programming the above pseudo-command, which depends on the type of EPROM to be written, at beginning of the source program.

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

❋ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (32P4B for M37531M4T-XXXSP, 36P2R for M37531M4T-XXXFP, 32P6B for M37531M4T-XXXGP) and attach to the mask ROM confirmation form.

❋ 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the XIN-XOUT oscillator?

☐ Ceramic resonator

☐ External clock input ☐ Other (   )

At what frequency? f(XIN) = ☐ MHz

❋ 4. Comments

(2 / 2)

GZZ-SH56-95B<98A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER
M37531M4V-XXXGP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ❋.

				Issuance signature	Submitted by	Supervisor
❋	Customer	Company name	TEL ( )			
		Date issued	Date:			

❋ 1. Confirmation

Specify the type of EPROMs submitted.

Three EPROMs are required for each pattern (Check @ in the appropriate box).

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM					(hexadecimal notation)

EPROM type (indicate the type used)

☐ **27C256**		☐ **27C512**	
EPROM address		EPROM address	
0000_{16} – $000F_{16}$	Area for ASCII codes of the name of the product 'M37531M4V–'	0000_{16} – $000F_{16}$	Area for ASCII codes of the name of the product 'M37531M4V–'
0010_{16} – $607F_{16}$	(shaded)	0010_{16} – $E07F_{16}$	(shaded)
6080_{16} – $7FFD_{16}$	Data ROM (8K–130) bytes	$E080_{16}$ – $FFFD_{16}$	Data ROM (8K–130) bytes
$7FFE_{16}$ – $7FFF_{16}$	(shaded)	$FFFE_{16}$ – $FFFF_{16}$	(shaded)

In the address space of the microcomputer, the internal ROM area is from addresses $E080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set "FF_{16}" in the shaded area.

(2) Write the ASCII codes that indicates the name of the product 'M37531M4V–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37531M4V–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'V' = 56_{16}
0001_{16}	'3' = 33_{16}	0009_{16}	' – ' = $2D_{16}$
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'5' = 35_{16}	$000B_{16}$	FF_{16}
0004_{16}	'3' = 33_{16}	$000C_{16}$	FF_{16}
0005_{16}	'1' = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'4' = 34_{16}	$000F_{16}$	FF_{16}

(1 / 2)

GZZ-SH56-95B<98A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37531M4V-XXXGP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27C256	27C512
The pseudo-command	△✻=△$8000 △.BYTE△'M37531M4V-'	△✻=△$0000 △.BYTE△'M37531M4V-'

ASCII codes, that indicates the name of the product, are written in addresses 0000_{16} to 0008_{16} of the EPROM by programming the above pseudo-command, which depends on a type of EPROM to be written, at beginning of the source program.

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

❋ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (32P6B for M37531M4V-XXXGP) and attach to the mask ROM confirmation form.

❋ 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator?

☐ Ceramic resonator

☐ External clock input ☐ Other ( )

At what frequency? f(X_{IN}) = ☐ MHz

❋ 4. Comments

(2 / 2)

GZZ-SH53-64B<87B0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER
M37531M8-XXXFP/GP/SP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ❈.

❈ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

❈ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name : ☐ M37531M8-XXXFP ☐ M37531M8-XXXGP ☐ M37531M8-XXXSP

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27C256		☐ 27C512	
EPROM address		EPROM address	
0000_{16} – $000F_{16}$	Area for ASCII codes of the name of the product 'M37531M8–'	0000_{16} – $000F_{16}$	Area for ASCII codes of the name of the product 'M37531M8–'
0010_{16} – $407F_{16}$	(shaded)	0010_{16} – $C07F_{16}$	(shaded)
4080_{16} – $7FFD_{16}$	Data ROM (16K–130) bytes	$C080_{16}$ – $FFFD_{16}$	Data ROM (16K–130) bytes
$7FFE_{16}$ – $7FFF_{16}$	(shaded)	$FFFE_{16}$ – $FFFF_{16}$	(shaded)

In the address space of the microcomputer, the internal ROM area is from addresses $C080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set "FF_{16}" in the shaded area.
(2) Write the ASCII codes that indicates the name of the product 'M37531M8–' to addresses 0000_{16} to $000F_{16}$. ASCII codes 'M37531M8–' are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	' – ' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'7' = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	'5' = 35_{16}	$000B_{16}$	FF_{16}
0004_{16}	'3' = 33_{16}	$000C_{16}$	FF_{16}
0005_{16}	'1' = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'8' = 38_{16}	$000F_{16}$	FF_{16}

(1 / 2)

GZZ-SH53-64B<87B0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37531M8-XXXFP/GP/SP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27C256	27C512
The pseudo-command	△✻=△$8000 △.BYTE△'M37531M8-'	△✻=△$0000 △.BYTE△'M37531M8-'

ASCII codes, that indicates the name of the product, are written in addresses 0000_{16} to $000F_{16}$ of the EPROM by programming the above pseudo-command, which depends on a type of EPROM to be written, at beginning of the source program.

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

❋ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (36P2R for M37531M8-XXXFP, 32P6B for M37531M8-XXXGP, 32P4B for M37531M8-XXXSP) and attach to the mask ROM confirmation form.

❋ 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the XIN-XOUT oscillator?

☐ Ceramic resonator

☐ External clock input ☐ Other ( )

At what frequency? f(XIN) = ☐ MHz

❋ 4. Comments

(2 / 2)

3.7 ROM programming confirmation form

GZZ-SH54-78B<91A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER
M37531E4T-XXXGP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ❋.

❋ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

❋ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM data based on this data.
We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data.
Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27C256		☐ 27C512	
EPROM address		EPROM address	
0000_{16}	Area for ASCII codes of the name of the product ‘M37531E4T–’	0000_{16}	Area for ASCII codes of the name of the product ‘M37531E4T–’
$000F_{16}$		$000F_{16}$	
0010_{16}		0010_{16}	
$607F_{16}$		$E07F_{16}$	
6080_{16}	Data ROM (8K–130) bytes	$E080_{16}$	Data ROM (8K–130) bytes
$7FFD_{16}$		$FFFD_{16}$	
$7FFE_{16}$		$FFFE_{16}$	
$7FFF_{16}$		$FFFF_{16}$	

In the address space of the microcomputer, the internal ROM area is from addresses $E080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set “FF_{16}” in the shaded area.
(2) Write the ASCII codes that indicates the name of the product ‘M37531E4T–’ to addresses 0000_{16} to $000F_{16}$. ASCII codes ‘M37531E4T–’ are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	‘M’ = $4D_{16}$	0008_{16}	‘ T ’ = 54_{16}
0001_{16}	‘3’ = 33_{16}	0009_{16}	‘ – ’ = $2D_{16}$
0002_{16}	‘7’ = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	‘5’ = 35_{16}	$000B_{16}$	FF_{16}
0004_{16}	‘3’ = 33_{16}	$000C_{16}$	FF_{16}
0005_{16}	‘1’ = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	‘E’ = 45_{16}	$000E_{16}$	FF_{16}
0007_{16}	‘4’ = 34_{16}	$000F_{16}$	FF_{16}

(1 / 2)

GZZ-SH54-78B<91A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37531E4T-XXXGP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27C256	27C512
The pseudo-command	△✻=△$8000 △.BYTE △'M37531E4T-'	△✻=△$0000 △.BYTE △'M37531E4T-'

ASCII codes, that indicates the name of the product, are written in addresses 0000_{16} to 0008_{16} of the EPROM by programming the above pseudo-command, which depends on a type of EPROM to be written, at beginning of the source program.

Note : If the name of the product written to the EPROMs does not match the name of the ROM programming confirmation form, the ROM processing is disabled. Write the data correctly.

❋ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (32P6B for M37531E4T-XXXGP) and attach to the ROM programming confirmation form.

❋ 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the XIN-XOUT oscillator?

☐ Ceramic resonator

☐ External clock input ☐ Other ( )

At what frequency? f(XIN) = ☐ MHz

❋ 4. Comments

(2 / 2)

GZZ-SH54-79B<91A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER
M37531E4V-XXXGP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ❋.

					Submitted by	Supervisor
❋	Customer	Company name	TEL ( )	Issuance signature		
		Date issued	Date:			

❋ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM data based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27C256		☐ 27C512	
EPROM address		EPROM address	
0000_{16} – $000F_{16}$	Area for ASCII codes of the name of the product ‘M37531E4V–’	0000_{16} – $000F_{16}$	Area for ASCII codes of the name of the product ‘M37531E4V–’
0010_{16} – $607F_{16}$	(shaded)	0010_{16} – $E07F_{16}$	(shaded)
6080_{16} – $7FFD_{16}$	Data ROM (8K–130) bytes	$E080_{16}$ – $FFFD_{16}$	Data ROM (8K–130) bytes
$7FFE_{16}$ – $7FFF_{16}$	(shaded)	$FFFE_{16}$ – $FFFF_{16}$	(shaded)

In the address space of the microcomputer, the internal ROM area is from addresses $E080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set “FF_{16}” in the shaded area.
(2) Write the ASCII codes that indicates the name of the product ‘M37531E4V–’ to addresses 0000_{16} to $000F_{16}$. ASCII codes ‘M37531E4V–’ are listed on the right. The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	‘M’ = $4D_{16}$	0008_{16}	‘ V ’ = 56_{16}
0001_{16}	‘3’ = 33_{16}	0009_{16}	‘ – ’ = $2D_{16}$
0002_{16}	‘7’ = 37_{16}	$000A_{16}$	FF_{16}
0003_{16}	‘5’ = 35_{16}	$000B_{16}$	FF_{16}
0004_{16}	‘3’ = 33_{16}	$000C_{16}$	FF_{16}
0005_{16}	‘1’ = 31_{16}	$000D_{16}$	FF_{16}
0006_{16}	‘E’ = 45_{16}	$000E_{16}$	FF_{16}
0007_{16}	‘4’ = 34_{16}	$000F_{16}$	FF_{16}

(1 / 2)

GZZ-SH54-79B<91A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37531E4V-XXXGP
MITSUBISHI ELECTRIC

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27C256	27C512
The pseudo-command	△✻=△$8000 △.BYTE △'M37531E4V-'	△✻=△$0000 △.BYTE △'M37531E4V-'

ASCII codes, that indicates the name of the product, are written in addresses 0000_{16} to 0008_{16} of the EPROM by programming the above pseudo-command, which depends on a type of EPROM to be written, at beginning of the source program.
Note : If the name of the product written to the EPROMs does not match the name of the ROM programming confirmation form, the ROM processing is disabled. Write the data correctly.

❋ 2. Mark specification
Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (32P6B for M37531E4V-XXXGP) and attach to the ROM programming confirmation form.

❋ 3. Usage conditions
Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator?

☐ Ceramic resonator
☐ External clock input ☐ Other ( )

At what frequency? $f(X_{IN})$ = ☐ MHz

❋ 4. Comments

(2 / 2)

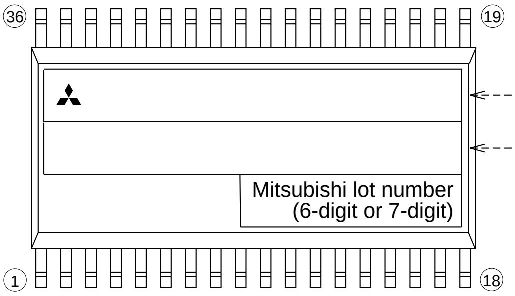
3.8 Mark specification form

36P2R-A (36-PIN SHRINK SOP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name [ ]

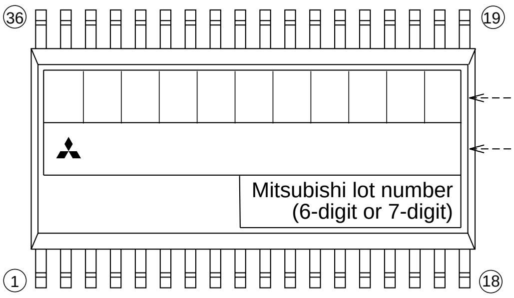
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name
Mitsubishi IC catalog name

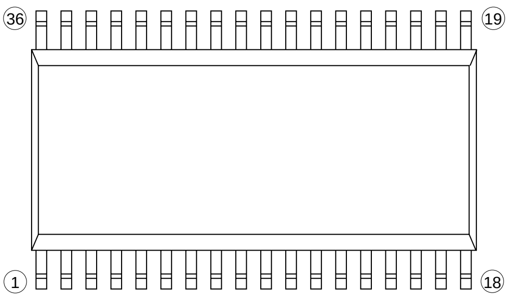
B. Customer's Parts Number + Mitsubishi catalog name



Customer's Parts Number
Note : The fonts and size of characters are standard Mitsubishi type.
Mitsubishi IC catalog name
Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's Parts Number can be up to 11 characters : Only 0 ~ 9, A ~ Z, +, –, /, (,), &, ©, . (periods), , (commas) are usable.
4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required [ ]

C. Special Mark Required



Note1 : If the Special Mark is to be Printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible.
Mitsubishi lot number (6-digit or 7-digit) and Mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the Special Mark, check the box below.
Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required [ ]

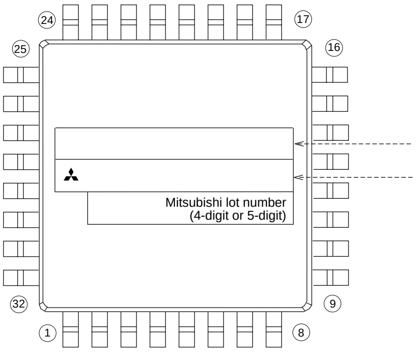
3 : The standard Mitsubishi font is used for all characters except for a logo.

32P6B (32-PIN LQFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

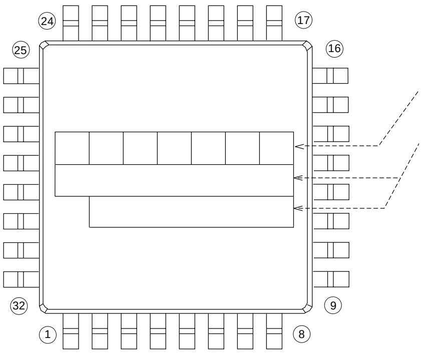
Please choose one of the marking types below (A, B), and enter the Mitsubishi catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



Mitsubishi IC catalog name
Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi catalog name



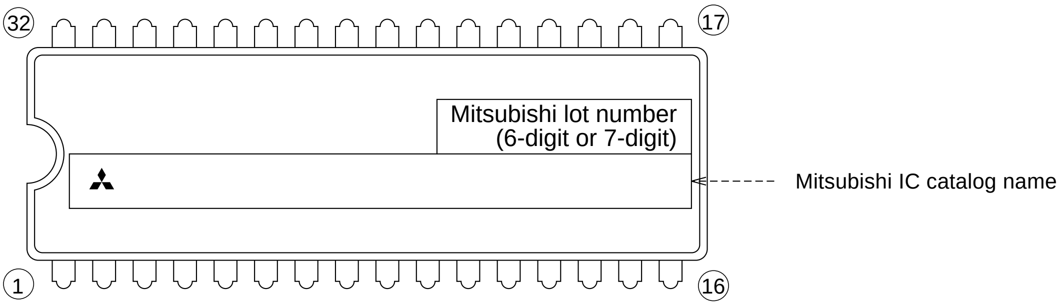
Customer's Parts Number
Note : The fonts and size of characters are standard Mitsubishi type.
Mitsubishi IC catalog name
Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's Parts Number can be up to 7 characters : Only 0 ~ 9, A ~ Z, +, –, /, (,), &, ©, **.** (periods), **,** (commas) are usable.

32P4B (32-PIN SHRINK DIP) MARK SPECIFICATION FORM

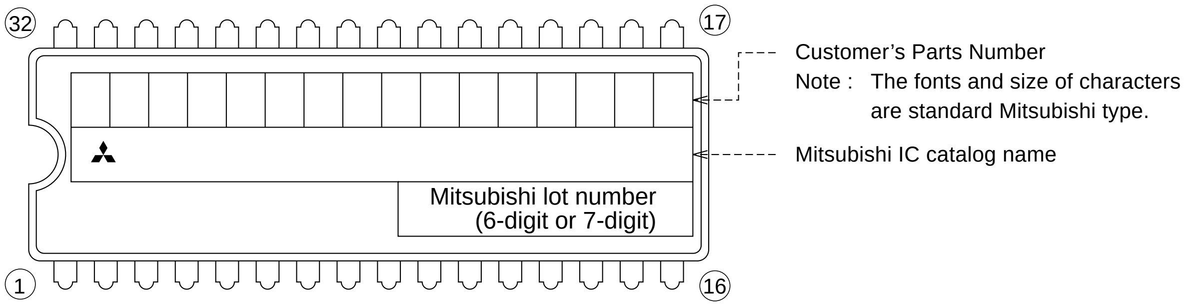
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



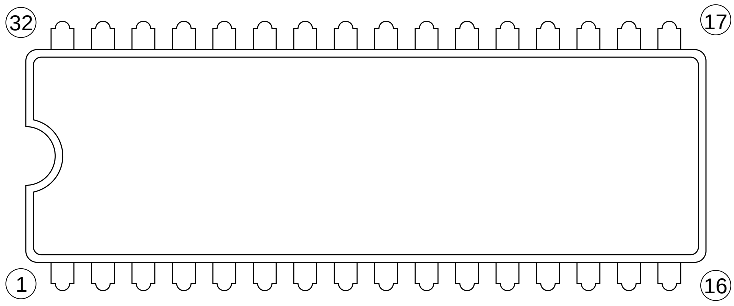
B. Customer’s Parts Number + Mitsubishi catalog name



Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer’s Parts Number can be up to 16 characters : Only 0 ~ 9, A ~ Z, +, –, /, (,), &, ©, . (periods), and , (commas) are usable.
4 : If the Mitsubishi logo is not required, check the box on the right.

Mitsubishi logo is not required ☐

C. Special Mark Required



Note1 : If the Special Mark is to be Printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and Mask ROM number (3-digit) are always marked.
2 : If the customer’s trade mark logo must be used in the Special Mark, check the box on the right. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.
3 : The standard Mitsubishi font is used for all characters except for a logo.

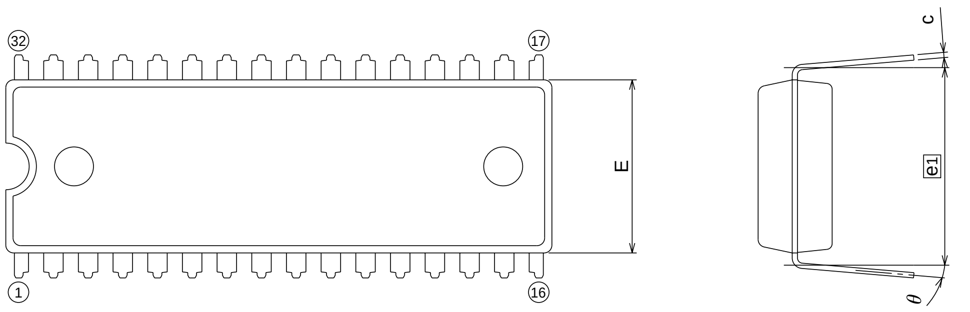
Special logo required ☐

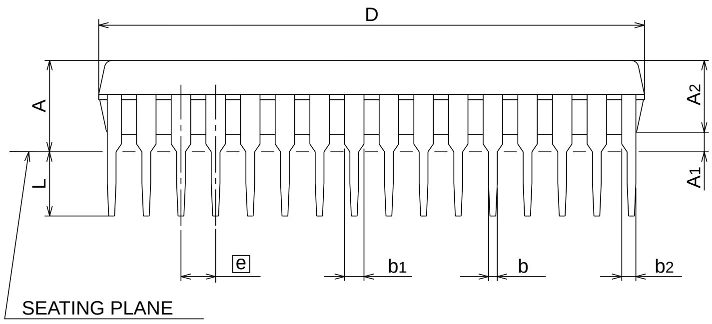
3.9 Package outline

32P4B

Plastic 32pin 400mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP32-P-400-1.78	–	2.2	Alloy 42/Cu Alloy



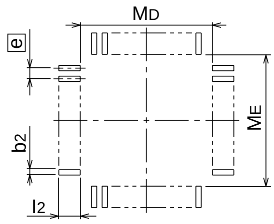


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.08
A_1	0.51	–	–
A_2	–	3.8	–
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
$\boxed{e}$	–	1.778	–
$\boxed{e_1}$	–	10.16	–
L	3.0	–	–
θ	0°	–	15°

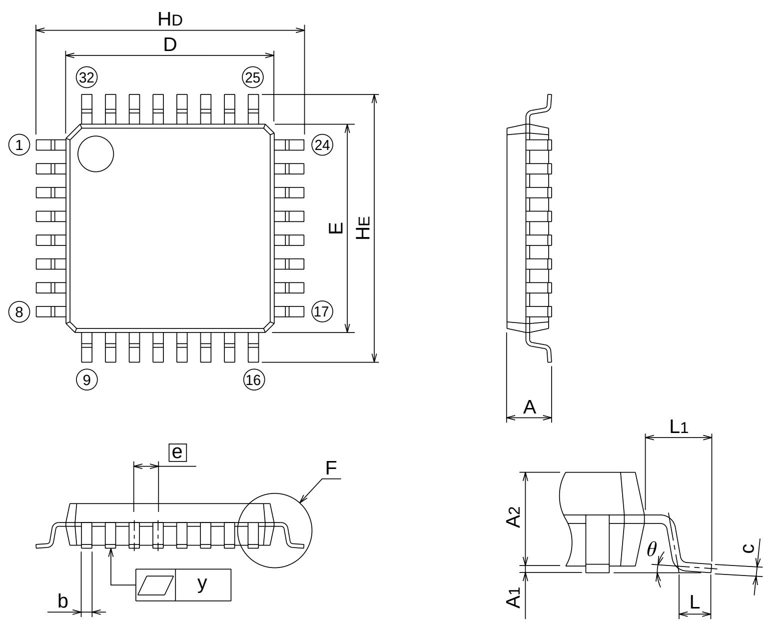
32P6B-A

Plastic 32pin 7×7mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP32-P-77-0.80	–		Alloy 42



Recommended Mount Pad



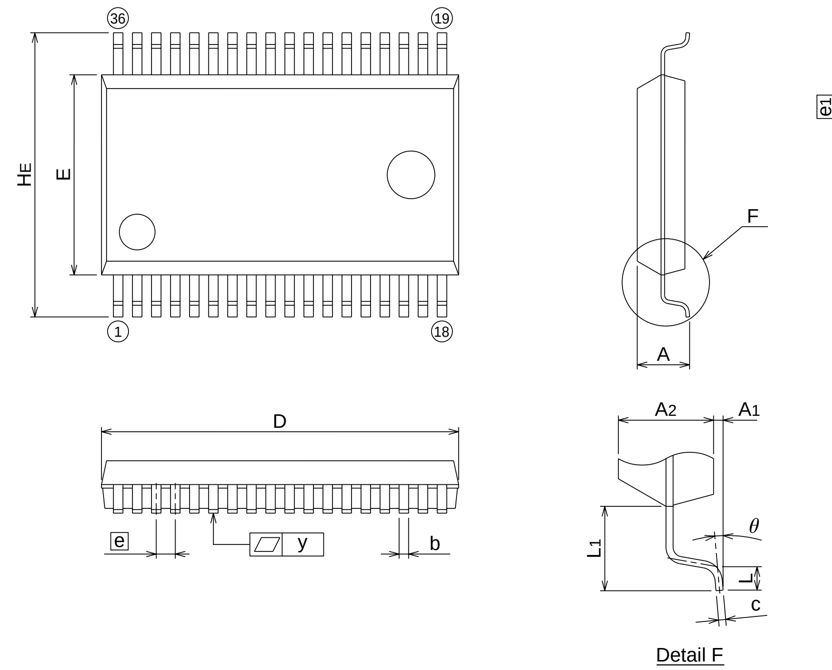
Detail F

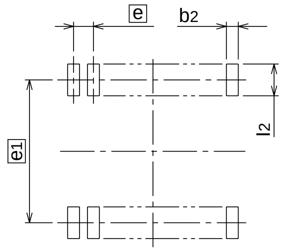
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.3	0.35	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
$\boxed{e}$	–	0.8	–
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
L	0.3	0.5	0.7
L_1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.5	–
l_2	1.0	–	–
M_D	–	7.4	–
M_E	–	7.4	–

36P2R-A

Plastic 36pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP36-P-450-0.80	–	0.53	Alloy 42





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A_1	0.05	–	–
A_2	–	2.0	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	14.8	15.0	15.2
E	8.2	8.4	8.6
$\boxed{e}$	–	0.8	–
H_E	11.63	11.93	12.23
L	0.3	0.5	0.7
L_1	–	1.765	–
y	–	–	0.15
θ	0°	–	10°
b_2	–	0.5	–
$\boxed{e_1}$	–	11.43	–
l_2	1.27	–	–

APPENDIX
3.10 Machine instructions

3.10 Machine instructions

Symbol	Function	Details	IMP			IMM			A			BIT, A, R			ZP			BIT, ZP, R		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
ADC (Note 1) (Note 5)	When T = 0 A ← A + M + C When T = 1 M(X) ← M(X) + M + C	When T = 0, this instruction adds the contents M, C, and A; and stores the results in A and C. When T = 1, this instruction adds the contents of M(X), M and C; and stores the results in M(X) and C. When T=1, the contents of A remain unchanged, but the contents of status flags are changed. M(X) represents the contents of memory where is indicated by X.				69	2	2							65	3	2			
AND (Note 1)	When T = 0 A ← A ∧ M When T = 1 M(X) ← M(X) ∧ M	When T = 0, this instruction transfers the contents of A and M to the ALU which performs a bit-wise AND operation and stores the result back in A. When T = 1, this instruction transfers the contents M(X) and M to the ALU which performs a bit-wise AND operation and stores the results back in M(X). When T = 1, the contents of A remain unchanged, but status flags are changed. M(X) represents the contents of memory where is indicated by X.				29	2	2							25	3	2			
ASL	7 0 C ← [ ] ← 0	This instruction shifts the content of A or M by one bit to the left, with bit 0 always being set to 0 and bit 7 of A or M always being contained in C.							0A	2	1				06	5	2			
BBC (Note 4)	Ai or Mi = 0?	This instruction tests the designated bit i of M or A and takes a branch if the bit is 0. The branch address is specified by a relative address. If the bit is 1, next instruction is executed.										13+20i	4	2				17+20i	5	3
BBS (Note 4)	Ai or Mi = 1?	This instruction tests the designated bit i of the M or A and takes a branch if the bit is 1. The branch address is specified by a relative address. If the bit is 0, next instruction is executed.										03+20i	4	2				07+20i	5	3
BCC (Note 4)	C = 0?	This instruction takes a branch to the appointed address if C is 0. The branch address is specified by a relative address. If C is 1, the next instruction is executed.																		
BCS (Note 4)	C = 1?	This instruction takes a branch to the appointed address if C is 1. The branch address is specified by a relative address. If C is 0, the next instruction is executed.																		
BEQ (Note 4)	Z = 1?	This instruction takes a branch to the appointed address when Z is 1. The branch address is specified by a relative address. If Z is 0, the next instruction is executed.																		
BIT	A ∧ M	This instruction takes a bit-wise logical AND of A and M contents; however, the contents of A and M are not modified. The contents of N, V, Z are changed, but the contents of A, M remain unchanged.													24	3	2			
BMI (Note 4)	N = 1?	This instruction takes a branch to the appointed address when N is 1. The branch address is specified by a relative address. If N is 0, the next instruction is executed.																		
BNE (Note 4)	Z = 0?	This instruction takes a branch to the appointed address if Z is 0. The branch address is specified by a relative address. If Z is 1, the next instruction is executed.																		

Symbol	ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0
	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
ADC	75	4	2				6D	4	3	7D	5	3	79	5	3							61	6	2	71	6	2							N	V	•	•	•	•	Z	C
AND	35	4	2				2D	4	3	3D	5	3	39	5	3							21	6	2	31	6	2							N	•	•	•	•	•	Z	•
ASL	16	6	2				0E	6	3	1E	7	3																						N	•	•	•	•	•	Z	C
BBC																																		•	•	•	•	•	•	•	•
BBS																																		•	•	•	•	•	•	•	•
BCC																												90	2	2				•	•	•	•	•	•	•	•
BCS																												B0	2	2				•	•	•	•	•	•	•	•
BEQ																												F0	2	2				•	•	•	•	•	•	•	•
BIT							2C	4	3																									M_7	M_6	•	•	•	•	Z	•
BMI																												30	2	2				•	•	•	•	•	•	•	•
BNE																												D0	2	2				•	•	•	•	•	•	•	•

APPENDIX
3.10 Machine instructions

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT, A			ZP			BIT, ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
BPL (Note 4)	N = 0?	This instruction takes a branch to the appointed address if N is 0. The branch address is specified by a relative address. If N is 1, the next instruction is executed.																		
BRA	PC ← PC ± offset	This instruction branches to the appointed address. The branch address is specified by a relative address.																		
BRK	B ← 1 (PC) ← (PC) + 2 M(S) ← PC_H S ← S – 1 M(S) ← PC_L S ← S – 1 M(S) ← PS S ← S – 1 I← 1 PC_L ← AD_L PC_H ← AD_H	When the BRK instruction is executed, the CPU pushes the current PC contents onto the stack. The BADRS designated in the interrupt vector table is stored into the PC.	00	7	1															
BVC (Note 4)	V = 0?	This instruction takes a branch to the appointed address if V is 0. The branch address is specified by a relative address. If V is 1, the next instruction is executed.																		
BVS (Note 4)	V = 1?	This instruction takes a branch to the appointed address when V is 1. The branch address is specified by a relative address. When V is 0, the next instruction is executed.																		
CLB	Ai or Mi ← 0	This instruction clears the designated bit i of A or M.										1B + 20i	2	1				1F + 20i	5	2
CLC	C ← 0	This instruction clears C.	18	2	1															
CLD	D ← 0	This instruction clears D.	D8	2	1															
CLI	I ← 0	This instruction clears I.	58	2	1															
CLT	T ← 0	This instruction clears T.	12	2	1															
CLV	V ← 0	This instruction clears V.	B8	2	1															
CMP (Note 3)	When T = 0 A – M When T = 1 M(X) – M	When T = 0, this instruction subtracts the contents of M from the contents of A. The result is not stored and the contents of A or M are not modified. When T = 1, the CMP subtracts the contents of M from the contents of M(X). The result is not stored and the contents of X, M, and A are not modified. M(X) represents the contents of memory where is indicated by X.				C9	2	2							C5	3	2			
COM	M ← $\overline{M}$	This instruction takes the one's complement of the contents of M and stores the result in M.													44	5	2			
CPX	X – M	This instruction subtracts the contents of M from the contents of X. The result is not stored and the contents of X and M are not modified.				E0	2	2							E4	3	2			
CPY	Y – M	This instruction subtracts the contents of M from the contents of Y. The result is not stored and the contents of Y and M are not modified.				C0	2	2							C4	3	2			
DEC	A ← A – 1 or M ← M – 1	This instruction subtracts 1 from the contents of A or M.							1A	2	1				C6	5	2			

Symbol	Addressing mode																																	Processor status register							
	ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0
	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
BPL																												10	2	2				•	•	•	•	•	•	•	•
BRA																												80	4	2				•	•	•	•	•	•	•	•
BRK																																		•	•	•	1	•	1	•	•
BVC																												50	2	2				•	•	•	•	•	•	•	•
BVS																												70	2	2				•	•	•	•	•	•	•	•
CLB																																		•	•	•	•	•	•	•	•
CLC																																		•	•	•	•	•	•	•	0
CLD																																		•	•	•	•	0	•	•	•
CLI																																		•	•	•	•	•	0	•	•
CLT																																		•	•	0	•	•	•	•	•
CLV																																		•	0	•	•	•	•	•	•
CMP	D5	4	2				CD	4	3	DD	5	3	D9	5	3							C1	6	2	D1	6	2							N	•	•	•	•	•	Z	C
COM																																		N	•	•	•	•	•	Z	•
CPX							EC	4	3																									N	•	•	•	•	•	Z	C
CPY							CC	4	3																									N	•	•	•	•	•	Z	C
DEC	D6	6	2				CE	6	3	DE	7	3																						N	•	•	•	•	•	Z	•

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT, A			ZP			BIT, ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
DEX	X ← X – 1	This instruction subtracts one from the current contents of X.	CA	2	1															
DEY	Y ← Y – 1	This instruction subtracts one from the current contents of Y.	88	2	1															
EOR (Note 1)	When T = 0 A ← A ∀ M When T = 1 M(X) ← M(X) ∀ M	When T = 0, this instruction transfers the contents of the M and A to the ALU which performs a bit-wise Exclusive OR, and stores the result in A. When T = 1, the contents of M(X) and M are transferred to the ALU, which performs a bit-wise Exclusive OR and stores the results in M(X). The contents of A remain unchanged, but status flags are changed. M(X) represents the contents of memory where is indicated by X.				49	2	2							45	3	2			
INC	A ← A + 1 or M ← M + 1	This instruction adds one to the contents of A or M.							3A	2	1				E6	5	2			
INX	X ← X + 1	This instruction adds one to the contents of X.	E8	2	1															
INY	Y ← Y + 1	This instruction adds one to the contents of Y.	C8	2	1															
JMP	If addressing mode is ABS PC_L ← AD_L PC_H ← AD_H If addressing mode is IND PC_L ← M (AD_H, AD_L) PC_H ← M (AD_H, AD_L + 1) If addressing mode is ZP, IND PC_L ← M(00, AD_L) PC_H ← M(00, AD_L + 1)	This instruction jumps to the address designated by the following three addressing modes: Absolute Indirect Absolute Zero Page Indirect Absolute																		
JSR	M(S) ← PC_H S ← S – 1 M(S) ← PC_L S ← S – 1 After executing the above, if addressing mode is ABS, PC_L ← AD_L PC_H ← AD_H if addressing mode is SP, PC_L ← AD_L PC_H ← FF If addressing mode is ZP, IND, PC_L ← M(00, AD_L) PC_H ← M(00, AD_L + 1)	This instruction stores the contents of the PC in the stack, then jumps to the address designated by the following addressing modes: Absolute Special Page Zero Page Indirect Absolute																		
LDA (Note 2)	When T = 0 A ← M When T = 1 M(X) ← M	When T = 0, this instruction transfers the contents of M to A. When T = 1, this instruction transfers the contents of M to (M(X)). The contents of A remain unchanged, but status flags are changed. M(X) represents the contents of memory where is indicated by X.				A9	2	2							A5	3	2			
LDM	M ← nn	This instruction loads the immediate value in M.													3C	4	3			
LDX	X ← M	This instruction loads the contents of M in X.				A2	2	2							A6	3	2			
LDY	Y ← M	This instruction loads the contents of M in Y.				A0	2	2							A4	3	2			

Symbol	Addressing mode																																	Processor status register							
	ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0
	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
DEX																																		N	•	•	•	•	•	Z	•
DEY																																		N	•	•	•	•	•	Z	•
EOR	55	4	2				4D	4	3	5D	5	3	59	5	3							41	6	2	51	6	2							N	•	•	•	•	•	Z	•
INC	F6	6	2				EE	6	3	FE	7	3																						N	•	•	•	•	•	Z	•
INX																																		N	•	•	•	•	•	Z	•
INY																																		N	•	•	•	•	•	Z	•
JMP							4C	3	3							6C	5	3	B2	4	2													•	•	•	•	•	•	•	•
JSR							20	6	3										02	7	2										22	5	2	•	•	•	•	•	•	•	•
LDA	B5	4	2				AD	4	3	BD	5	3	B9	5	3							A1	6	2	B1	6	2							N	•	•	•	•	•	Z	•
LDM																																		•	•	•	•	•	•	•	•
LDX				B6	4	2	AE	4	3				BE	5	3																			N	•	•	•	•	•	Z	•
LDY	B4	4	2				AC	4	3	BC	5	3																						N	•	•	•	•	•	Z	•

APPENDIX
3.10 Machine instructions

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT, A			ZP			BIT, ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
LSR	7 0 0 → □ → C	This instruction shifts either A or M one bit to the right such that bit 7 of the result always is set to 0, and the bit 0 is stored in C.							4A	2	1				46	5	2			
NOP	PC ← PC + 1	This instruction adds one to the PC but does no otheroperation.	EA	2	1															
ORA (Note 1)	When T = 0 A ← A V M When T = 1 M(X) ← M(X) V M	When T = 0, this instruction transfers the contents of A and M to the ALU which performs a bit-wise "OR", and stores the result in A. When T = 1, this instruction transfers the contents of M(X) and the M to the ALU which performs a bit-wise OR, and stores the result in M(X). The contents of A remain unchanged, but status flags are changed. M(X) represents the contents of memory where is indicated by X.				09	2	2							05	3	2			
PHA	S ← S – 1	This instruction pushes the contents of A to the memory location designated by S, and decrements the contents of S by one.	48	3	1															
PHP	M(S) ← PS S ← S – 1	This instruction pushes the contents of PS to the memory location designated by S and decrements the contents of S by one.	08	3	1															
PLA	S ← S + 1 A ← M(S)	This instruction increments S by one and stores the contents of the memory designated by S in A.	68	4	1															
PLP	S ← S + 1 PS ← M(S)	This instruction increments S by one and stores the contents of the memory location designated by S in PS.	28	4	1															
ROL	7 0 ← □ ← C ←	This instruction shifts either A or M one bit left through C. C is stored in bit 0 and bit 7 is stored in C.							2A	2	1				26	5	2			
ROR	7 0 C → □ →	This instruction shifts either A or M one bit right through C. C is stored in bit 7 and bit 0 is stored in C.							6A	2	1				66	5	2			
RRF	7 0 → □ →	This instruction rotates 4 bits of the M content to the right.													82	8	2			
RTI	S ← S + 1 PS ← M(S) S ← S + 1 PC_L ← M(S) S ← S + 1 PC_H ← M(S)	This instruction increments S by one, and stores the contents of the memory location designated by S in PS. S is again incremented by one and stores the contents of the memory location designated by S in PC_L. S is again incremented by one and stores the contents of memory location designated by S in PC_H.	40	6	1															
RTS	S ← S + 1 PC_L ← M(S) S ← S + 1 PC_H ← M(S) (PC) ← (PC) + 1	This instruction increments S by one and stores the contents of the memory location designated by S in PC_L. S is again incremented by one and the contents of the memory location is stored in PC_H. PC is incremented by 1.	60	6	1															

Symbol	Addressing mode																																Processor status register							
	ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0
	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
LSR	56	6	2				4E	6	3	5E	7	3																						0	•	•	•	•	•	Z	C
NOP																																		•	•	•	•	•	•	•	•
ORA	15	4	2				0D	4	3	1D	5	3	19	5	3							01	6	2	11	6	2							N	•	•	•	•	•	Z	•
PHA																																		•	•	•	•	•	•	•	•
PHP																																		•	•	•	•	•	•	•	•
PLA																																		N	•	•	•	•	•	Z	•
PLP																																		(Value saved in stack)							
ROL	36	6	2				2E	6	3	3E	7	3																						N	•	•	•	•	•	Z	C
ROR	76	6	2				6E	6	3	7E	7	3																						N	•	•	•	•	•	Z	C
RRF																																		•	•	•	•	•	•	•	•
RTI																																		(Value saved in stack)							
RTS																																		•	•	•	•	•	•	•	•

Symbol	Function	Details	Addressing mode: IMP			IMM			A			BIT, A			ZP			BIT, ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
SBC (Note 1) (Note 5)	When T = 0 $A \leftarrow A - M - \overline{C}$ When T = 1 $M(X) \leftarrow M(X) - M - \overline{C}$	When T = 0, this instruction subtracts the value of M and the complement of C from A, and stores the results in A and C. When T = 1, the instruction subtracts the contents of M and the complement of C from the contents of M(X), and stores the results in M(X) and C. A remain unchanged, but status flag are changed. M(X) represents the contents of memory where is indicated by X.				E9	2	2							E5	3	2			
SEB	Ai or Mi ← 1	This instruction sets the designated bit i of A or M.										0B + 20i	2	1				0F + 20i	5	2
SEC	C ← 1	This instruction sets C.	38	2	1															
SED	D ← 1	This instruction set D.	F8	2	1															
SEI	I ← 1	This instruction set I.	78	2	1															
SET	T ← 1	This instruction set T.	32	2	1															
STA	M ← A	This instruction stores the contents of A in M. The contents of A does not change.													85	4	2			
STP		This instruction resets the oscillation control F/F and the oscillation stops. Reset or interrupt input is needed to wake up from this mode.	42	2	1															
STX	M ← X	This instruction stores the contents of X in M. The contents of X does not change.													86	4	2			
STY	M ← Y	This instruction stores the contents of Y in M. The contents of Y does not change.													84	4	2			
TAX	X ← A	This instruction stores the contents of A in X. The contents of A does not change.	AA	2	1															
TAY	Y ← A	This instruction stores the contents of A in Y. The contents of A does not change.	A8	2	1															
TST	M = 0?	This instruction tests whether the contents of M are “0” or not and modifies the N and Z.													64	3	2			
TSX	X ← S	This instruction transfers the contents of S in X.	BA	2	1															
TXA	A ← X	This instruction stores the contents of X in A.	8A	2	1															
TXS	S ← X	This instruction stores the contents of X in S.	9A	2	1															
TYA	A ← Y	This instruction stores the contents of Y in A.	98	2	1															
WIT		The WIT instruction stops the internal clock but not the oscillation of the oscillation circuit is not stopped. CPU starts its function after the Timer X over flows (comes to the terminal count). All registers or internal memory contents except Timer X will not change during this mode. (Of course needs VDD).	C2	2	1															

Notes 1 : The number of cycles “n” is increased by 3 when T is 1.
2 : The number of cycles “n” is increased by 2 when T is 1.
3 : The number of cycles “n” is increased by 1 when T is 1.
4 : The number of cycles “n” is increased by 2 when branching has occurred.
5 : N, V, and Z flags are invalid in decimal operation mode.

Symbol	Addressing mode: ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			Processor status register: 7	6	5	4	3	2	1	0
	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
SBC	F5	4	2				ED	4	3	FD	5	3	F9	5	3							E1	6	2	F1	6	2							N	V	•	•	•	•	Z	C
SEB																																		•	•	•	•	•	•	•	•
SEC																																		•	•	•	•	•	•	•	1
SED																																		•	•	•	•	1	•	•	•
SEI																																		•	•	•	•	•	1	•	•
SET																																		•	•	1	•	•	•	•	•
STA	95	5	2				8D	5	3	9D	6	3	99	6	3							81	7	2	91	7	2							•	•	•	•	•	•	•	•
STP																																		•	•	•	•	•	•	•	•
STX				96	5	2	8E	5	3																									•	•	•	•	•	•	•	•
STY	94	5	2				8C	5	3																									•	•	•	•	•	•	•	•
TAX																																		N	•	•	•	•	•	Z	•
TAY																																		N	•	•	•	•	•	Z	•
TST																																		N	•	•	•	•	•	Z	•
TSX																																		N	•	•	•	•	•	Z	•
TXA																																		N	•	•	•	•	•	Z	•
TXS																																		•	•	•	•	•	•	•	•
TYA																																		N	•	•	•	•	•	Z	•
WIT																																		•	•	•	•	•	•	•	•

3.10 Machine instructions

Symbol	Contents	Symbol	Contents
IMP	Implied addressing mode	+	Addition
IMM	Immediate addressing mode	–	Subtraction
A	Accumulator or Accumulator addressing mode	Λ	Logical OR
BIT, A	Accumulator bit addressing mode	V	Logical AND
BIT, A, R	Accumulator bit relative addressing mode	∀	Logical exclusive OR
ZP	Zero page addressing mode	—	Negation
BIT, ZP	Zero page bit addressing mode	←	Shows direction of data flow
BIT, ZP, R	Zero page bit relative addressing mode	X	Index register X
ZP, X	Zero page X addressing mode	Y	Index register Y
ZP, Y	Zero page Y addressing mode	S	Stack pointer
ABS	Absolute addressing mode	PC	Program counter
ABS, X	Absolute X addressing mode	PS	Processor status register
ABS, Y	Absolute Y addressing mode	PC_H	8 high-order bits of program counter
IND	Indirect absolute addressing mode	PC_L	8 low-order bits of program counter
		AD_H	8 high-order bits of address
ZP, IND	Zero page indirect absolute addressing mode	AD_L	8 low-order bits of address
		FF	FF in Hexadecimal notation
IND, X	Indirect X addressing mode	nn	Immediate value
IND, Y	Indirect Y addressing mode	zz	Zero page address
REL	Relative addressing mode	M	Memory specified by address designation of any addressing mode
SP	Special page addressing mode		
C	Carry flag	M(X)	Memory of address indicated by contents of index register X
Z	Zero flag		
I	Interrupt disable flag	M(S)	Memory of address indicated by contents of stack pointer
D	Decimal mode flag		
B	Break flag	M(AD_H, AD_L)	Contents of memory at address indicated by AD_H and AD_L, in AD_H is 8 high-order bits and AD_L is 8 low-order bits.
T	X-modified arithmetic mode flag		
V	Overflow flag		
N	Negative flag	M(00, AD_L)	Contents of address indicated by zero page AD_L
		Ai	Bit i (i = 0 to 7) of accumulator
		Mi	Bit i (i = 0 to 7) of memory
		OP	Opcode
		n	Number of cycles
		#	Number of bytes

3.11 List of instruction code

D_7 – D_4	D_3 – D_0 / Hexadecimal notation	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	BRK	ORA IND, X	JSR ZP, IND	BBS 0, A	—	ORA ZP	ASL ZP	BBS 0, ZP	PHP	ORA IMM	ASL A	SEB 0, A	—	ORA ABS	ASL ABS	SEB 0, ZP
0001	1	BPL	ORA IND, Y	CLT	BBC 0, A	—	ORA ZP, X	ASL ZP, X	BBC 0, ZP	CLC	ORA ABS, Y	DEC A	CLB 0, A	—	ORA ABS, X	ASL ABS, X	CLB 0, ZP
0010	2	JSR ABS	AND IND, X	JSR SP	BBS 1, A	BIT ZP	AND ZP	ROL ZP	BBS 1, ZP	PLP	AND IMM	ROL A	SEB 1, A	BIT ABS	AND ABS	ROL ABS	SEB 1, ZP
0011	3	BMI	AND IND, Y	SET	BBC 1, A	—	AND ZP, X	ROL ZP, X	BBC 1, ZP	SEC	AND ABS, Y	INC A	CLB 1, A	LDM ZP	AND ABS, X	ROL ABS, X	CLB 1, ZP
0100	4	RTI	EOR IND, X	STP	BBS 2, A	COM ZP	EOR ZP	LSR ZP	BBS 2, ZP	PHA	EOR IMM	LSR A	SEB 2, A	JMP ABS	EOR ABS	LSR ABS	SEB 2, ZP
0101	5	BVC	EOR IND, Y	—	BBC 2, A	—	EOR ZP, X	LSR ZP, X	BBC 2, ZP	CLI	EOR ABS, Y	—	CLB 2, A	—	EOR ABS, X	LSR ABS, X	CLB 2, ZP
0110	6	RTS	ADC IND, X	—	BBS 3, A	TST ZP	ADC ZP	ROR ZP	BBS 3, ZP	PLA	ADC IMM	ROR A	SEB 3, A	JMP IND	ADC ABS	ROR ABS	SEB 3, ZP
0111	7	BVS	ADC IND, Y	—	BBC 3, A	—	ADC ZP, X	ROR ZP, X	BBC 3, ZP	SEI	ADC ABS, Y	—	CLB 3, A	—	ADC ABS, X	ROR ABS, X	CLB 3, ZP
1000	8	BRA	STA IND, X	RRF ZP	BBS 4, A	STY ZP	STA ZP	STX ZP	BBS 4, ZP	DEY	—	TXA	SEB 4, A	STY ABS	STA ABS	STX ABS	SEB 4, ZP
1001	9	BCC	STA IND, Y	—	BBC 4, A	STY ZP, X	STA ZP, X	STX ZP, Y	BBC 4, ZP	TYA	STA ABS, Y	TXS	CLB 4, A	—	STA ABS, X	—	CLB 4, ZP
1010	A	LDY IMM	LDA IND, X	LDX IMM	BBS 5, A	LDY ZP	LDA ZP	LDX ZP	BBS 5, ZP	TAY	LDA IMM	TAX	SEB 5, A	LDY ABS	LDA ABS	LDX ABS	SEB 5, ZP
1011	B	BCS	LDA IND, Y	JMP ZP, IND	BBC 5, A	LDY ZP, X	LDA ZP, X	LDX ZP, Y	BBC 5, ZP	CLV	LDA ABS, Y	TSX	CLB 5, A	LDY ABS, X	LDA ABS, X	LDX ABS, Y	CLB 5, ZP
1100	C	CPY IMM	CMP IND, X	WIT	BBS 6, A	CPY ZP	CMP ZP	DEC ZP	BBS 6, ZP	INY	CMP IMM	DEX	SEB 6, A	CPY ABS	CMP ABS	DEC ABS	SEB 6, ZP
1101	D	BNE	CMP IND, Y	—	BBC 6, A	—	CMP ZP, X	DEC ZP, X	BBC 6, ZP	CLD	CMP ABS, Y	—	CLB 6, A	—	CMP ABS, X	DEC ABS, X	CLB 6, ZP
1110	E	CPX IMM	SBC IND, X	—	BBS 7, A	CPX ZP	SBC ZP	INC ZP	BBS 7, ZP	INX	SBC IMM	NOP	SEB 7, A	CPX ABS	SBC ABS	INC ABS	SEB 7, ZP
1111	F	BEQ	SBC IND, Y	—	BBC 7, A	—	SBC ZP, X	INC ZP, X	BBC 7, ZP	SED	SBC ABS, Y	—	CLB 7, A	—	SBC ABS, X	INC ABS, X	CLB 7, ZP

: 3-byte instruction

: 2-byte instruction

: 1-byte instruction

3.12 SFR memory map

Address	Register	Address	Register
0000_{16}	Port P0 (P0)	0020_{16}	
0001_{16}	Port P0 direction register (P0D)	0021_{16}	
0002_{16}	Port P1 (P1)	0022_{16}	
0003_{16}	Port P1 direction register (P1D)	0023_{16}	
0004_{16}	Port P2 (P2)	0024_{16}	
0005_{16}	Port P2 direction register (P2D)	0025_{16}	
0006_{16}	Port P3 (P3)	0026_{16}	
0007_{16}	Port P3 direction register (P3D)	0027_{16}	
0008_{16}		0028_{16}	Prescaler 12 (PRE12)
0009_{16}		0029_{16}	Timer 1 (T1)
$000A_{16}$		$002A_{16}$	Timer 2 (T2)
$000B_{16}$		$002B_{16}$	Timer X mode register (TM)
$000C_{16}$		$002C_{16}$	Prescaler X (PREX)
$000D_{16}$		$002D_{16}$	Timer X (TX)
$000E_{16}$		$002E_{16}$	Timer count source setting register (TCSS)
$000F_{16}$		$002F_{16}$	
0010_{16}		0030_{16}	Serial I/O2 control register (SIO2CON)
0011_{16}		0031_{16}	Serial I/O2 register (SIO2)
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	A-D control register (ADCON)
0015_{16}		0035_{16}	A-D conversion register (low-order) (ADL)
0016_{16}	Pull-up control register (PULL)	0036_{16}	A-D conversion register (high-order) (ADH)
0017_{16}	Port P1P3 control register (P1P3C)	0037_{16}	
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	MISRG
0019_{16}	Serial I/O1 status register (SIO1STS)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$		$003D_{16}$	
$001E_{16}$		$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$		$003F_{16}$	

3.13 Pin configurations

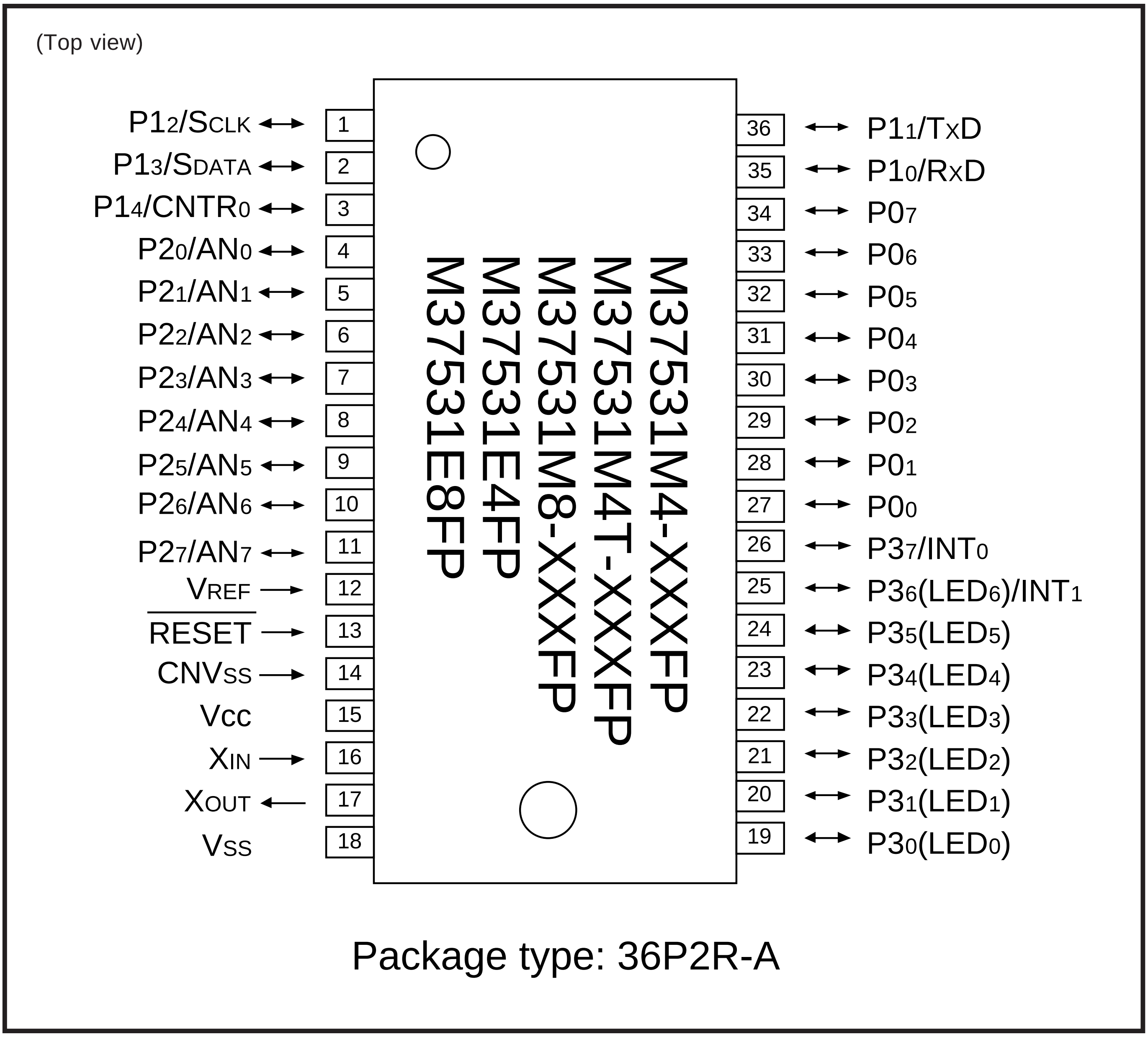


Fig. 3.13.1 Pin configuration (36P2R package type)

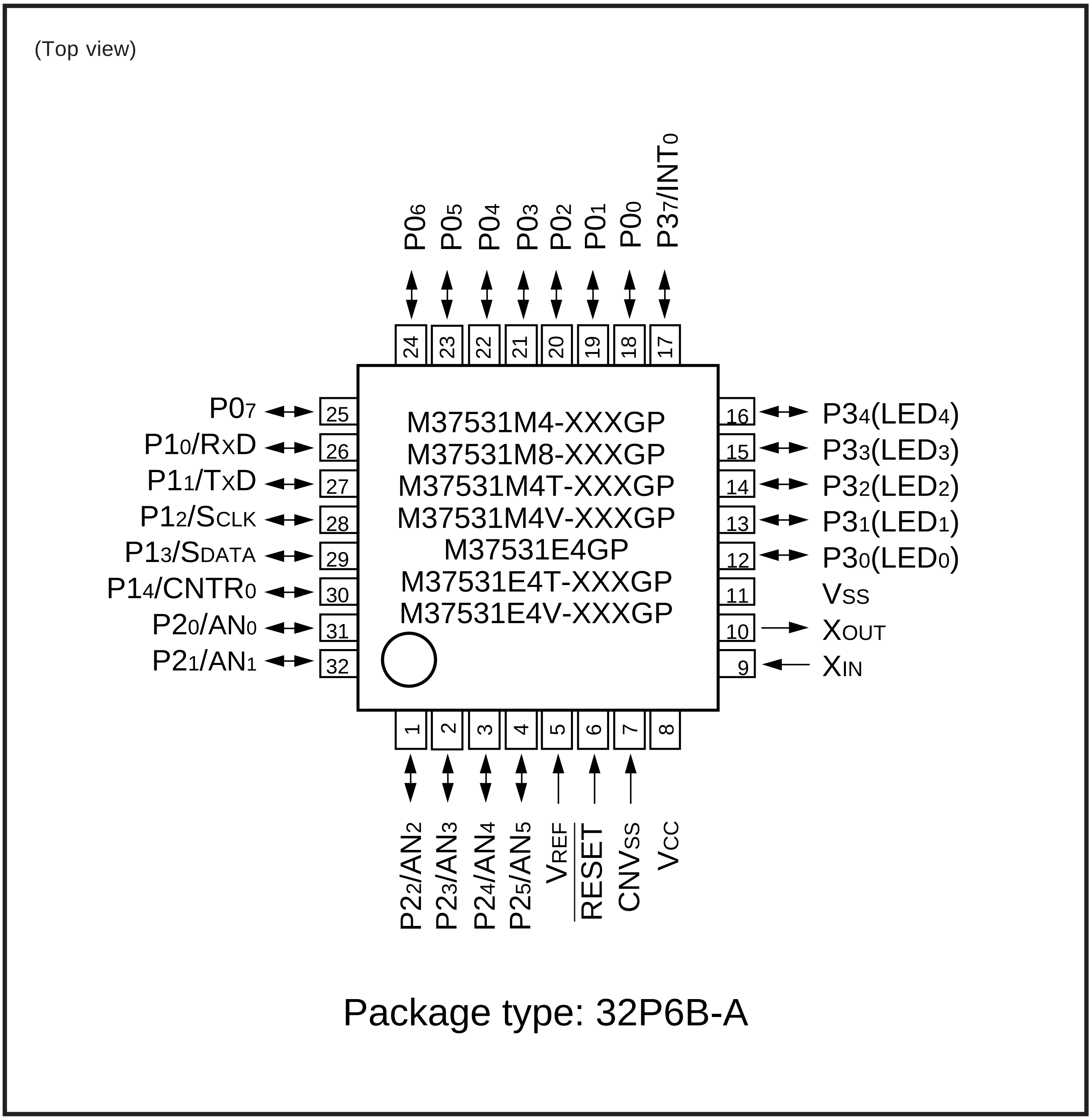


Fig. 3.13.2 Pin configuration (32P6B package type)

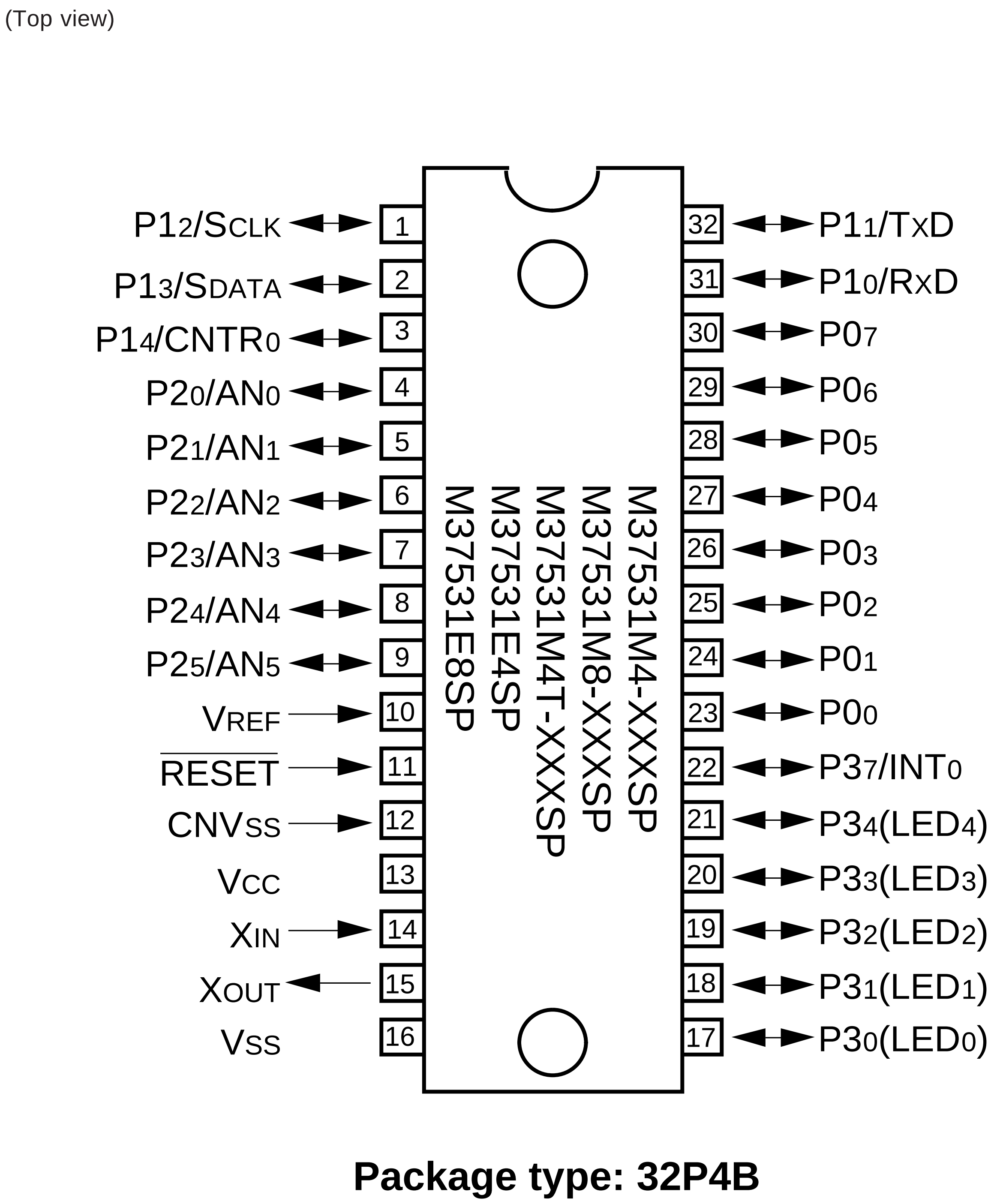


Fig. 3.13.3 Pin configuration (32P4B package type)

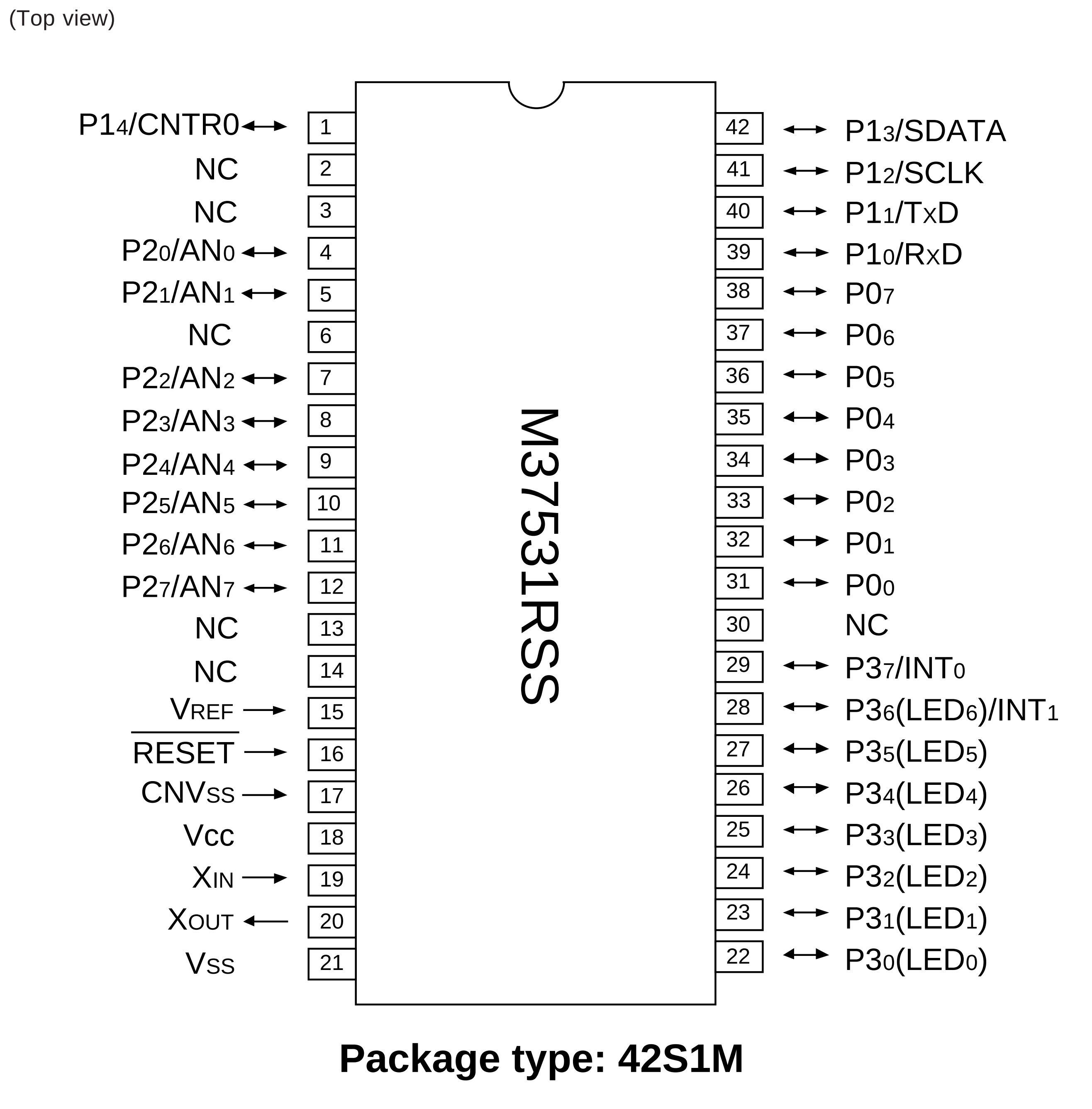


Fig. 3.13.4 M37531RSS pin configuration

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