

MITSUBISHI 8-BIT SINGLE-CHIP MICROCOMPUTER
740 FAMILY / 38000 SERIES

3819

User's Manual

Group



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Preface

This user's manual describes Mitsubishi's CMOS 8-bit microcomputers 3819 Group.

After reading this manual, the user should have a thorough knowledge of the functions and features of the 3819 Group, and should be able to fully utilize the product. The manual starts with specifications and ends with application examples.

For details of software, refer to the "740 Family Software MANUAL".

BEFORE USING THIS USER'S MANUAL

This user's manual consists of the following three chapters. Refer to the chapter appropriate to your conditions, such as hardware design or software development.

1. Organization

● CHAPTER 1 HARDWARE

This chapter describes features of the microcomputer, operation of each peripheral function and electric characteristics.

● CHAPTER 2 APPLICATION

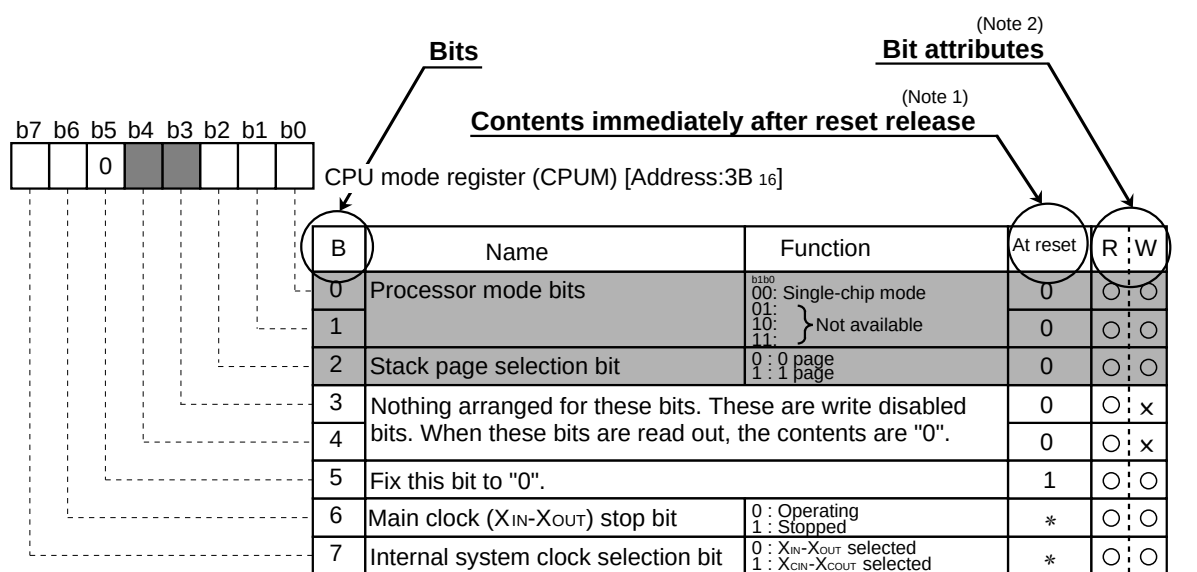
This chapter describes usage and application examples of peripheral functions, based mainly on setting examples of related registers.

● CHAPTER 3 APPENDIX

This chapter includes precautions for systems development using the microcomputer, a list of control registers, the masking confirmation (mask ROM version), and mark specifications which are to be submitted when ordering.

2. Structure of register

The figure of each register structure describes its functions, contents at reset, and attributes as follows :



■ : Bit in which nothing is arranged

■ : Bit that is not used for control of the corresponding function

Note 1. Contents immediately after reset release

0....."0" at reset release

1....."1" at reset release

Undefined.....Undefined or reset release

*.....Contents determined by option at reset release (D) Note

Note 2. Bit attributes.....The attributes of control register bits are classified into 3 bytes : read-only, write-only and read and write. In the figure, these attributes are represented as follows :

R.....Read

○.....Read enabled

x.....Read disabled

W.....Write

○.....Write enabled

x.....Write disabled

*....."0" write

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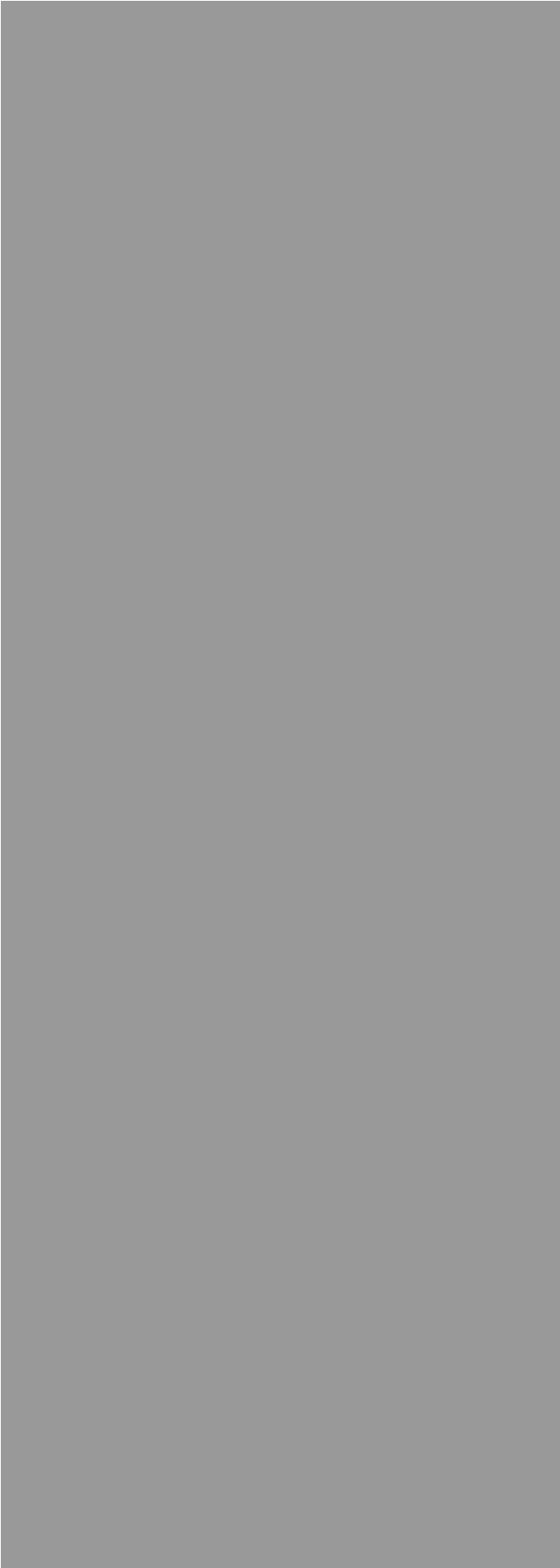
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CHAPTER 1

HARDWARE

3819 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 3819 group is a 8-bit microcomputer based on the 740 family core technology.

The 3819 group has a fluorescent display automatic display circuit and an 16-channel 8-bit A-D converter as additional functions.

The various microcomputers in the 3819 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 3819 group, refer to the section on group expansion.

FEATURES

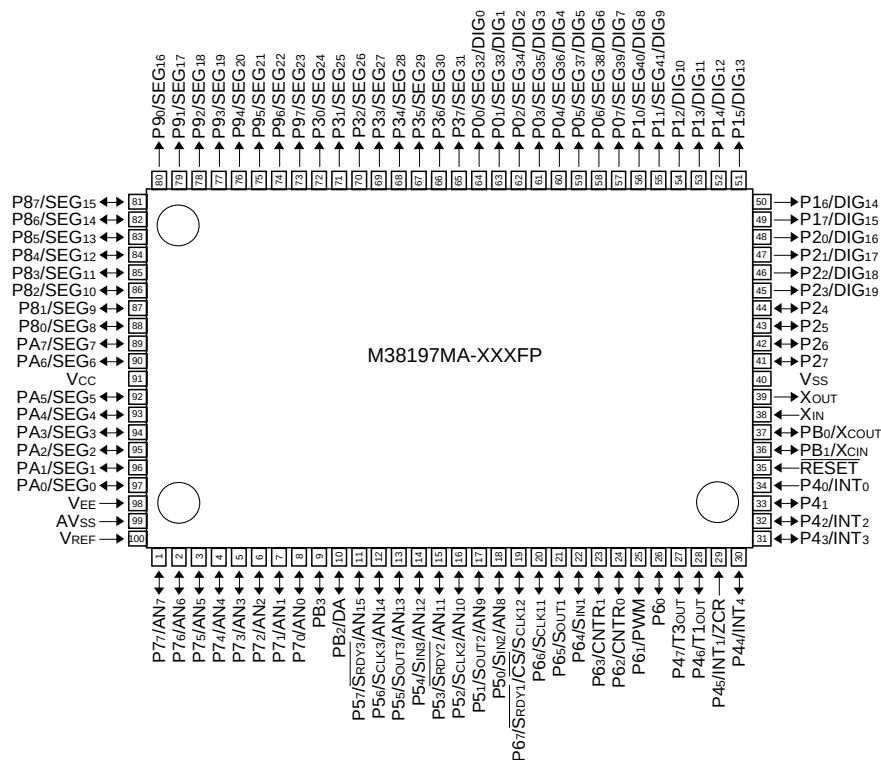
- Basic machine-language instructions 71
- The minimum instruction execution time 0.48 μ s
(at 8.4 MHz oscillation frequency)
- Memory size
 - ROM 4K to 60 K bytes
 - RAM 192 to 2048 bytes
- Programmable input/output ports 54
- High-breakdown-voltage output ports 52
- Interrupts 20 sources, 16 vectors
- Timers 8-bit X 6
- Serial I/O (Serial I/O1 has an automatic transfer function)
 - 8-bit X 3(clock-synchronized)
- PWM output circuit 8-bit X 1(also functions as timer 6)
- A-D converter 8-bit X 16 channels

- D-A converter 8-bit X 1 channels
- Zero cross detection input 1 channel
- Fluorescent display function
 - Segments 16 to 42
 - Digits 6 to 16
- 2 Clock generating circuit
 - Clock (XIN-XOUT) Internal feedback resistor
 - Sub-clock (XCIN-XCOUT) Without internal feedback resistor
(connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
 - In high-speed mode 4.0 to 5.5 V
(at 8.4 MHz oscillation frequency and high-speed selected)
 - In middle-speed mode 2.8 to 5.5 V
(at 8.4 MHz oscillation frequency)
 - In low-speed mode 2.8 to 5.5 V
(at 32 kHz oscillation frequency)
- Power dissipation
 - In high-speed mode 35 mW
(at 8.4 MHz oscillation frequency)
 - In low-speed mode 60 μ W
(at 3 V power source voltage and 32 kHz oscillation frequency)
- Operating temperature range -10 to 85°C

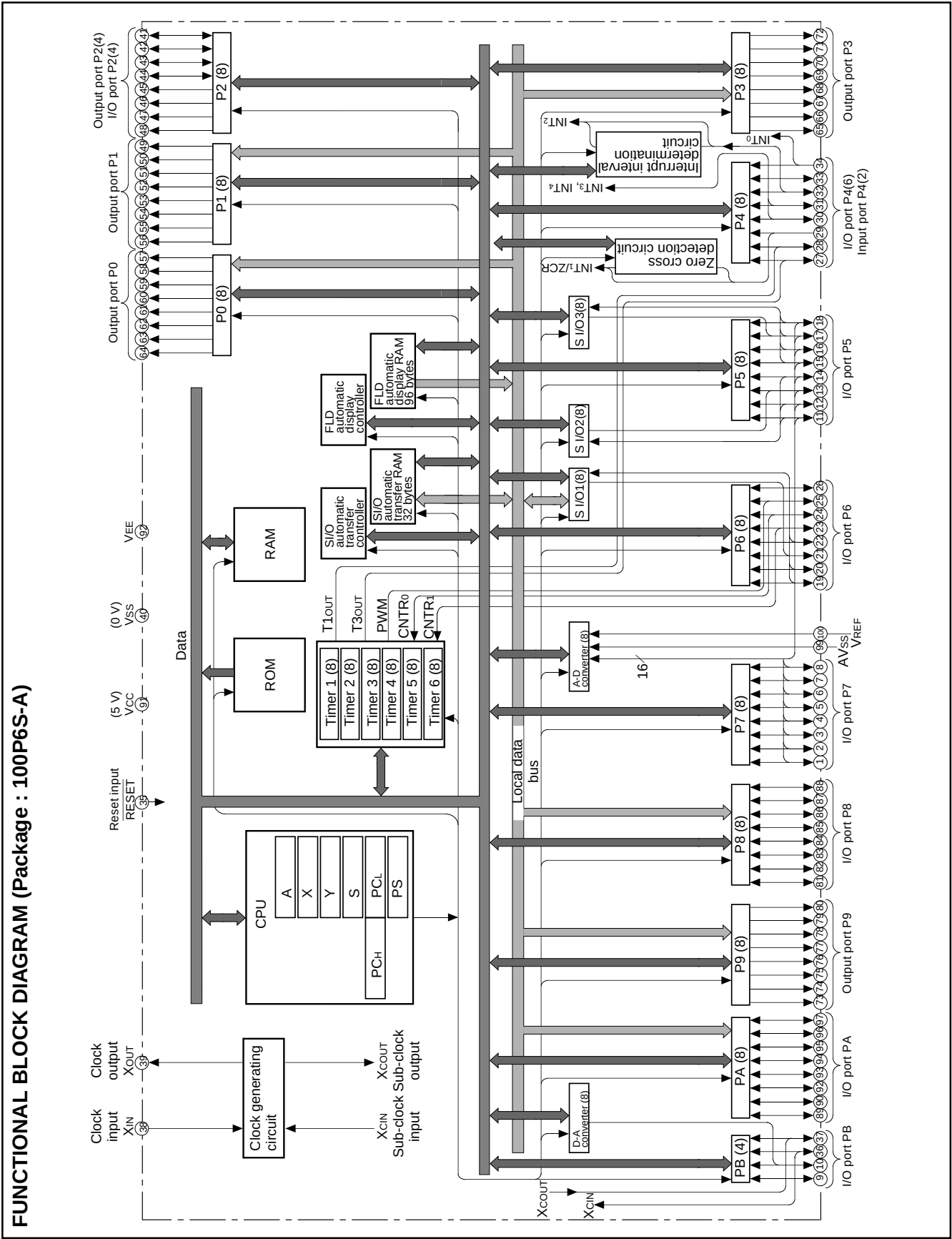
APPLICATION

Musical Instruments, household appliance, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : 100P6S-A
100-pin plastic-molded QFP



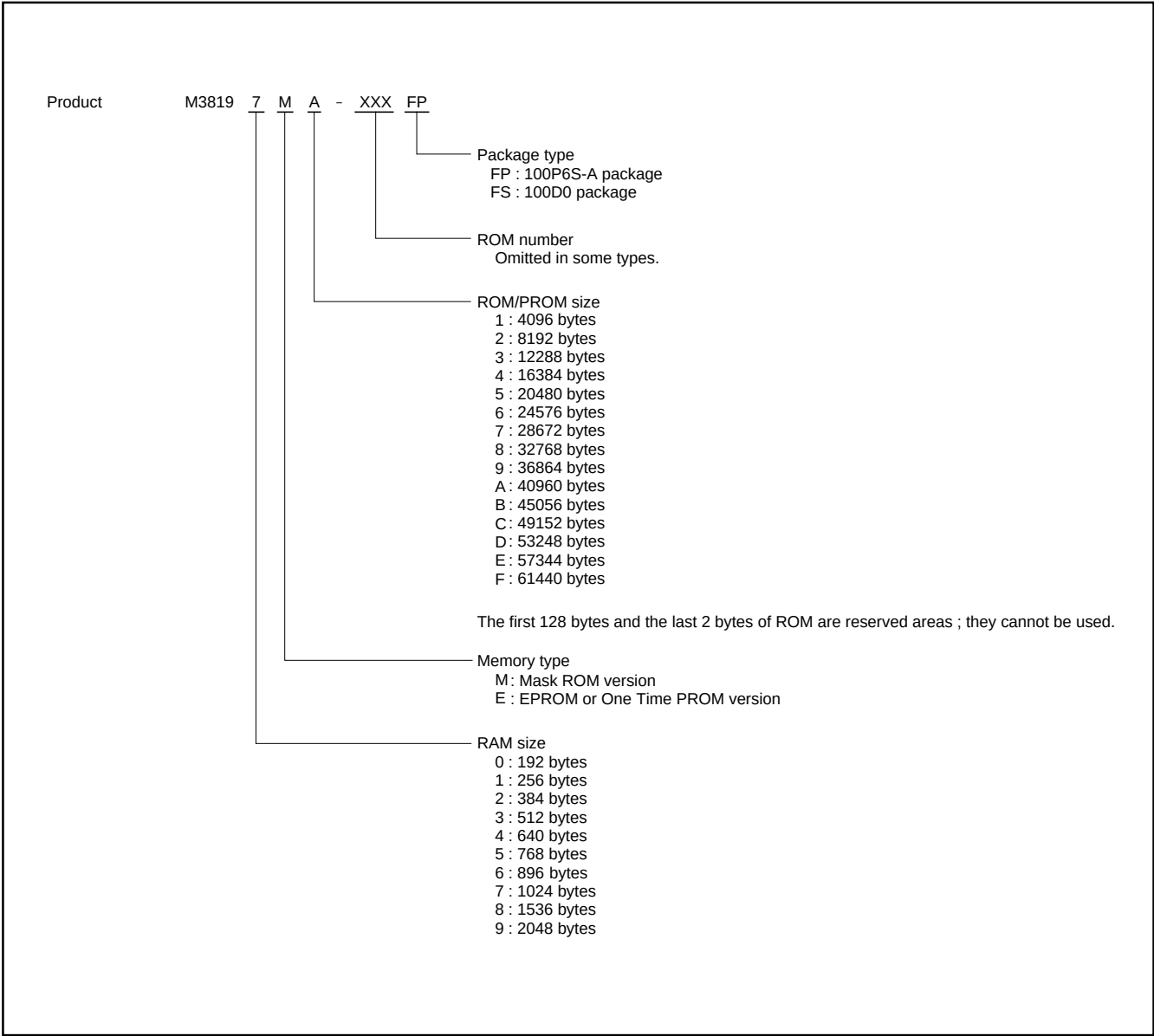
PIN DESCRIPTION

Pin	Name	Function	Function except a port function
VCC, VSS	Power source	•Apply voltage of 4.0 to 5.5 V to Vcc, and 0 V to Vss.	
VEE	Pull-down Power source	•Applies voltage supplied to pull-down resistors of ports P0, P1, P20–P23, P3, and P9.	
VREF	Analog reference voltage	•Reference voltage input pin for A-D converter and D-A converter	
AVSS	Analog power source	•GND input pin for A-D converter and D-A converter •Connect AVss to Vss.	
RESET	Reset input	•Reset input pin for active “L”	
XIN	Clock input	•Input and output pins for the main clock generating circuit •Feedback resistor is built in between XIN pin and XOUT pin. •Connect a ceramic resonator or a quartz-crystal oscillator between the XIN pin and XOUT pin to set oscillation frequency. •If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. •This clock is used as the oscillating source of system clock.	
XOUT	Clock output		
P00/SEG32/ DIG0–P07/ SEG39/DIG7	Output port P0	•8-bit output port •This port builds in pull-down resistor between port P0 and the VEE pin. •At reset this port is set to VEE level. •The high-breakdown-voltage P-channel open-drain	FLD automatic display pins
P10/SEG40/ DIG8–P17/ DIG15	Output port P1	•8-bit output port with the same function as port P0	FLD automatic display pins
P20/DIG16– P23/DIG19	Output port P2	•4-bit output port with the same function as port P0	FLD automatic display pins
P24–P27	I/O port P2	•4-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •At reset this port is set to input mode. •TTL input level •CMOS 3-state output	
P30/SEG24– P37/SEG31	Output port P3	•8-bit output port with the same function as port P0	FLD automatic display pins
P40/INT0, P45/INT1/ ZCR	Input port P4	•2-bit input port •CMOS compatible input level	External interrupt input pins A zero cross detection circuit input pin (P45)
P42/INT2– P44/INT4	I/O port P4	•6-bit CMOS I/O port with the same function as ports P24–P27 •CMOS compatible input level •CMOS 3-state output	
P41			
P46/T1OUT, P47/T3OUT		Timer output pins	

PIN DESCRIPTION (Continued)

Pin	Name	Function	Function except a port function
P50/SIN2/AN8, P51/SOUT2/AN9, P52/SCLK2/AN10, P53/SRDY2/AN11	I/O port P5	•8-bit CMOS I/O port with the same function as ports P24–P27 •CMOS compatible input level •CMOS 3-state output	Serial I/O2 function pins A-D conversion input pins
P54/SIN3/AN12, P55/SOUT3/AN13, P56/SCLK3/AN14, P57/SRDY3/AN15			Serial I/O3 function pins A-D conversion input pins
P60	I/O port P6	•8-bit CMOS I/O port with the same function as ports P24–P47 •CMOS compatible input level •CMOS 3-state output	
P61/PWM			PWM output pin (Timer output pin)
P62/CNTR0, P63/CNTR1			Timer input pins
P64/SIN1, P65/SOUT1, P66/SCLK11, P67/SRDY1/CS/ SCLK12			Serial I/O1 function pins
P70/AN0– P77/AN7	I/O port P7	•8-bit CMOS I/O port with the same function as ports P24–P27 •CMOS compatible input level •CMOS 3-state output	A-D conversion input pins
P80/SEG8– P87/SEG15	I/O port P8	•8-bit I/O port with the same function as ports P24–P27 •CMOS compatible input level •The high-breakdown-voltage P-channel open-drain	FLD automatic display pins
P90/SEG16– P97/SEG23	Output port P9	•8-bit output port with the same function as port P0	
PA0/SEG0– PA7/SEG7	I/O port PA	•8-bit I/O port with the same function as ports P24–P27 •CMOS compatible input level •The high-breakdown voltage P-channel open-drain	
PB0/XCOUT, PB1/XCIN	I/O port PB	•4-bit CMOS I/O port with the same function as ports P24–P27 •CMOS compatible input level •CMOS 3-state output	I/O pins for sub-clock generating circuit (connect a ceramic resonator or a quartz-crystal oscillator)
PB2/DA			D-A conversion output pin
PB3			

PART NUMBERING



GROUP EXPANSION

Mitsubishi plans to expand the 3819 group as follows:

(1) Support for mask ROM, One Time PROM, and EPROM versions

ROM/PROM capacity 40 K to 60 K bytes

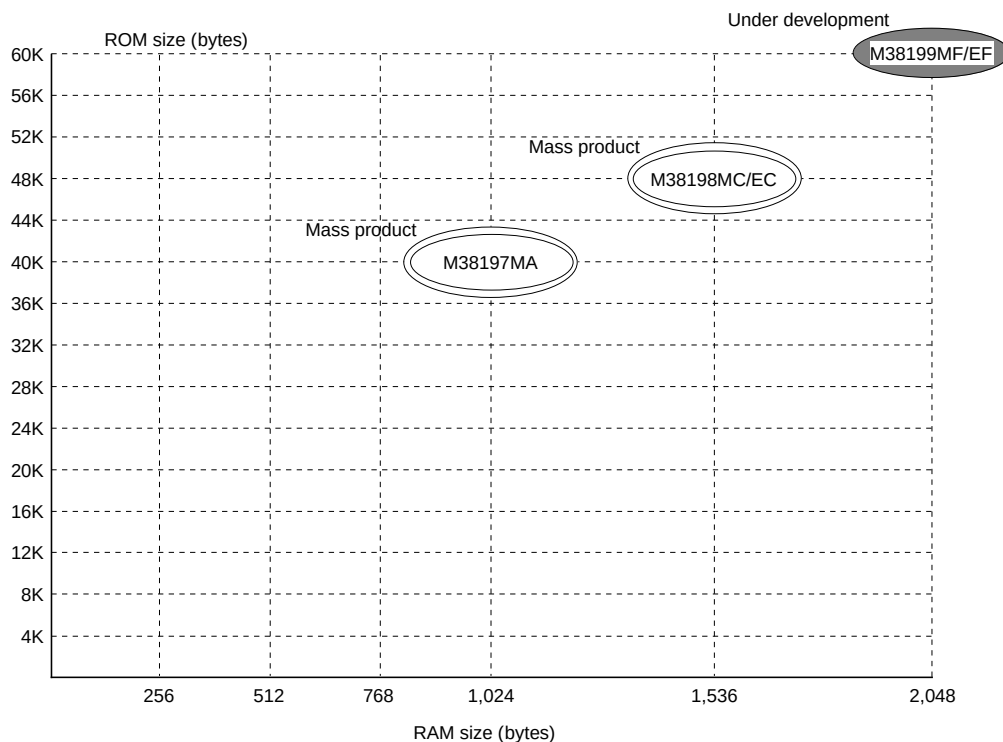
RAM capacity 1024 to 2048 bytes

(2) Packages

100P6S-A 0.65 mm-pitch plastic molded QFP

100D0 Ceramic LCC(built-in EPROM version)

Memory Expansion Plan



Products under development : the development schedule and specifications may be revised without notice.

Currently supported products are listed below.

As of May 1996

Product	(P) ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38197MA-XXXFP	40960 (40830)	1024	100P6S-A	Mask ROM version
M38197MA-XXXKP			100P6P-E	Mask ROM version
M38198MC-XXXKP				Mask ROM version
M38199MF-XXXKP				Mask ROM version
M38198MC-XXXFP	49152 (49022)	1536	100P6S-A	Mask ROM version
M38198EC-XXXFP				One Time PROM version
M38198ECFP				One Time PROM version (blank)
M38198ECFS			100D0	EPROM version
M38199MF-XXXFP	61440 (61310)	2048	100P6S-A	Mask ROM version
M38199EF-XXXFP				One Time PROM version
M38199EFP				One Time PROM version (blank)
M38199EFP			100D0	EPROM version

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The 3819 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST, SLW instruction cannot be used.

The MUL, DIV, WIT and STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated at address 003B₁₆. The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

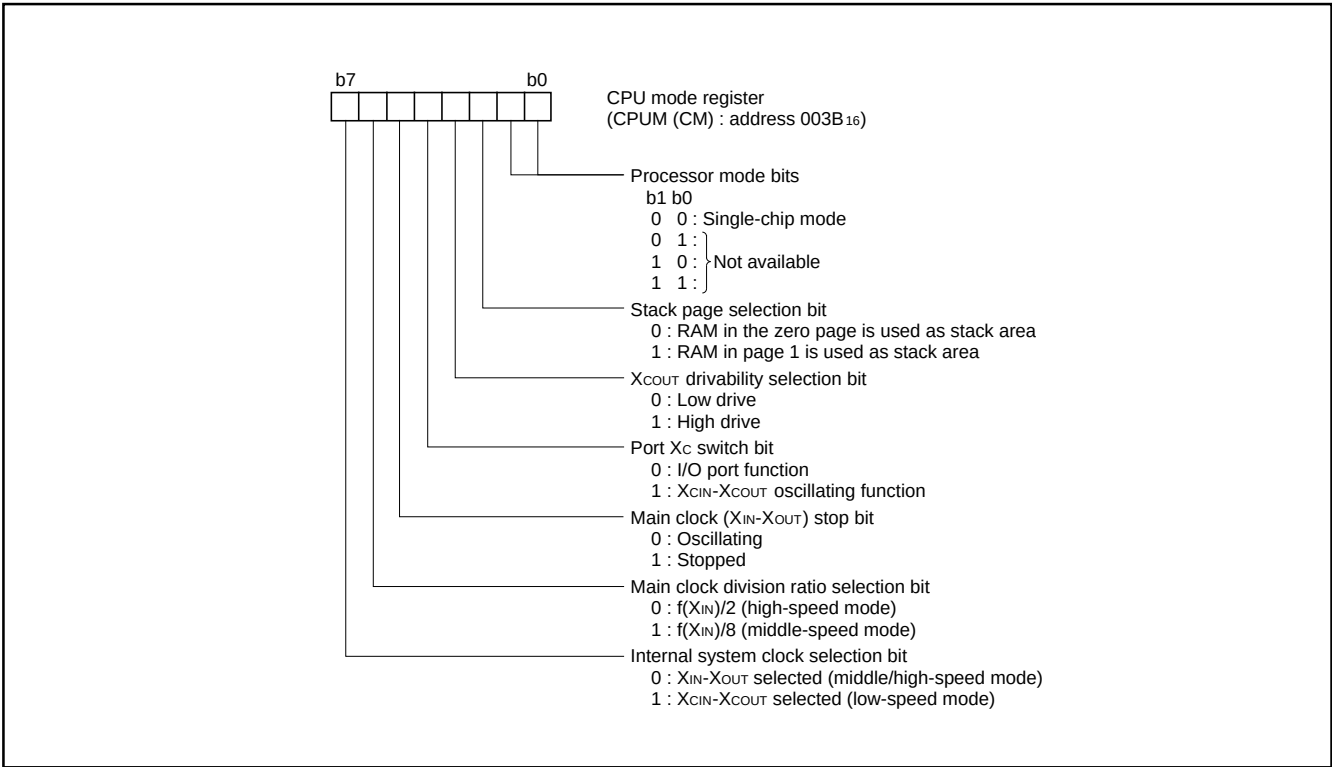


Fig. 1 Structure of CPU mode register

Memory

Special function register (SFR) area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the reset is user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000₁₆ to 00FF₁₆ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses FF00₁₆ to FFFF₁₆ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM capacity (bytes)	Address XXXX ₁₆
192	00FF ₁₆
256	013F ₁₆
384	01BF ₁₆
512	023F ₁₆
640	02BF ₁₆
768	033F ₁₆
896	03BF ₁₆
1024	043F ₁₆
1536	063F ₁₆
2048	083F ₁₆

ROM area

ROM capacity (bytes)	Address YYYY ₁₆	Address ZZZZ ₁₆
4096	F000 ₁₆	F080 ₁₆
8192	E000 ₁₆	E080 ₁₆
12288	D000 ₁₆	D080 ₁₆
16384	C000 ₁₆	C080 ₁₆
20480	B000 ₁₆	B080 ₁₆
24576	A000 ₁₆	A080 ₁₆
28672	9000 ₁₆	9080 ₁₆
32768	8000 ₁₆	8080 ₁₆
36864	7000 ₁₆	7080 ₁₆
40960	6000 ₁₆	6080 ₁₆
45056	5000 ₁₆	5080 ₁₆
49152	4000 ₁₆	4080 ₁₆
53248	3000 ₁₆	3080 ₁₆
57344	2000 ₁₆	2080 ₁₆
61440	1000 ₁₆	1080 ₁₆

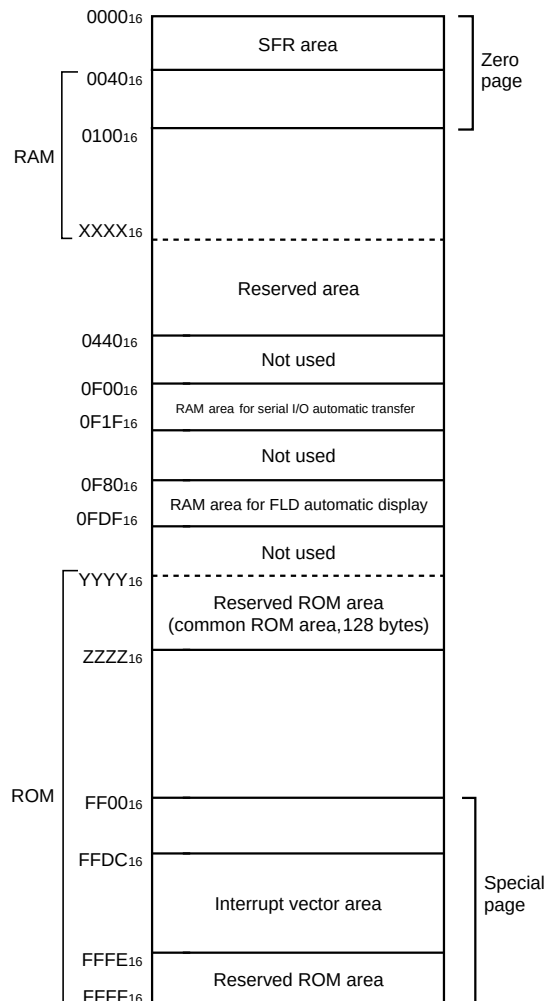


Fig. 2 Memory map

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Timer 1 (T1)
0001 ₁₆		0021 ₁₆	Timer 2 (T2)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer 3 (T3)
0003 ₁₆		0023 ₁₆	Timer 4 (T4)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Timer 5 (T5)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer 6 (T6)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Serial I/O3 register (SIO3)
0007 ₁₆		0027 ₁₆	Timer 6 PWM register (T6PWM)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Timer 12 mode register (T12M)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	Timer 34 mode register (T34M)
000A ₁₆	Port P5 (P5)	002A ₁₆	Timer 56 mode register (T56M)
000B ₁₆	Port P5 direction register (P5D)	002B ₁₆	D-A conversion register (DA)
000C ₁₆	Port P6 (P6)	002C ₁₆	AD-DA control register (ADCON)
000D ₁₆	Port P6 direction register (P6D)	002D ₁₆	A-D conversion register (AD)
000E ₁₆	Port P7 (P7)	002E ₁₆	
000F ₁₆	Port P7 direction register (P7D)	002F ₁₆	
0010 ₁₆	Port P8 (P8)	0030 ₁₆	Interrupt interval determination register (IID)
0011 ₁₆	Port P8 direction register (P8D)	0031 ₁₆	Interrupt interval determination control register (IIDCON)
0012 ₁₆	Port P9 (P9)	0032 ₁₆	Port P0 segment/digit switch register (P0SDR)
0013 ₁₆		0033 ₁₆	Port P2 digit/port switch register (P2DPR)
0014 ₁₆	Port PA (PA)	0034 ₁₆	Port P8 segment/port switch register (P8SPR)
0015 ₁₆	Port PA direction register (PAD)	0035 ₁₆	Port PA segment/port switch register (PASPR)
0016 ₁₆	Port PB (PB)	0036 ₁₆	FLDC mode register 1 (FLDM1)
0017 ₁₆	Port PB direction register (PBD)	0037 ₁₆	FLDC mode register 2 (FLDM2)
0018 ₁₆	Serial I/O automatic transfer data pointer (SIODP)	0038 ₁₆	FLD data pointer (FLDDP)
0019 ₁₆	Serial I/O1 control register (SIO1CON)	0039 ₁₆	Zero cross detection control register (ZCRCON)
001A ₁₆	Serial I/O automatic transfer control register (SIOAC)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	Serial I/O1 register (SIO1)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Serial I/O automatic transfer interval register (SIOAI)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆	Serial I/O2 control register (SIO2CON)	003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆	Serial I/O3 control register (SIO3CON)	003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆	Serial I/O2 register (SIO2)	003F ₁₆	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

I/O PORTS**Direction Registers**

The 3819 group has 54 programmable I/O pins arranged in 8 I/O ports (ports P24–P27, P41–P44, P46, P47, P5–P8, PA, and PB). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set for output, the value of the port latch is read, not the value of the pin itself. A pin which is set for input the value of the pin itself is read because the pin is in floating state. If a pin set for input is written to, only the port latch is written to and the pin remains floating.

High-Breakdown-Voltage Output Ports

The 3819 group microprocessors have 7 ports with high-breakdown-voltage pins (ports P0, P1, P20–P23, P3, P8, P9, PA). The high-breakdown-voltage ports have P-channel open-drain output with $V_{CC} - 40$ V of breakdown voltage.

Each pin in ports P0, P1, P20–P23, P3, and P9 has an internal pull-down resistor connected to V_{EE} . Ports P8 and PA have no internal pull-down resistors, so that connect an external resistor to each port. At reset, the P-channel output transistor of each port latch is turned off, so it becomes V_{EE} level (“L”) by the pull-down resistor.

Writing “1” (weak drivability) to bit 7 of the FLDC mode register 1 (address 003616) shows the rising transition of the output transistors for reducing transient noise. At reset, bit 7 of the FLDC mode register 1 is set to “0” (strong drivability).

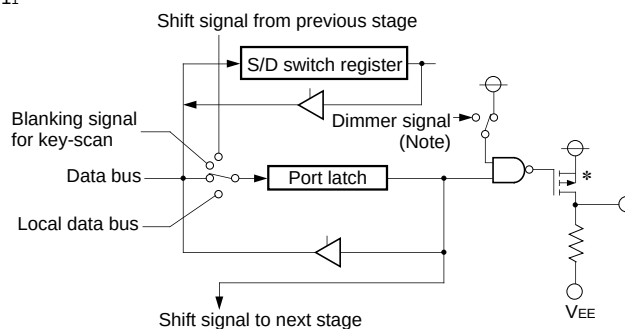
Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P00/SEG32/ DIG0– P07/SEG39/ DIG7	Port P0	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register 1 FLDC mode register 2 Port P0 segment/digit switch register	(1)
P10/SEG40/ DIG8– P17/DIG15	Port P1	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register 1 FLDC mode register 2	(1) (2)
P20/DIG16– P23/DIG19	Port P2	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register 1 FLDC mode register 2 Port P2 digit/port switch register	(3)
P24–P27		Input/output, individual bits	TTL level input CMOS 3-state output			(4)
P30/SEG24– P37/SEG31	Port P3	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register 1 FLDC mode register 2	(5)
P40/INT0 P45/INT1/ ZCR	Port P4	Input	CMOS compatible input level	External interrupt input Zero cross detection circuit input (P45)	Interrupt edge selection register Zero cross detection control register	(6)
P42/INT2– P44/INT4		Input/output, individual bits	CMOS compatible input level CMOS 3-state output			(7)
P41						(4)
P46/T1OUT, P47/T3OUT				Timer output	Timer 12 mode register Timer 34 mode register	(8)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

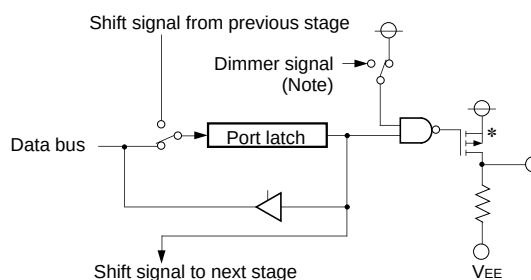
Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P50/SIN2/ AN8	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 func- tion I/O A-D conversion in- put	Serial I/O2 control register AD/DA control regis- ter	(9)
P51/SOUT2/ AN9, P52/SCLK2/ AN10						(10)
P53/SRDY2/ AN11						(11)
P54/SIN3/ AN12				Serial I/O3 func- tion I/O A-D conversion in- put	Serial I/O3 control register AD/DA control regis- ter	(9)
P55/SOUT3/ AN13, P56/SCLK3/ AN14						(10)
P57/SRDY3/ AN15						(11)
P60	Port P6	Input/output, individual bits	CMOS compatible input level CMOS 3-state output			(4)
P61/PWM				PWM (timer) out- put	Timer 56 mode regis- ter	(8)
P62/CNTR0, P63/CNTR1				Timer input	Interrupt edge selec- tion register	(7)
P64/SIN1				Serial I/O1 func- tion I/O	Serial I/O1 control register Serial I/O automatic transfer control regis- ter	(9)
P65/SOUT1, P66/SCLK11						(10)
P67/SRDY1/ CS/SCLK12						(11)
P70/AN0– P77/AN7	Port P7		CMOS compatible input level CMOS 3-state output	A-D conversion in- put	AD/DA control regis- ter	(12)
P80/SEG8– P87/SEG15	Port P8		CMOS compatible input level High-breakdown- voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register Segment/port switch register	(13)
P90/SEG16– P97/SEG23	Port P9	Output	High-breakdown- voltage P-channel open-drain output with pull-down resistor		FLDC mode register	(5)
PA0/SEG0– PA7/SEG7	Port PA	Input/output, individual bits	CMOS compatible input level High-breakdown- voltage P-channel open-drain output		FLDC mode register Segment/port switch register	(13)
PB0/XCOUT, PB1/XCIN	Port PB	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	I/O for sub-clock generating circuit	CPU mode register	(14) (15)
PB2/DA				D-A conversion output	AD/DA control regis- ter	(16)
PB3						(4)

Note : Make sure that the input level at each pin is either 0 V or V_{CC} during execution of the STP instruction. When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.

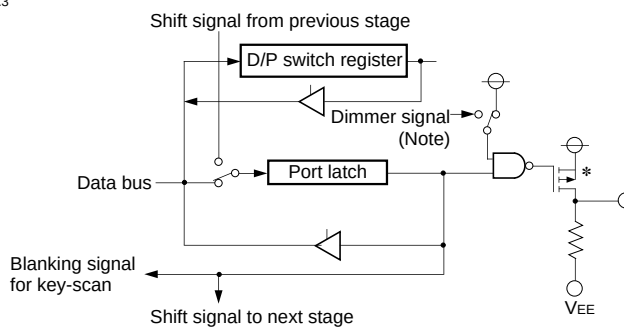
(1) Ports P0, P10, P11



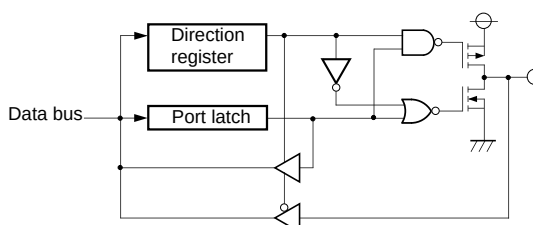
(2) Ports P12–P17



(3) Ports P20–P23



(4) Ports P24–P27, P41, P60, PB3

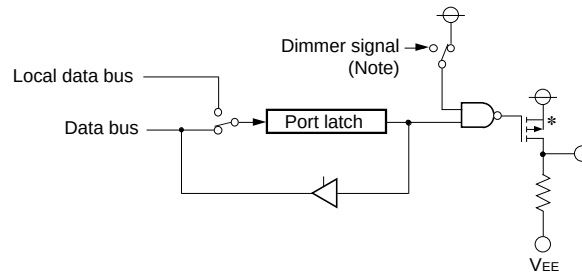


* : High-breakdown-voltage P-channel transistor

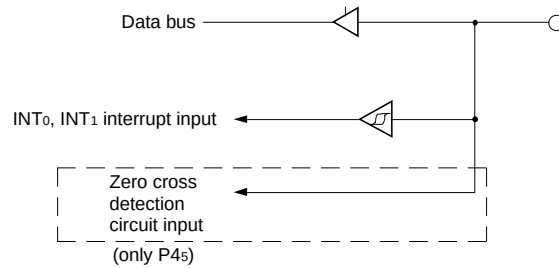
Note: The dimmer signal sets the Toff timing.

Fig. 4 Port block diagram (1)

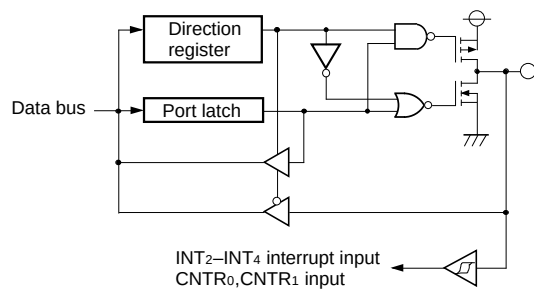
(5) Ports P3, P9



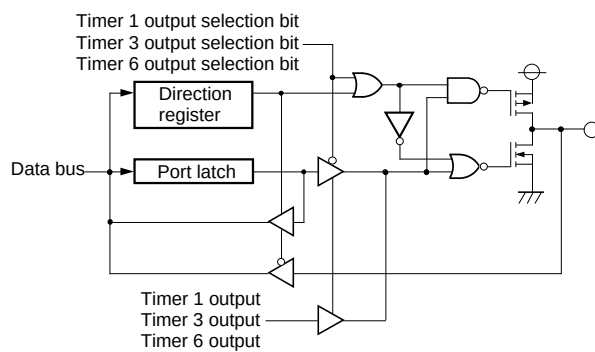
(6) Ports P40, P45



(7) Ports P42–P44, P62, P63



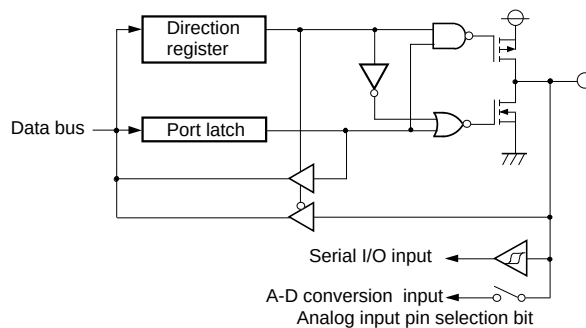
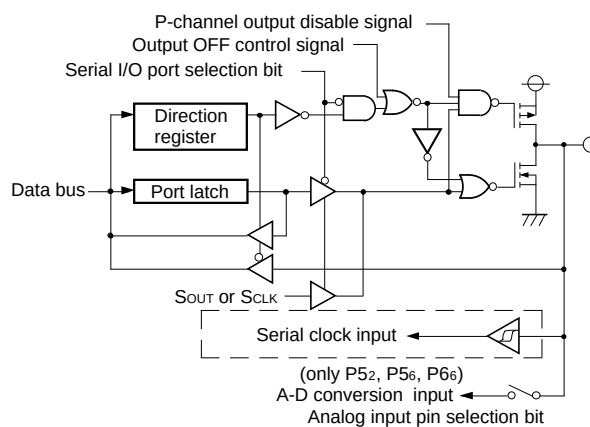
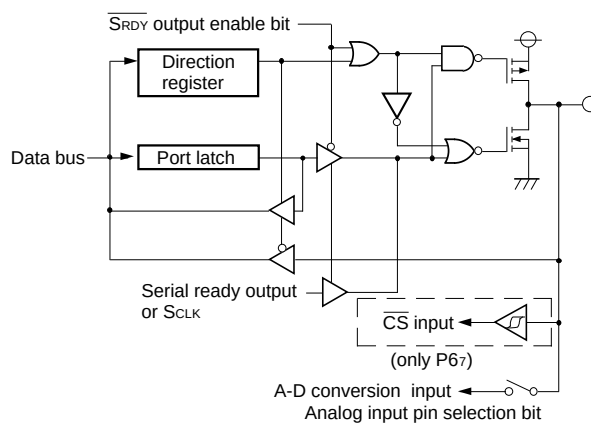
(8) Ports P46, P47, P61



* : High-breakdown-voltage P-channel transistor

Note: The dimmer signal sets the Toff timing.

Fig. 5 Port block diagram (2)

(9) Ports P5₀, P5₄, P6₄(10) Ports P5₁, P5₂, P5₅, P5₆, P6₅, P6₆(11) Ports P5₃, P5₇, P6₇

(12) Port P7

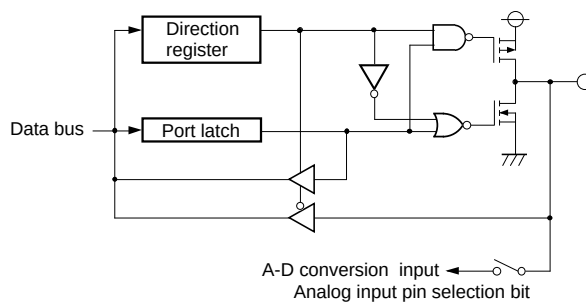
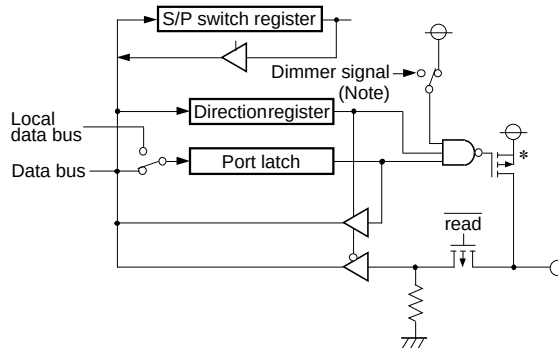
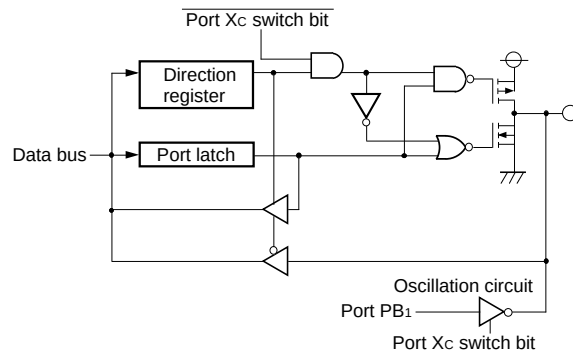


Fig. 6 Port block diagram (3)

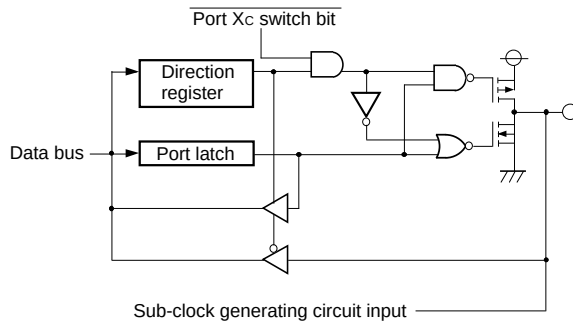
(13) Ports P8, PA



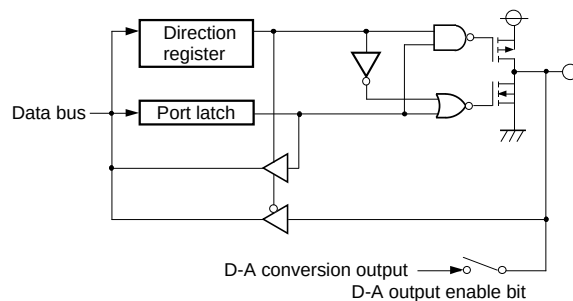
(14) Port PB₀



(15) Port PB₁



(16) Port PB₂



* : High-breakdown-voltage P-channel transistor

Note: The dimmer signal sets the Toff timing.

Fig. 7 Port block diagram (4)

INTERRUPTS

Interrupts occur by 20 sources: 5 external, 14 internal, and 1 software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit.

The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

Interrupt Operation

When an interrupt is received, the contents of the program counter and processor status register are automatically stored into the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

Notes on Use

When the active edge of an external interrupt (INT0 to INT4) is changed or when switching interrupt sources in the same vector address, the corresponding interrupt request bit may also be set. Therefore, please take following sequence;

- (1) Disable the external interrupt which is selected.
- (2) Change the active edge.
- (3) Clear the interrupt request bit which is selected to "0".
- (4) Enable the external interrupt which is selected.

Table 1. Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
INT1/ZCR	3	FFF916	FFF816	At detection of either rising or falling edge of INT1/ZCR input	External interrupt (active edge selectable)
INT2	4	FFF716	FFF616	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
Remote control/counter overflow				At 8-bit counter overflow	Valid when interrupt interval determination is operating
Serial I/O1	5	FFF516	FFF416	At completion of data transfer	Valid when serial I/O ordinary mode is selected
Serial I/O automatic transfer				At completion of the last data transfer	Valid when serial I/O automatic transfer mode is selected
Serial I/O2	6	FFF316	FFF216	At completion of data transfer	Valid when serial I/O2 is selected
Serial I/O3	7	FFF116	FFF016	At completion of data transfer	Valid when serial I/O3 is selected
Timer 1	8	FFEF16	FFEE16	At timer 1 underflow	STP release timer underflow
Timer 2	9	FFED16	FFEC16	At timer 2 underflow	
Timer 3	10	FFEB16	FFEA16	At timer 3 underflow	
Timer 4	11	FFE916	FFE816	At timer 4 underflow	
Timer 5	12	FFE716	FFE616	At timer 5 underflow	
Timer 6	13	FFE516	FFE416	At timer 6 underflow	
INT3	14	FFE316	FFE216	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
INT4	15	FFE116	FFE016	At detection of either rising or falling edge of INT4 input	Valid when INT4 interrupt is selected External interrupt (active edge selectable)
A-D conversion				At completion of A-D conversion	Valid when A-D conversion interrupt is selected
FLD blanking	16	FFDF16	FFDE16	At falling edge of the last digit immediately before blanking period starts	Valid when FLD blanking interrupt is selected
FLD digit				At rising edge of each digit	Valid when FLD digit interrupt is selected
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Notes 1 : Vector addresses contain interrupt jump destination addresses.

2 : Reset function in the same way as an interrupt with the highest priority.

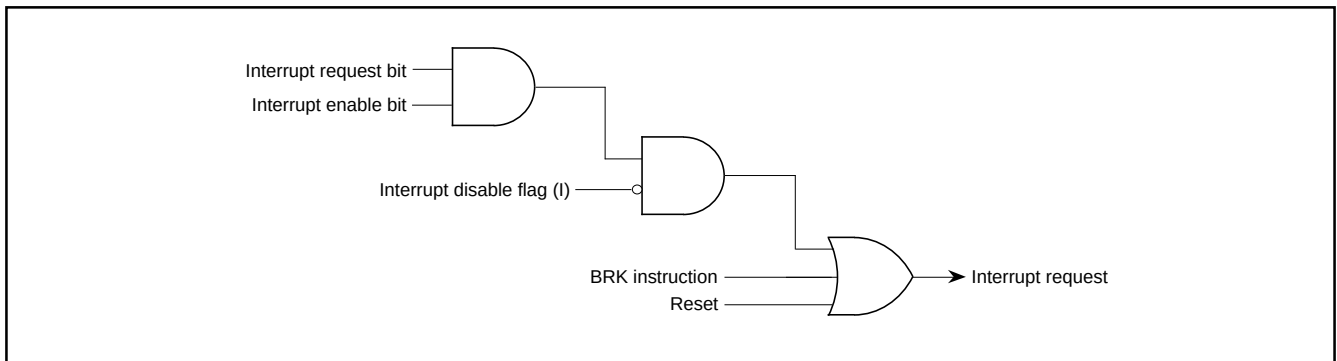


Fig. 8 Interrupt control

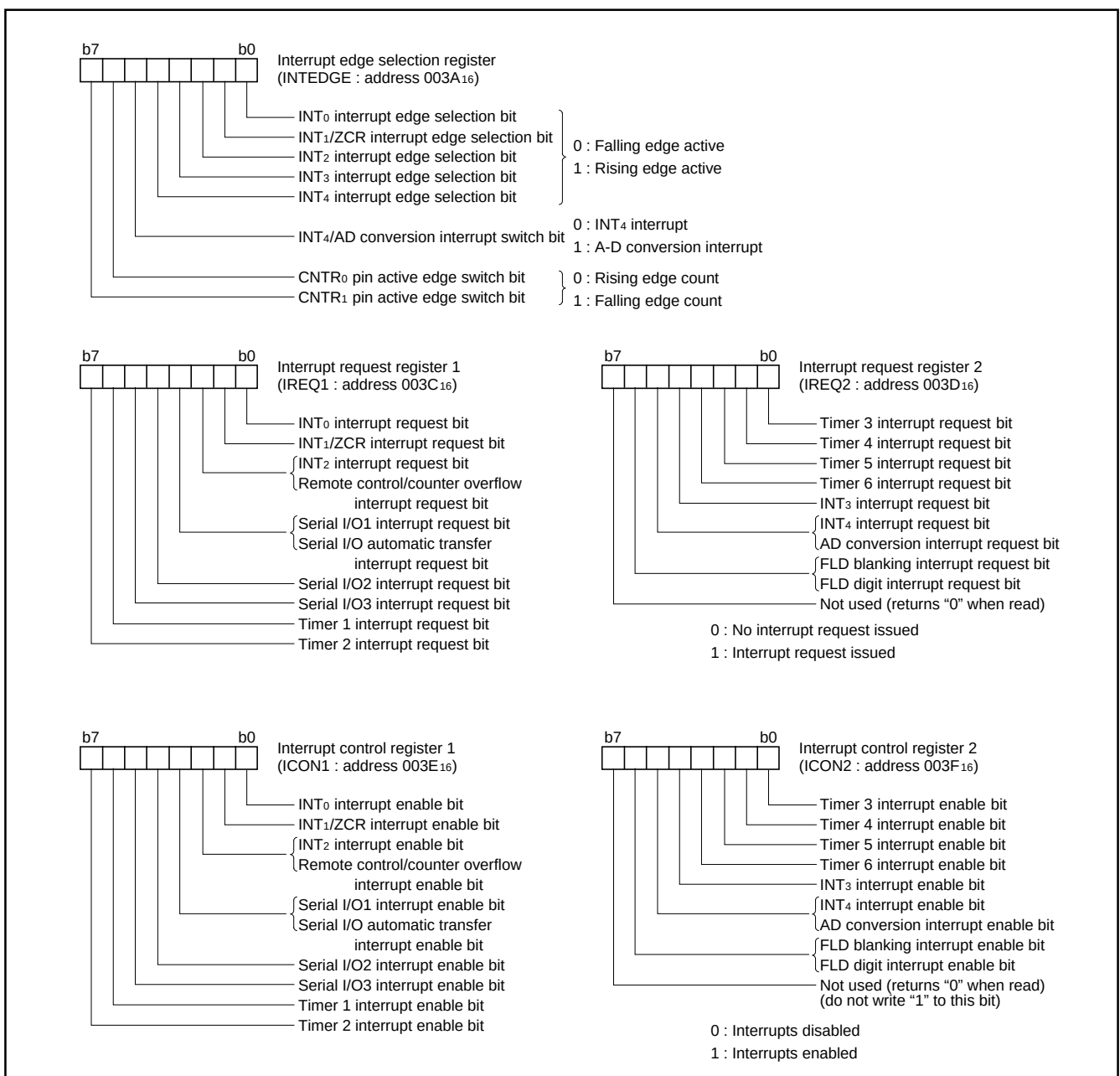


Fig. 9 Structure of interrupt-related registers

TIMERS

The 3819 group has 6 built-in timers: timer 1, timer 2, timer 3, timer 4, timer 5, and timer 6.

Each timer has the 8-bit timer latch. The timers count down.

Once a timer reaches 00₁₆, at the next count pulse the contents of each timer latch is loaded into the corresponding timer, and sets the corresponding interrupt request bit to "1".

The count can be stopped by setting the stop bit of each timer to "1". The internal clock ϕ can be set to either the high-speed mode or low-speed mode with the CPU mode register. At the same time, timer internal count source is switched to either $f(XIN)$ or $f(XCIN)$.

Timer 1 and Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register. A rectangular waveform of timer 1 underflow signal divided by 2 is output from the P46/T1OUT pin. The waveform polarity changes each time timer 1 overflows. The active edge of the external clock CNTR0 can be switched with the bit 6 of the interrupt edge selection register.

At reset or when executing the STP instruction, all bits of the timer 12 mode register are cleared to "0", timer 1 is set to "FF₁₆", and timer 2 is set to "01₁₆".

Timer 3 and Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register. A rectangular waveform of timer 3 underflow signal divided by 2 is output from the P47/T3OUT pin. The waveform polarity changes each time timer 3 overflows.

The active edge of the external clock CNTR1 can be switched with the bit 7 of the interrupt edge selection register.

Timer 5 and Timer 6

The count sources of timer 5 and timer 6 can be selected by setting the timer 56 mode register.

A rectangular waveform of timer 6 underflow signal divided by 2 is output from the P61/PWM pin. The waveform polarity changes each time timer 6 overflows.

Timer 6 PWM Mode

Timer 6 can output a rectangular waveform with duty cycle $n/(n + m)$ from the P61/PWM pin by setting the timer 56 mode register (refer to fig. 12). The n is the value set in timer 6 latch (address 0025₁₆) and m is the value in the timer 6 PWM register (address 0027₁₆). If n is "0", the PWM output is "L", if m is "0", the PWM output is "H" ($n=0$ is prior than $m=0$). In the PWM mode, interrupts occur at the rising edge of the PWM output.

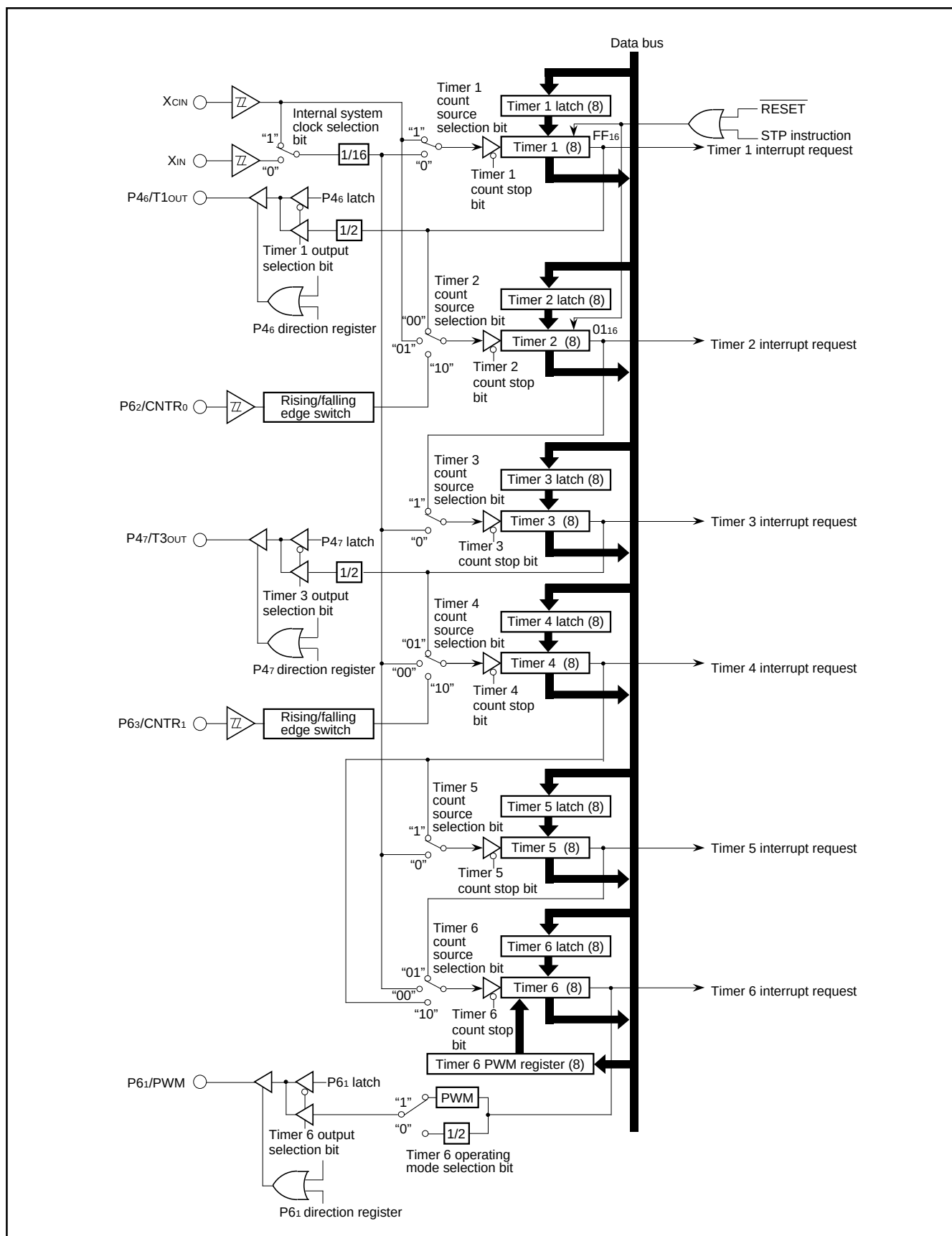


Fig. 10 Timer block diagram

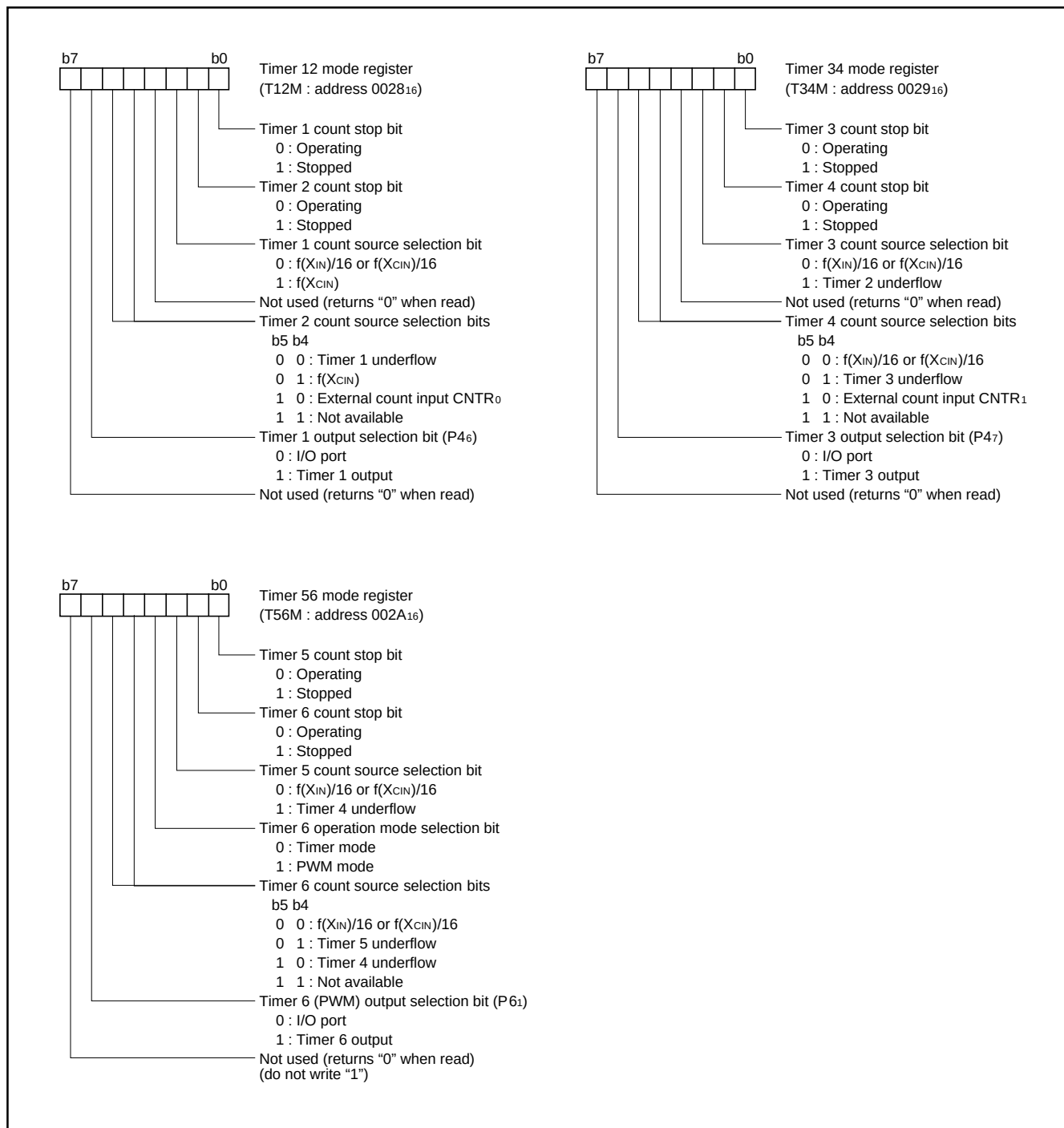


Fig. 11 Structure of timer-related registers

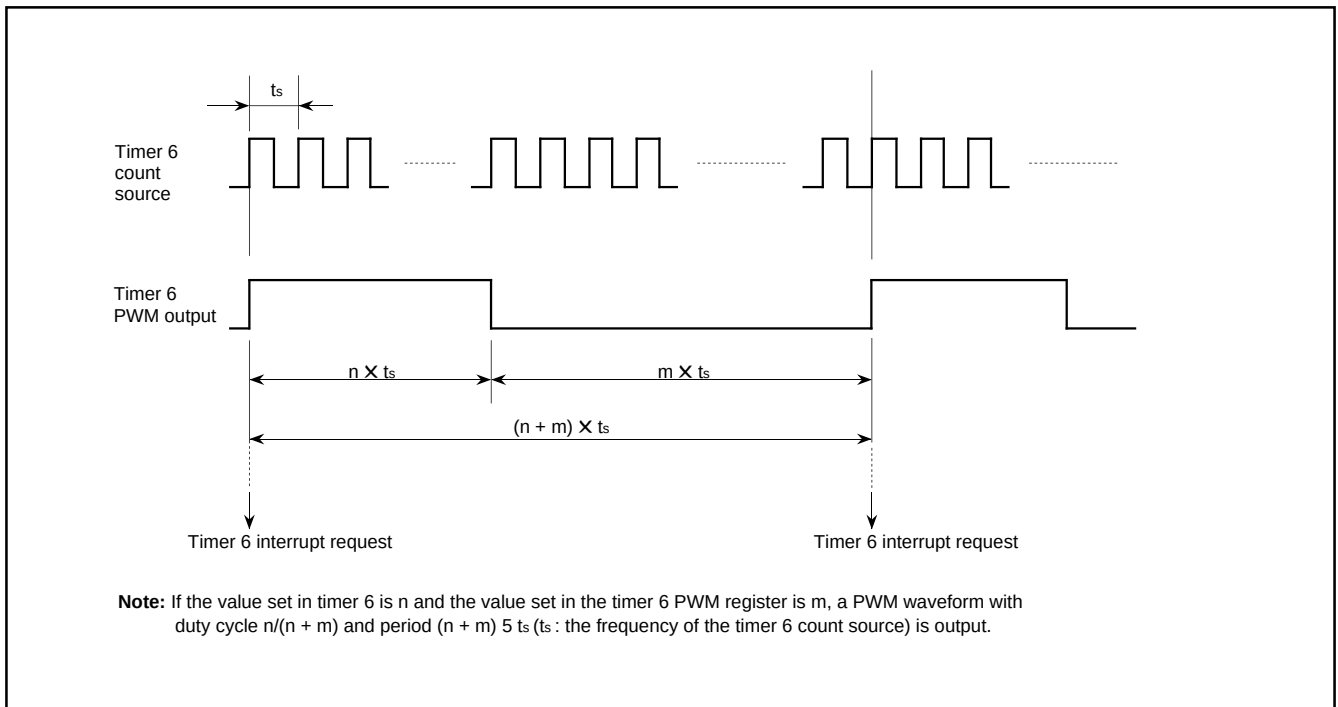


Fig. 12 Timing in timer 6 PWM mode

SERIAL I/O

The 3819 group has built-in 8-bit clock synchronized serial I/O × 3 channels (serial I/O1, serial I/O2, and serial I/O3).

Serial I/O1 builds in the automatic transfer function. The function can be switched to the serial I/O ordinary mode with the serial I/O automatic transfer control register (address 001A₁₆).

Serial I/O2 and Serial I/O3 can be used only in the serial I/O ordinary mode.

The I/O pins of the serial I/O function are also used as I/O ports P5 and P64–P67, and their operation is selected with the serial I/O control registers (addresses 0019₁₆, 001D₁₆, and 001E₁₆).

Serial I/O Control Registers (SIO1CON, SIO2CON, SIO3CON) 0019₁₆, 001D₁₆, 001E₁₆

Each of the serial I/O control registers (addresses 0019₁₆, 001D₁₆, and 001E₁₆) consists of 8 selection bits which control the serial I/O function.

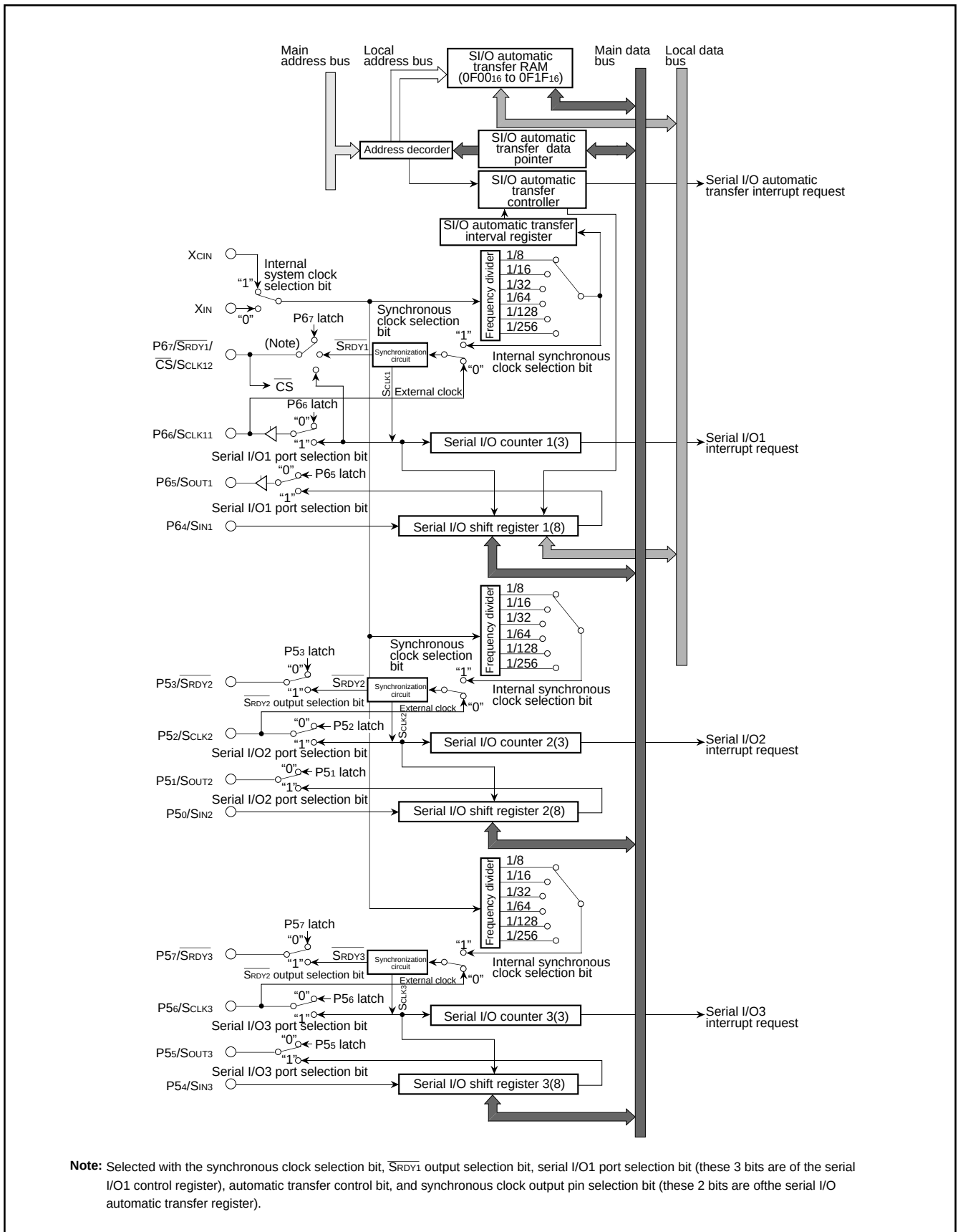


Fig. 13 Serial I/O block diagram

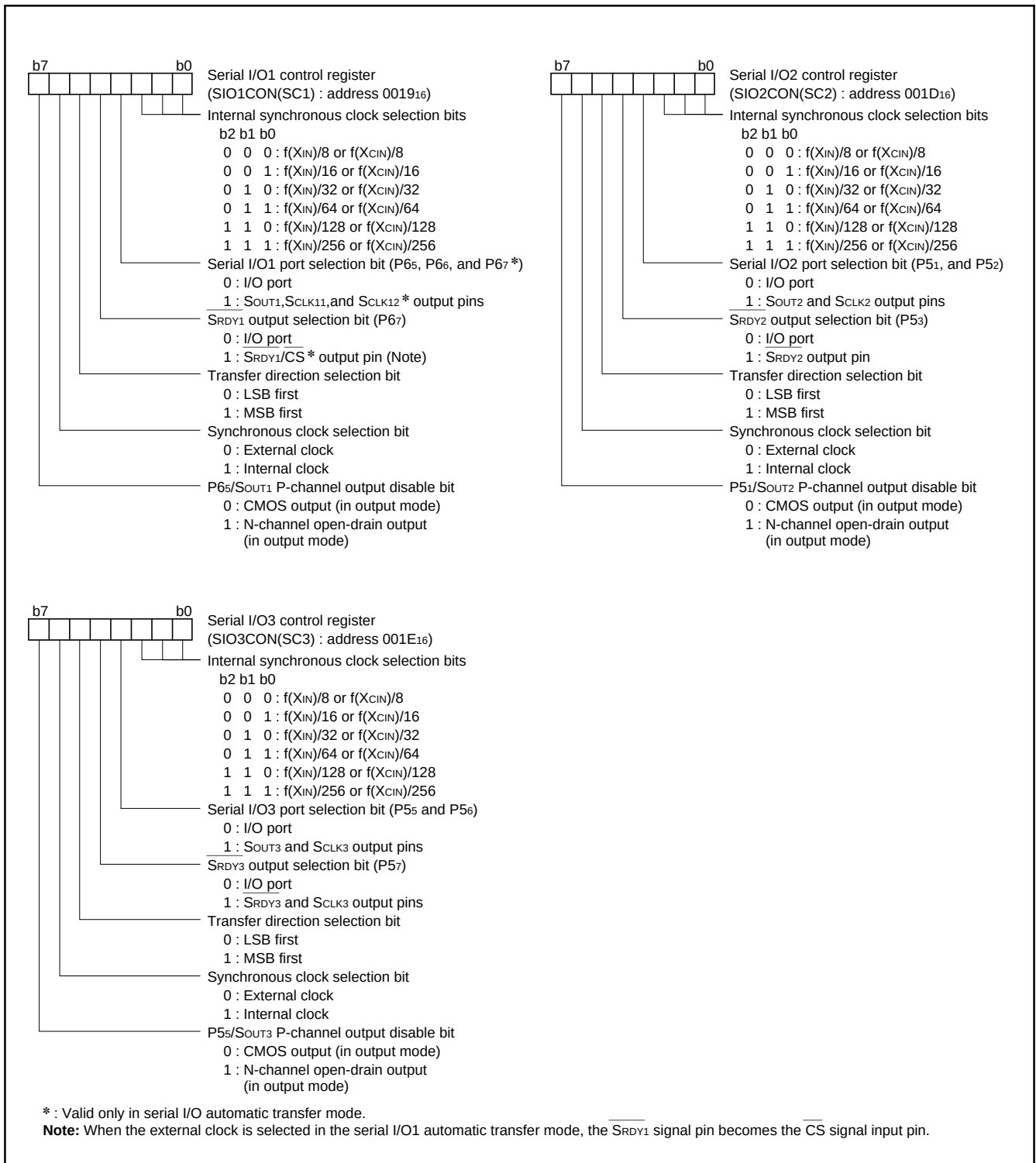


Fig. 14 Structure of serial I/O control registers

(1) Serial I/O Ordinary Mode

Either an internal clock or an external clock can be selected as the synchronous clock for serial I/O transfer. A dedicated divider is built in as the internal clock for selecting of 6 clocks. If internal clock is selected, transfer starts with a write signal to a serial I/O register (addresses 001B16, 001F16, or 002616). After 8 bits have been transferred, the SOUT pin goes to high impedance state.

If external clock is selected, control the clock externally because the contents of the serial I/O register continue to shift during inputting the transfer clock. In this case, note that the SOUT pin does not go to high impedance state at the completion of data transfer.

The interrupt request bit is set at the completion of the transfer of 8 bits, regardless of whether the internal or external clock is selected.

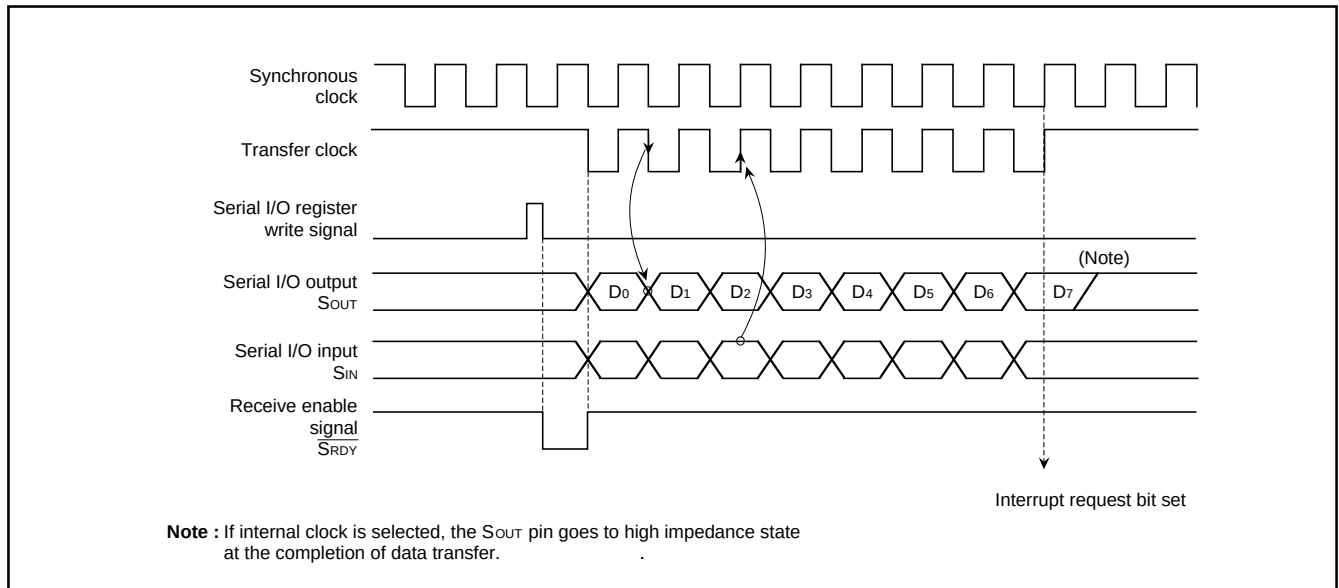


Fig. 15 Serial I/O timing in the serial I/O ordinary mode (for LSB first)

(2) Serial I/O Automatic Transfer Mode

The serial I/O1 has the automatic transfer function. For automatic transfer, switch to the automatic transfer mode by setting the serial I/O automatic transfer control register (address 001A16).

The following memory spaces and registers used to enable automatic transfer mode:

- 32-byte serial I/O automatic transfer RAM
- A serial I/O automatic transfer control register
- A serial I/O automatic transfer interval register
- A serial I/O automatic transfer data pointer

When using serial I/O automatic transfer, set the serial I/O1 control register (address 001916) in the same way as the serial I/O ordinary mode. However, note that when external clock is selected, port P67 becomes the $\overline{CS}$ input pin by setting the bit 4 (the $\overline{SRDY}$ output selection bit) of the serial I/O1 control register to "1".

Serial I/O Automatic Transfer Control Register (SIOAC) 001A16

The serial I/O automatic transfer control register (address 001A16) consists of 4 bits which control automatic transfer.

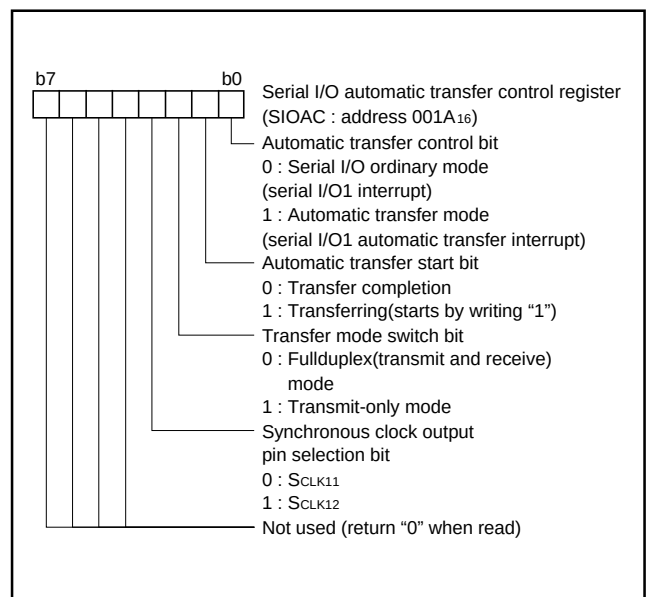


Fig. 16 Structure of serial I/O automatic transfer control register

Serial I/O Automatic Transfer Data Pointer (SIODP) 0018₁₆

The serial I/O automatic transfer data pointer (address 0018₁₆) consists of 5 bits which indicate addresses in serial I/O automatic transfer RAM (the value which adds 0F00₁₆ to the serial I/O automatic transfer data pointer is actual address in memory). Set the value (the number of transfer data-1) to the serial I/O automatic transfer data pointer for specifying the storage address of first data.

● Serial I/O Automatic Transfer RAM

The serial I/O automatic transfer RAM is the 32 bytes from address 0F00₁₆ to address 0F1F₁₆.

Address \ Bit	7	6	5	4	3	2	1	0
0F00 ₁₆								
0F01 ₁₆								
0F02 ₁₆								
⋮								
0F1D ₁₆								
0F1E ₁₆								
0F1F ₁₆								

Fig. 17 Bit allocation of serial I/O automatic transfer RAM

● Setting of Serial I/O Automatic Transfer Data

When data is stored in the serial I/O automatic transfer RAM, store the first data at the address set with the serial I/O automatic transfer data pointer so that the last data can be stored at address 0F00₁₆.

Serial I/O Automatic Transfer Interval Register (SIOAI) 001C₁₆

The serial I/O automatic transfer interval register (address 001C₁₆) consists of a 5-bit counter that determines the transfer interval T_i during automatic transfer.

When writing the value n to the serial I/O automatic transfer interval register, $T_i = (n+2) \times T_c$ (T_c : the length of one bit of the transfer clock) occurs. However, note that this transfer interval setting is valid only when selecting the internal clock as the clock source.

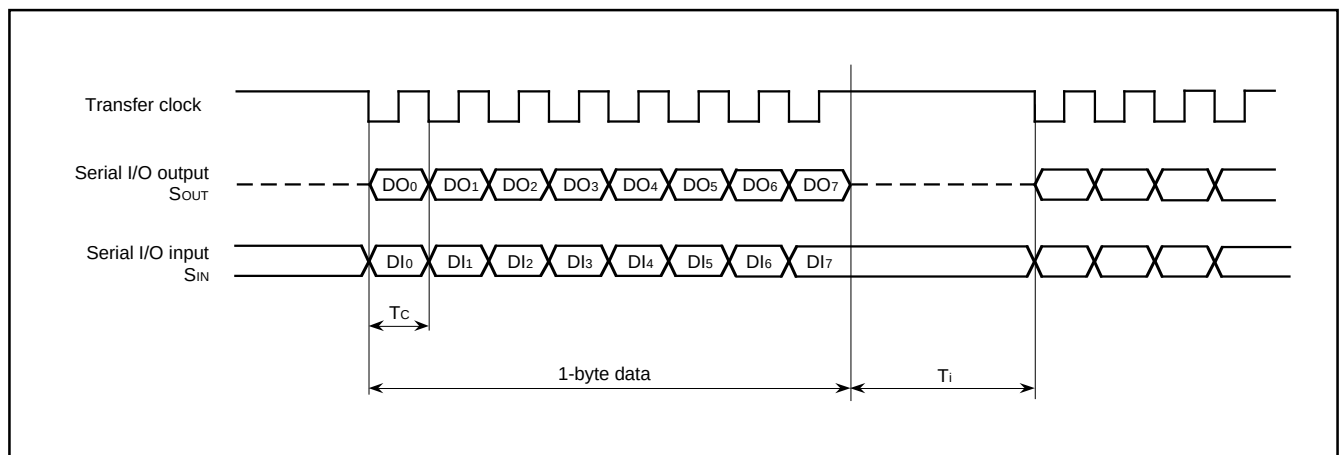


Fig. 18 Serial I/O automatic transfer interval timing

● Setting of Serial I/O Automatic Transfer Timing

The timing of serial I/O automatic transfer is set with the serial I/O1 control register (address 0019₁₆) and the serial I/O automatic transfer interval register (address 001C₁₆).

The serial I/O1 control register sets the transfer clock speed, and the serial I/O automatic transfer interval register sets the serial I/O automatic transfer interval. This setting of transfer interval is valid only when selecting the internal clock as the clock source.

● Start of Serial I/O Automatic Transfer

Automatic transfer mode is set by writing "1" to the bit 0 of the serial I/O automatic transfer control register (address 001A₁₆), then automatic transfer starts by writing "1" to the bit 1.

The bit 1 of the serial I/O automatic transfer control register is always "1" during automatic transfer; writing "0" can complete the serial I/O automatic transfer.

● Operation in Serial I/O Automatic Transfer Modes

There are two modes for serial I/O automatic transfer: full duplex mode and transmit-only mode. Either internal or external clock can be selected for each of these modes.

(2.1) Operation in Full Duplex Mode

In full duplex mode, data can be transmitted and received at the same time. Data in the automatic transfer RAM is transmitted in sequence in accordance with the serial I/O automatic transfer data pointer and simultaneously reception data is written to the automatic transfer RAM.

The transfer timing of each bit is the same as that in ordinary operation mode, and the transfer clock stops at "H" after eight transfer clocks are counted.

When selecting the internal clock, the transfer clock remains at "H" for the time set with the serial I/O automatic transfer interval register, then the data at the next address (the address is indicated with the serial I/O automatic transfer data pointer) are transferred.

If when selecting the external clock, the setting of the automatic transfer interval register is invalid, so control the transfer clock externally.

The last data transfer completes when the contents of the serial I/O automatic transfer pointer reach "00₁₆". At that point, the serial I/O automatic transfer interrupt request bit is set to "1" and the bit 1 of the serial I/O automatic transfer control register is cleared to "0" to complete the serial I/O automatic transfer.

(2.2) Operation in Transmit-Only Mode

The operation in transmit-only mode is the same as that in full duplex mode, except for that data is not transferred from the serial I/O1 register to the serial I/O automatic transfer RAM.

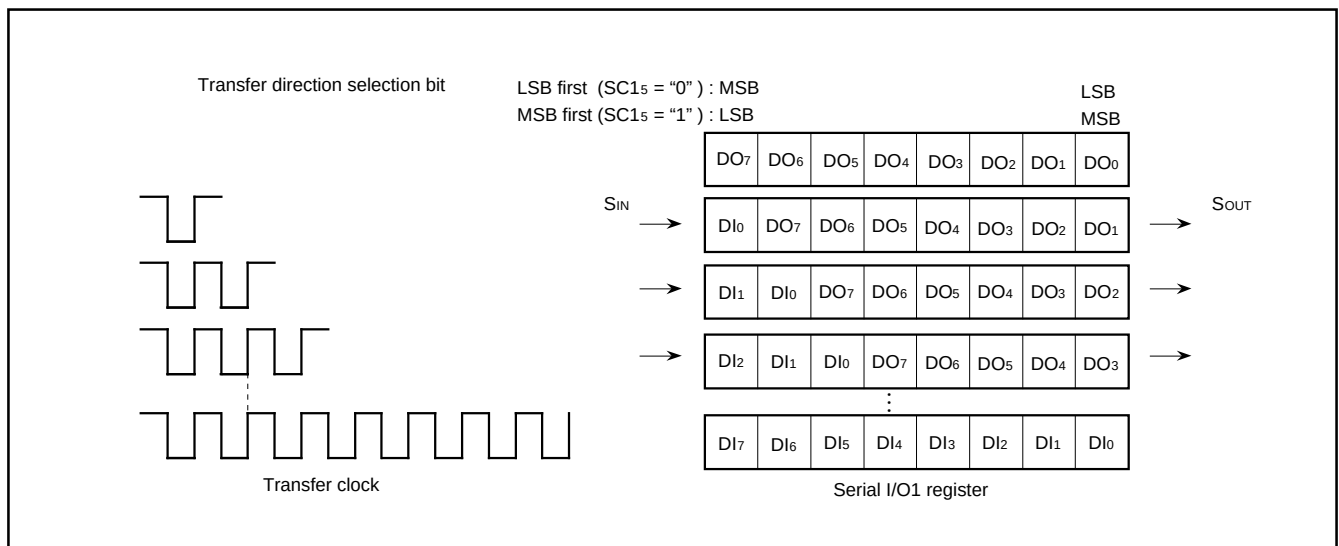


Fig. 19 Serial I/O1 register transfer operation in full duplex mode

(2.3) When Selecting the Internal Clock

When selecting the internal clock, the P67/ $\overline{\text{SRDY1}}/\overline{\text{CS}}/\text{SCLK12}$ pin can be used as the $\overline{\text{SRDY1}}$ pin by setting SC14 to "1".

When selecting the internal clock, the P67 pin can be used as the synchronous clock output pin SCLK12 by setting SIOAC3 to "1". In this case, the SCLK11 pin goes to high impedance state.

Select the function of the P67/ $\overline{\text{SRDY1}}/\overline{\text{CS}}/\text{SCLK12}$ and P66/SCLK11 with the following registers (refer to Table 2):

- the bit 3 (SC13), the bit 4(SC14), and the bit 6(SC16) of the serial I/O1 control register
- the bit 3 (SIOAC3) of the serial I/O automatic transfer control register

When using both the SCLK11 and SCLK12 by switching, switch the P67/ $\overline{\text{SRDY1}}/\overline{\text{CS}}/\text{SCLK12}$ to the P67 (SC14=0) and set the P67 direction register to input mode. Note that switch SIOAC3 during "H" of transfer clock at the completion of automatic transfer.

Table 2. SCLK11 and SCLK12 selection

SC16	SC14	SC33	SIOAC3	P66/SCLK11	P67/SCLK12
1	0	1	0	SCLK11	P67
			1	High impedance	SCLK12

Note : SC13: Serial I/O1 port selection bit

SC14: $\overline{\text{SRDY1}}$ output selection bit

SC16: Synchronous clock selection bit

SIOAC3: Synchronous clock output pin selection bit

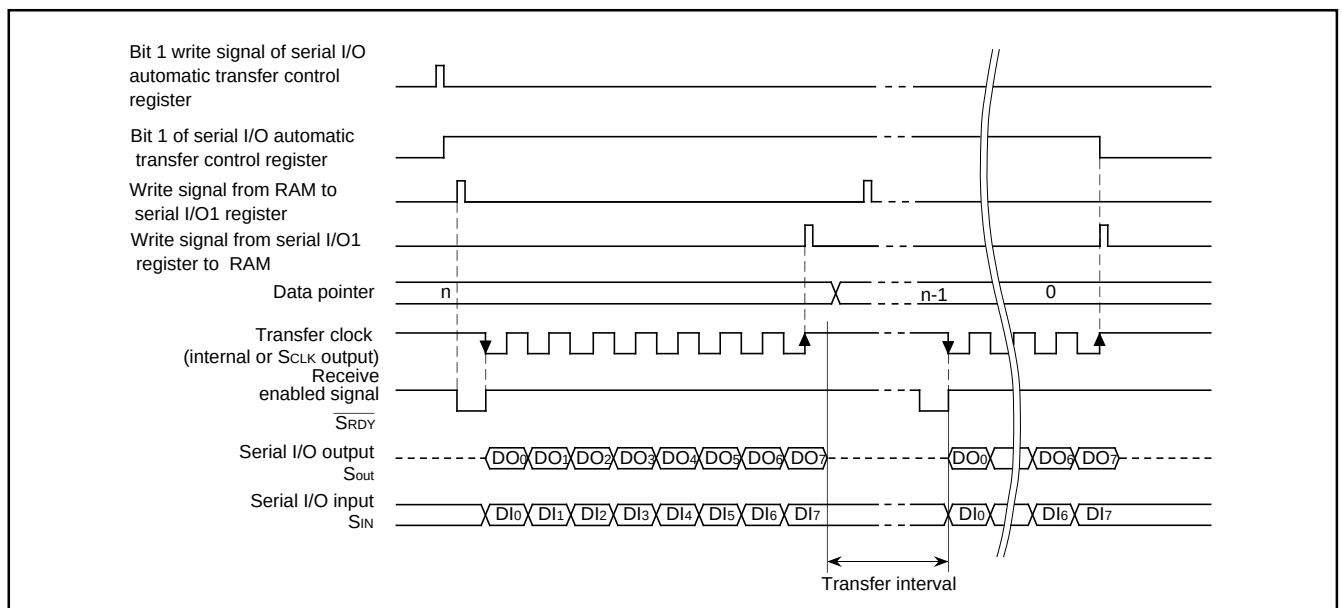


Fig. 20 Timing diagram during serial I/O automatic transfer (internal clock selected, $\overline{\text{SRDY}}$ used)

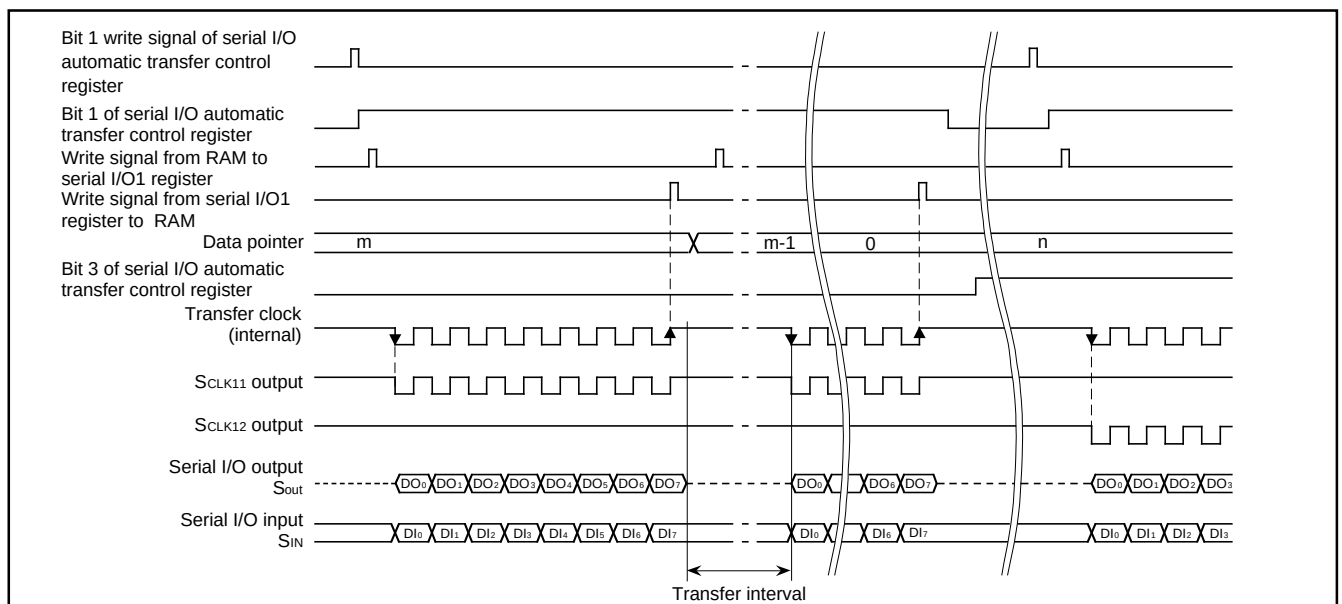


Fig. 21 Timing during serial I/O automatic transfer (internal clock selected, SCLK11 and SCLK12 used)

(2.4) When Selecting the External Clock

When selecting the external clock, the internal clock and the setting of transfer interval with the serial I/O automatic transfer interval register are invalid, but the serial I/O output pin SOUT1 and the internal transfer clock can be controlled from the outside by setting the SRDY1 pin to the CS (input) pin.

When the CS input is "L", the SOUT1 pin and the internal transfer clock are enabled.

When the CS input is "H", the SOUT1 pin goes to high impedance state and the internal transfer clock goes to "H".

Select the function of the P67/SRDY1/CS/SCLK12 with the following registers (refer to Table GA-2):

- the bit 4 (SC14) and the bit 6 (SC16) of the serial I/O1 control register
- the bit 0 (SIOAC0) of the serial I/O automatic transfer control register

Switch the CS pin from "L" to "H" or from "H" to "L" during "H" of the transfer clock (SCLK11 input) after transferring 1-byte data.

When selecting the external clock, set the external clock to "L" after 9 cycles or more of the internal clock ϕ after setting the start bit. After transferring 1-byte data, leave 11 cycles or more of the internal clock ϕ free for the transfer interval.

When not using the CS input, note that the SOUT pin will not go to high impedance state, even after transfer is completed.

When not using the CS input, or when CS is "L", control the external clock because the data in the serial I/O register will continue to shift while the external clock is input, even after the completion of automatic transfer (Note that the automatic transfer interrupt request bit is set and the bit 1 of the serial I/O automatic transfer register is cleared at the point when the specified number of bytes of data have been transferred.)

Table 3. P67/SRDY1/CS selection

SC16	SC14	SIOAC0	P67/SRDY1/CS
0	0	X	P67
	1	0	SRDY1
		1	CS

Note : SC14: SRDY1 output selection bit

SC16: Synchronous clock selection bit

SIOAC0: Automatic transfer control bit

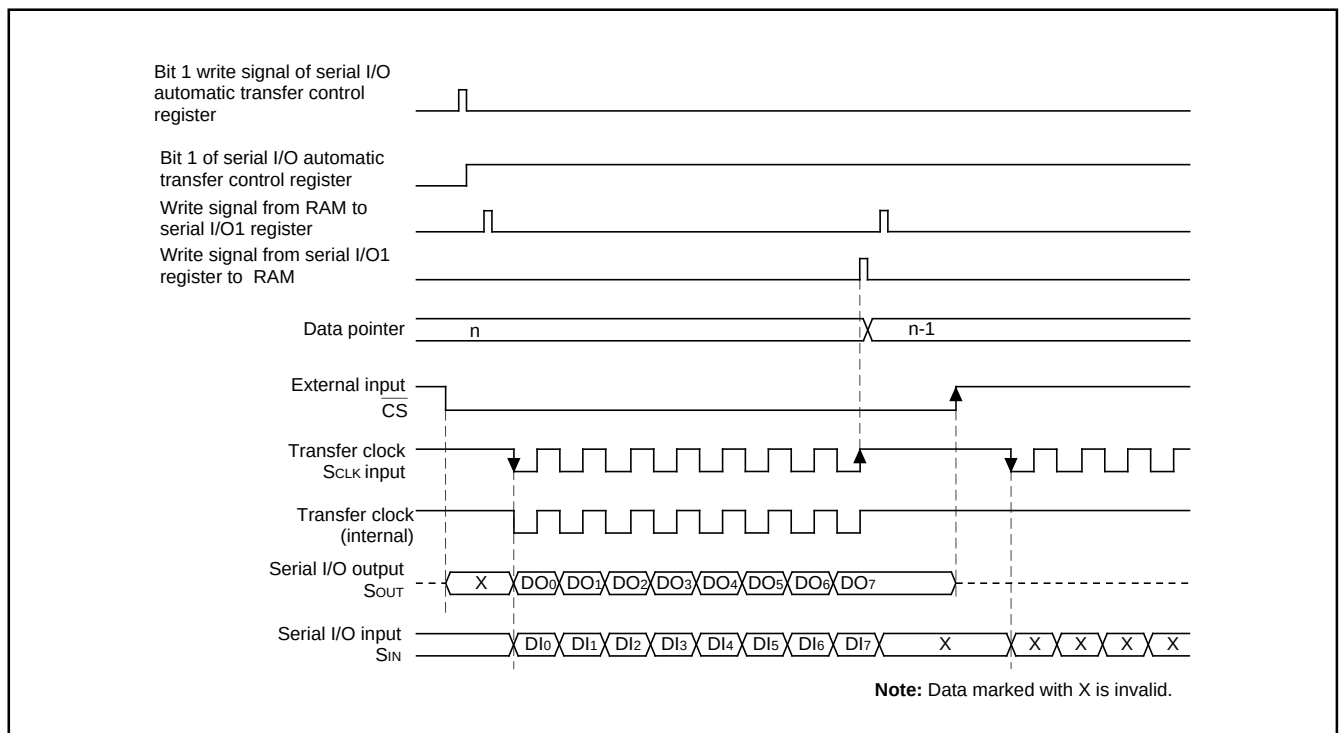


Fig. 22 Timing during serial I/O automatic transfer (external clock selected)

A-D CONVERTER

The functional blocks of the A-D converter are described below.

A-D Conversion Register (AD) 002D16

The A-D conversion register is a read-only register that stores the result of an A-D conversion. This register should not be read during A-D conversion.

AD/DA Control Register (ADCON) 002C16

The AD/DA control register controls the A-D and the D-A conversion process. Bits 0 to 3 of this register select analog input pins. Bit 4 is the AD conversion completion bit. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed.

The A-D conversion starts by writing "0" to this bit. Bit 6 controls the output of D-A converter.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF by 256, and outputs the divided voltages.

Channel Selector

The channel selector selects one of the input ports P77/AN7–P70/AN0, P57/SRDY3/AN15–P50/SIN2/AN8, and inputs to the comparator.

Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD conversion interrupt request bit to "1".

Note that the comparator is constructed linked to a capacitor, so set f(XIN) to 500 kHz or more during A-D conversion.

Note : When using the A-D conversion interrupt, set the INT4/AD conversion interrupt switch bit (the bit 5 of the interrupt selection register) to "1".

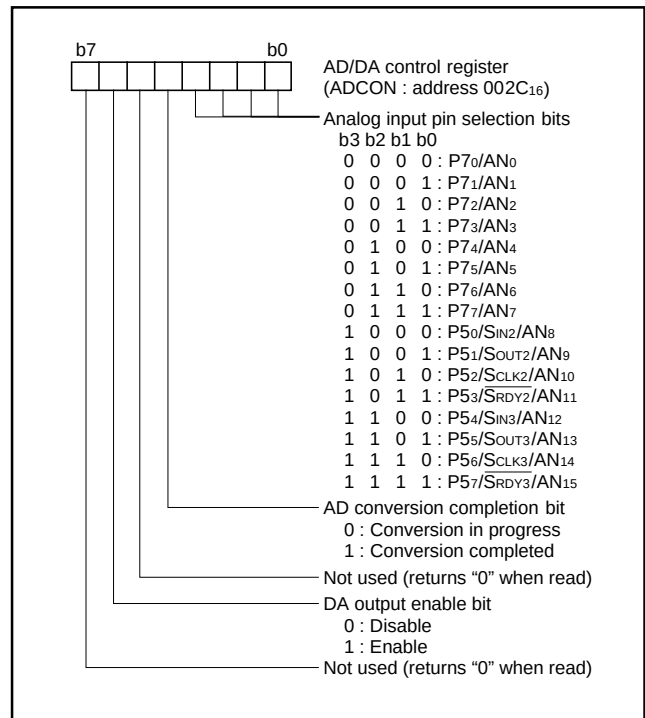


Fig. 23 Structure of A-D control register

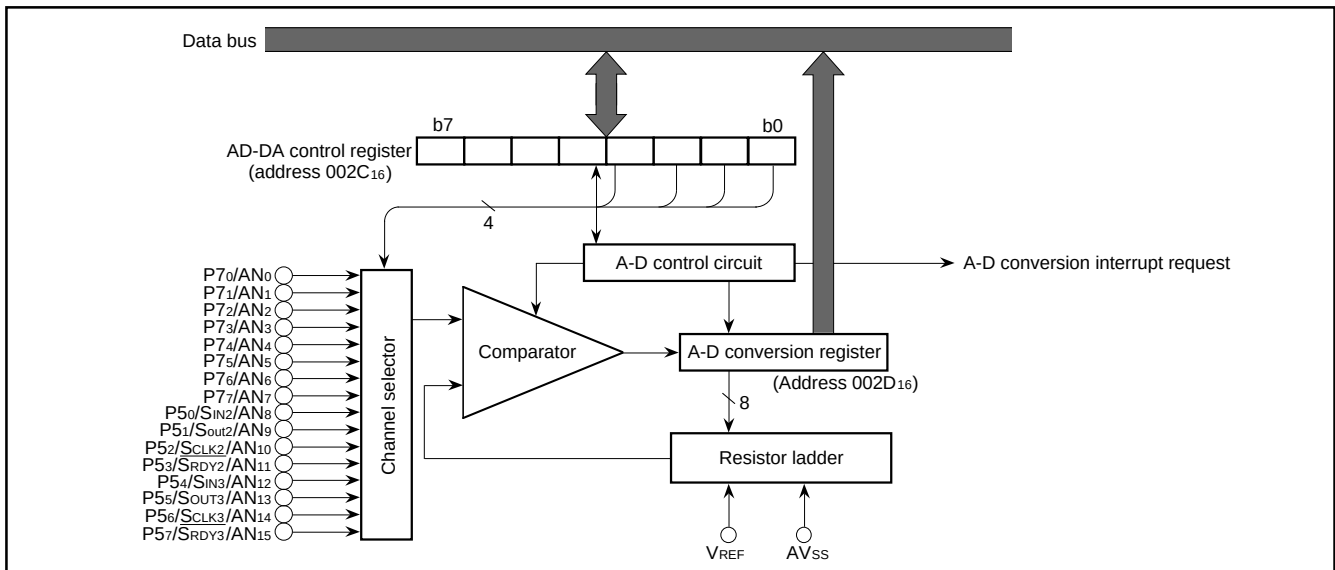


Fig. 24 A-D converter block diagram

D-A CONVERTER

The 3819 group has internal D-A converter with 8-bit resolutions X 1 channel.

D-A conversion is performed by setting the value in the D-A conversion register. The result of D-A conversion is output from the DA pin by setting the DA output enable bit to "1". At this time, the corresponding bit (PB2/DA) of the port PB direction register should be set to "0" (input status).

The output analog voltage V is determined with the value n (n : decimal number) in the D-A conversion register as follows:

$$V = V_{REF} \times n / 256 \quad (n=0 \text{ to } 255)$$

* V_{REF} : the reference voltage

At reset, the D-A conversion register is cleared to "0016", the DA output enable bits are cleared to "0", and the PB2/DA pin goes to high impedance state. The D-A output does not build in a buffer, so connect an external buffer when driving a low-impedance load. Set V_{CC} to 3.0 V or more when using the D-A converter.

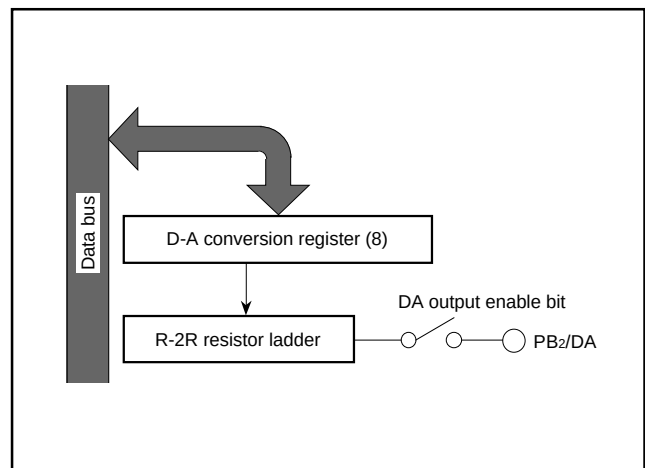


Fig. 25 D-A converter block diagram

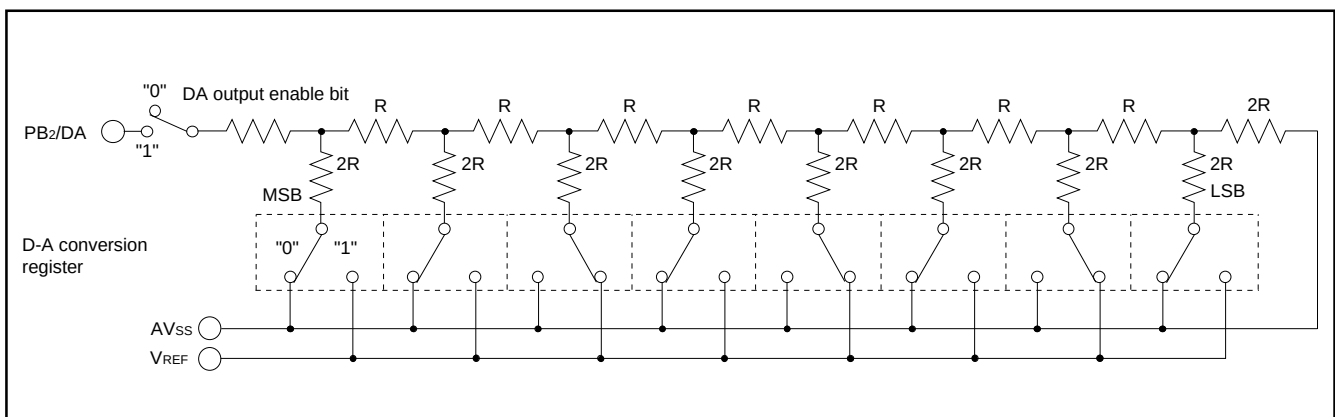


Fig. 26 Equivalent connection circuit of D-A converter

FLD CONTROLLER

The 3819 group has fluorescent display (FLD) drive and control circuits.

The FLD controller consists of the following components:

- 42 pins for segments
- 20 pins for digits
- FLDC mode register 1
- FLDC mode register 2
- FLD data pointer
- FLD data pointer reload register

- Port P0 segment/digit switch register
- Port P2 digit/port switch register
- Port PA segment/port switch register
- Port P8 segment/port switch register
- 96-byte FLD automatic display RAM

The segment pins can be used from 16 up to 42 pins (maximum) and the digit pins can be used from 6 up to 16 pins (maximum). The segment and the digit pins can be used up to 52 pins (maximum) in total.

In the FLD automatic display mode ports P12 to P17 become digit pins DIG10 to DIG15 automatically.

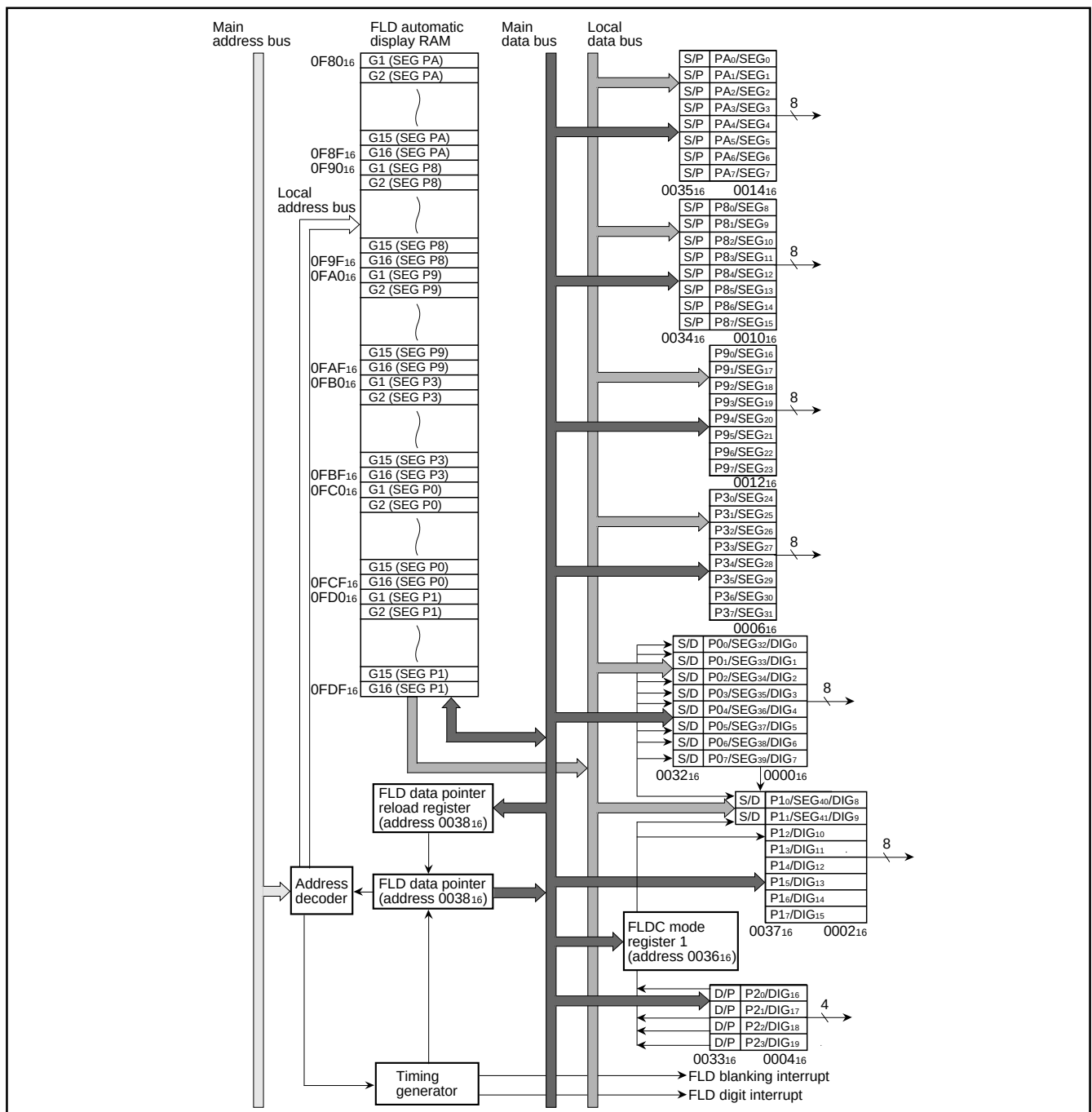


Fig. 27 FLD control circuit block diagram

FLDC Mode Registers (FLDM 1, FLDM 2) 0036₁₆, 0037₁₆

The FLDC mode register 1 (address 0036₁₆) and FLDC mode register 2 (address 0037₁₆) are a seven bit register and an eight bit

register respectively which are used to control the FLD automatic display and set the blanking time T_{scan} for key-scan.

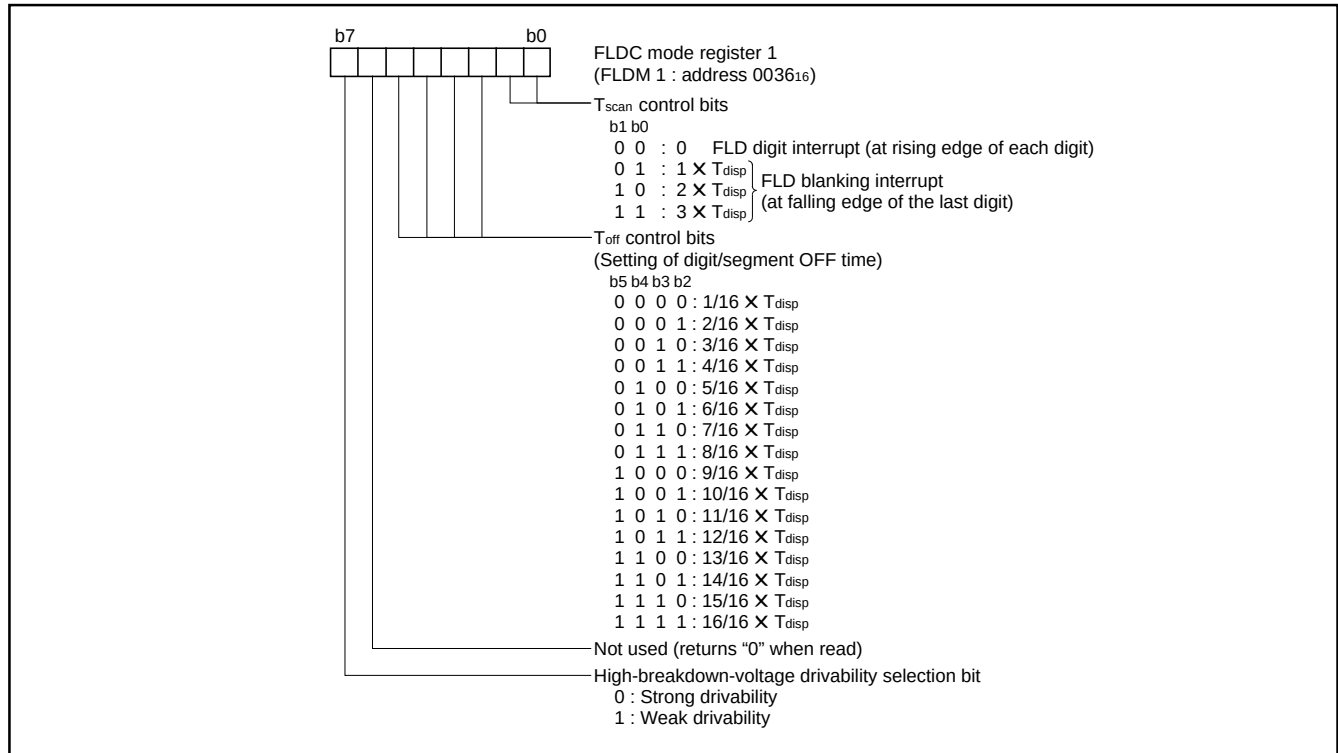


Fig. 28 Structure of FLDC mode register 1

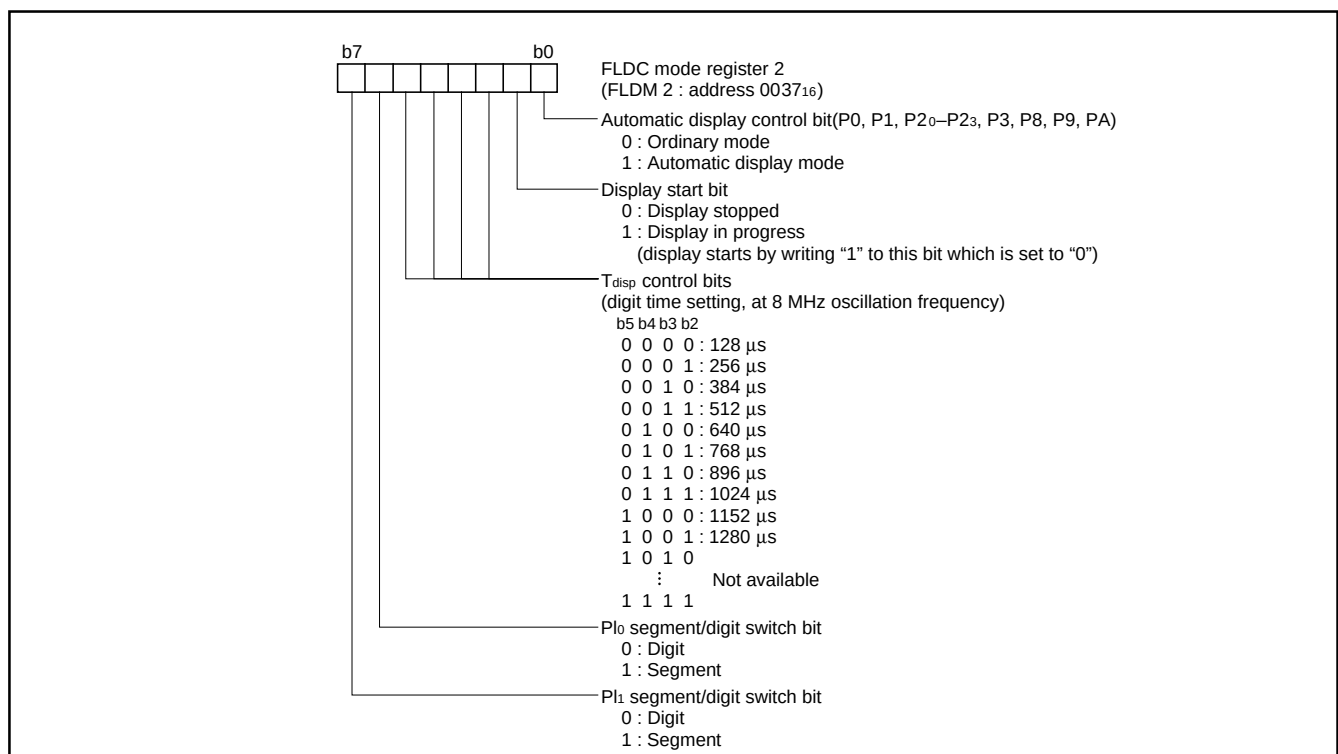


Fig. 29 Structure of FLDC mode register 2

● Pins for FLD Automatic Display

Ports P0, P1, P20–P23, P3, P8, P9, and PA is selected for the FLD automatic display function by setting the automatic display control bit of the FLDC mode register 2 (address 003716) to “1”.

When using the FLD automatic display mode, set the number of segments and digits for each port.

Table 4. Pins in FLD automatic display mode

Port Name	Automatic Display Pins	Setting Method
PA0–PA7	SEG0–SEG7 or PA0–PA7	The individual bits of the segment/port switch register (address 003516) can be set each pin to either segment (“1”) or general-purpose I/O port (“0”).
P80–P87	SEG8–SEG15 or P80–P87	The individual bits of the segment/port switch register (address 003416) can be used to set each pin to either segment (“1”) or general-purpose I/O port (“0”).
P90–P97	SEG16–SEG23	None (segment only)
P30–P37	SEG24–SEG31	None (segment only)
P00–P07 P10, P11	SEG32–SEG41 or DIG0–DIG9	The individual bits of the segment/digit switch register (address 003216) and the bit 6, 7 of the FLDC mode register 2 can be used to set each pin to segment (“1”) or digit (“0”). (Note)
P12–P17	DIG10–DIG15	None (digit only)
P20–P23	DIG16–DIG19 or P20–P23	The individual bits of the digit/port switch register (address 003316) can be used to set each pin to digit (“1”) or general-purpose output port (“0”). (Note)

Note : Be sure to set digits in sequence.

Number of segments Number of digits	24 8	30 10	36 16	Number of segments Number of digits	24 8	30 10	36 16																																																																																																
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0	P2 ₃																																																																																																						
1	DIG ₁₆ →G ₄																																																																																																						
1	DIG ₁₇ →G ₃																																																																																																						
1	DIG ₁₈ →G ₂																																																																																																						
1	DIG ₁₉ →G ₁																																																																																																						
1	DIG ₁₆ →G ₄																																																																																																						
1	DIG ₁₇ →G ₃																																																																																																						
1	DIG ₁₈ →G ₂																																																																																																						
1	DIG ₁₉ →G ₁																																																																																																						

Fig. 30 Segment/digit setting example

● FLD Automatic Display RAM

The FLD automatic display RAM area is the 96 bytes from addresses 0F80₁₆ to 0FDF₁₆. The FLD automatic display RAM area can store 6-byte segment data up to 16 digits (maximum). Addresses 0F80₁₆ to 0F8F₁₆ are used for PA segment data, addresses 0F90₁₆ to 0F9F₁₆ are used for P8 segment data, addresses 0FA0₁₆ to 0FAF₁₆ are used for P9 segment data, addresses 0FB0₁₆ to 0FBF₁₆ are used for P3 segment data, addresses 0FC0₁₆ to 0FCF₁₆ are used for P0 segment data, and addresses 0FD0 to 0FDF₁₆ are used for P1 segment data.

FLD Data Pointer and FLD Data Pointer Reload Register

(FLDDP) 0038₁₆

Both the FLD data pointer and FLD data pointer reload register are 7-bit registers allocated at address 0038₁₆. When writing data to this address, the data is written to the FLD data pointer reload register, when reading data from this address, the value in the FLD data pointer is read.

The FLD data pointer indicates the data address in the FLD automatic display RAM to be transferred to a segment. The FLD data pointer reload register indicates the first digit address of the most significant segment.

The value which adds 0F80₁₆ to these data is actual address in memory.

The contents of the FLD data pointer indicate the first address of segment P1(the contents of the FLD data pointer reload register) at the start of automatic display. The FLDC data pointer content changes repeatedly as follows: when transferring the segment P1 data to the segment, the content decreases by -16; when transferring the segment P0 data, it decreases by -16; when transferring the segment P3 data, it decreases by -16; when transferring the segment P9 data, it decreases by -16; when transferring the segment P8 data, it decreases by -16; when transferring the segment PA data, it increases by +79. Once it reaches "00", at the next timing the value in the FLD data pointer reload register is transferred to the FLD data pointer. In this way, the 6-byte data of P1, P0, P3, P9, P8 and PA segments for 1 digit are transferred.

Address \ Bit	7	6	5	4	3	2	1	0	
0F80 ₁₆	SEG ₇	SEG ₆	SEG ₅	SEG ₄	SEG ₃	SEG ₂	SEG ₁	SEG ₀	← The last digit (The last data of segment PA)
0F81 ₁₆	SEG ₇	SEG ₆	SEG ₅	SEG ₄	SEG ₃	SEG ₂	SEG ₁	SEG ₀	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	Segment PA data area
0F8E ₁₆	SEG ₇	SEG ₆	SEG ₅	SEG ₄	SEG ₃	SEG ₂	SEG ₁	SEG ₀	
0F8F ₁₆	SEG ₇	SEG ₆	SEG ₅	SEG ₄	SEG ₃	SEG ₂	SEG ₁	SEG ₀	← The last digit (The last data of segment P8)
0F90 ₁₆	SEG ₁₅	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	SEG ₈	
0F91 ₁₆	SEG ₁₅	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	SEG ₈	Segment P8 data area
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
0F9E ₁₆	SEG ₁₅	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	SEG ₈	← The last digit (The last data of segment P9)
0F9F ₁₆	SEG ₁₅	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	SEG ₈	
0FA0 ₁₆	SEG ₂₃	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	SEG ₁₆	← The last digit (The last data of segment P9)
0FA1 ₁₆	SEG ₂₃	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	SEG ₁₆	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	Segment P9 data area
0FAE ₁₆	SEG ₂₃	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	SEG ₁₆	
0FAF ₁₆	SEG ₂₃	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	SEG ₁₆	← The last digit (The last data of segment P3)
0FB0 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	
0FB1 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	Segment P3 data area
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
0FBE ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	← The last digit (The last data of segment P0)
0FBF ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	
0FC0 ₁₆	SEG ₃₉	SEG ₃₈	SEG ₃₇	SEG ₃₆	SEG ₃₅	SEG ₃₄	SEG ₃₃	SEG ₃₂	← The last digit (The last data of segment P0)
0FC1 ₁₆	SEG ₃₉	SEG ₃₈	SEG ₃₇	SEG ₃₆	SEG ₃₅	SEG ₃₄	SEG ₃₃	SEG ₃₂	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	Segment P0 data area
0FCE ₁₆	SEG ₃₉	SEG ₃₈	SEG ₃₇	SEG ₃₆	SEG ₃₅	SEG ₃₄	SEG ₃₃	SEG ₃₂	
0FCF ₁₆	SEG ₃₉	SEG ₃₈	SEG ₃₇	SEG ₃₆	SEG ₃₅	SEG ₃₄	SEG ₃₃	SEG ₃₂	← The last digit (The last data of segment P1)
0FD0 ₁₆							SEG ₄₁	SEG ₄₀	
0FD1 ₁₆							SEG ₄₁	SEG ₄₀	Segment P1 data area
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
0FDE ₁₆							SEG ₄₁	SEG ₄₀	
0FDF ₁₆							SEG ₄₁	SEG ₄₀	

Fig. 31 FLD automatic display RAM and bit allocation

● Data Setup

When data is stored in the FLD automatic display RAM, the last data of segment PA is stored at address 0F80₁₆, the last data of segment P8 is stored at address 0F90₁₆, the last data of segment P9 is stored at address 0FA0₁₆, the last data of segment P3 is stored at address 0FB0₁₆, the last data of segment P0 is stored at address 0FC0₁₆, and the last data of segment P1 is stored at address 0FD0₁₆ to allocate in se-

quence from the last data respectively. The first data of the segment PA, P8, P9, P3, P0, and P1 is stored at an address which adds the value of (the digit number-1) to the corresponding address 0F80₁₆, 0F90₁₆, 0FA0₁₆, 0FB0₁₆, 0FC0₁₆, and 0FD0₁₆.

Set the low-order 4 bits of the FLD data pointer reload register to the value given by the number of digits-1. "1" is always written to bit 6 and bit 4, and "0" is always written to bit 5. Note that "0" is always read from bits 6, 5 and 4 when reading.

For 30 segments and 15 digits
(FLD data pointer reload register = 14)

Address \ Bit	7	6	5	4	3	2	1	0
0F80 ₁₆								
0F81 ₁₆								
0F82 ₁₆								
0F83 ₁₆								
0F84 ₁₆								
0F85 ₁₆								
0F86 ₁₆								
0F87 ₁₆								
0F88 ₁₆								
0F89 ₁₆								
0F8A ₁₆								
0F8B ₁₆								
0F8C ₁₆								
0F8D ₁₆								
0F8E ₁₆								
0F8F ₁₆								
0F90 ₁₆								
0F91 ₁₆								
0F92 ₁₆								
0F93 ₁₆								
0F94 ₁₆								
0F95 ₁₆								
0F96 ₁₆								
0F97 ₁₆								
0F98 ₁₆								
0F99 ₁₆								
0F9A ₁₆								
0F9B ₁₆								
0F9C ₁₆								
0F9D ₁₆								
0F9E ₁₆								
0F9F ₁₆								
0FA0 ₁₆								
0FA1 ₁₆								
0FA2 ₁₆								
0FA3 ₁₆								
0FA4 ₁₆								
0FA5 ₁₆								
0FA6 ₁₆								
0FA7 ₁₆								
0FA8 ₁₆								
0FA9 ₁₆								
0FAA ₁₆								
0FAB ₁₆								
0FAC ₁₆								
0FAD ₁₆								
0FAE ₁₆								
0FAF ₁₆								

Note :  Shaded areas are used.

For 30 segments and 15 digits
(FLD data pointer reload register = 14)

Address \ Bit	7	6	5	4	3	2	1	0
0FB0 ₁₆								
0FB1 ₁₆								
0FB2 ₁₆								
0FB3 ₁₆								
0FB4 ₁₆								
0FB5 ₁₆								
0FB6 ₁₆								
0FB7 ₁₆								
0FB8 ₁₆								
0FB9 ₁₆								
0FBA ₁₆								
0FBB ₁₆								
0FBC ₁₆								
0FBD ₁₆								
0FBE ₁₆								
0FBF ₁₆								
0FC0 ₁₆								
0FC1 ₁₆								
0FC2 ₁₆								
0FC3 ₁₆								
0FC4 ₁₆								
0FC5 ₁₆								
0FC6 ₁₆								
0FC7 ₁₆								
0FC8 ₁₆								
0FC9 ₁₆								
0FCA ₁₆								
0FCB ₁₆								
0FCC ₁₆								
0FCD ₁₆								
0FCE ₁₆								
0FCF ₁₆								
0FD0 ₁₆								
0FD1 ₁₆								
0FD2 ₁₆								
0FD3 ₁₆								
0FD4 ₁₆								
0FD5 ₁₆								
0FD6 ₁₆								
0FD7 ₁₆								
0FD8 ₁₆								
0FD9 ₁₆								
0FDA ₁₆								
0FDB ₁₆								
0FDC ₁₆								
0FDD ₁₆								
0FDE ₁₆								
0FDF ₁₆								

Fig. 32 Example of using the FLD automatic display RAM (1)

For 42 segments and 8 digits (FLD data pointer reload register = 7)									
Address	Bit	7	6	5	4	3	2	1	0
0F80 ₁₆									
0F81 ₁₆									
0F82 ₁₆									
0F83 ₁₆									
0F84 ₁₆									
0F85 ₁₆									
0F86 ₁₆									
0F87 ₁₆									
0F88 ₁₆									
0F89 ₁₆									
0F8A ₁₆									
0F8B ₁₆									
0F8C ₁₆									
0F8D ₁₆									
0F8E ₁₆									
0F8F ₁₆									
0F90 ₁₆									
0F91 ₁₆									
0F92 ₁₆									
0F93 ₁₆									
0F94 ₁₆									
0F95 ₁₆									
0F96 ₁₆									
0F97 ₁₆									
0F98 ₁₆									
0F99 ₁₆									
0F9A ₁₆									
0F9B ₁₆									
0F9C ₁₆									
0F9D ₁₆									
0F9E ₁₆									
0F9F ₁₆									
0FA0 ₁₆									
0FA1 ₁₆									
0FA2 ₁₆									
0FA3 ₁₆									
0FA4 ₁₆									
0FA5 ₁₆									
0FA6 ₁₆									
0FA7 ₁₆									
0FA8 ₁₆									
0FA9 ₁₆									
0FAA ₁₆									
0FAB ₁₆									
0FAC ₁₆									
0FAD ₁₆									
0FAE ₁₆									
0FAF ₁₆									

Note :  Shaded areas are used.

For 42 segments and 8 digits (FLD data pointer reload register = 7)									
Address	Bit	7	6	5	4	3	2	1	0
0FB0 ₁₆									
0FB1 ₁₆									
0FB2 ₁₆									
0FB3 ₁₆									
0FB4 ₁₆									
0FB5 ₁₆									
0FB6 ₁₆									
0FB7 ₁₆									
0FB8 ₁₆									
0FB9 ₁₆									
0FBA ₁₆									
0FBB ₁₆									
0FBC ₁₆									
0FBD ₁₆									
0FBE ₁₆									
0FBF ₁₆									
0FC0 ₁₆									
0FC1 ₁₆									
0FC2 ₁₆									
0FC3 ₁₆									
0FC4 ₁₆									
0FC5 ₁₆									
0FC6 ₁₆									
0FC7 ₁₆									
0FC8 ₁₆									
0FC9 ₁₆									
0FCA ₁₆									
0FCB ₁₆									
0FCC ₁₆									
0FCD ₁₆									
0FCE ₁₆									
0FCF ₁₆									
0FD0 ₁₆									
0FD1 ₁₆									
0FD2 ₁₆									
0FD3 ₁₆									
0FD4 ₁₆									
0FD5 ₁₆									
0FD6 ₁₆									
0FD7 ₁₆									
0FD8 ₁₆									
0FD9 ₁₆									
0FDA ₁₆									
0FDB ₁₆									
0FDC ₁₆									
0FDD ₁₆									
0FDE ₁₆									
0FDF ₁₆									

Fig. 33 Example of using the FLD automatic display RAM (2) (continued)

● Timing Setting

The digit time (T_{disp}) can be set with the FLDC mode register 2 (address 0037₁₆). The T_{scan} and digit/segment OFF time (T_{off}) can be set with the FLDC mode register 1 (address 0036₁₆). Note that flickering will occur if the repetition frequency ($1/(T_{\text{disp}} \times \text{number of digits} + T_{\text{scan}})$) is an integral multiple of the digit timing T_{disp} .

● FLD Automatic Display Start

To perform FLD automatic display, set the following registers.

- Port P0 segment/digit switch register
- Port P2 digit/port switch register
- Port P8 segment/port switch register
- Port PA segment/port switch register
- FLDC mode register 1
- FLDC mode register 2
- FLD data pointer

Automatic display mode is selected by writing "1" to the bit 0 of the FLDC mode register 2 (address 0037₁₆), and the automatic display is started by writing "1" to the bit 1.

During automatic display bit 1 of the FLDC mode register 2 always keeps "1", automatic display can be interrupted by writing "0" to the bit 1.

● Key-scan

If key-scan is performed with the segment during the key-scan blanking period T_{scan} , take the following sequence:

1. Write "0" to the bit 0 (automatic display control bit) of the FLDC mode register 2 (address 0037₁₆).
2. Set the port corresponding to the segment for key-scan to the output port.
3. Perform the key-scan.
4. After the key-scan is performed, write "1" (automatic display mode) to the bit 0 of FLDC mode register 2 (address 0037₁₆).

Note on performance of key-scan in the above 1 to 4 sequence.

1. Do not write "0" to the bit 1 of FLDC mode register 2 (address 0037₁₆).
2. Do not write "1" to the port corresponding to the digit.

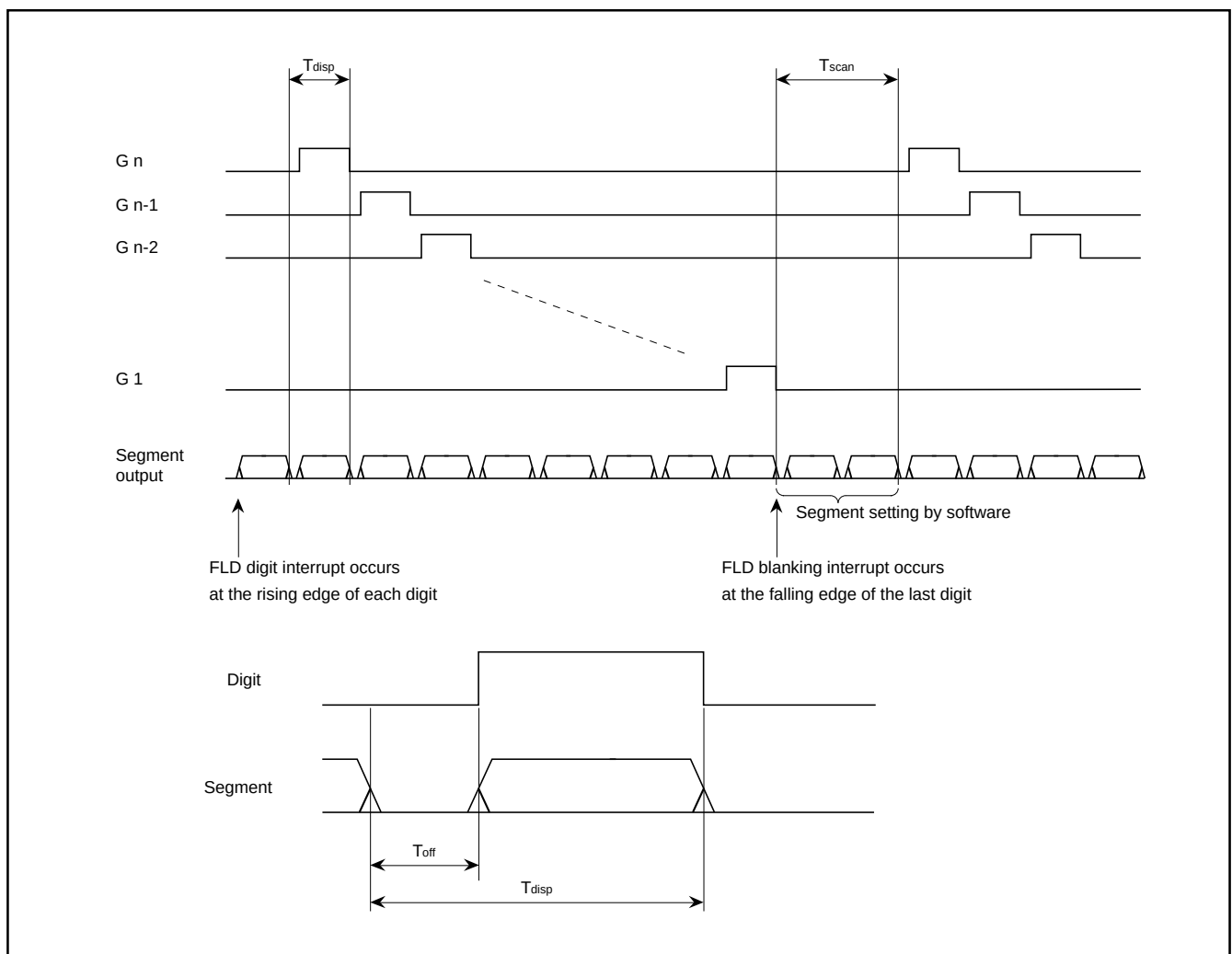


Fig. 34 FLDC timing

INTERRUPT INTERVAL DETERMINATION FUNCTION

The 3819 group builds in an interrupt interval determination circuit. This interrupt interval determination circuit has an 8-bit binary up counter. Using this counter, it determines a duration of time from the rising transition (falling transition) of an input signal pulse on the P42/INT2 pin to the rising transition (falling transition) of the signal pulse that is input next.

How to determine the interrupt interval is described below.

- ① Enable the INT2 interrupt by setting the bit 2 of the interrupt control register 1 (address 003E16). Select the rising interval or falling interval by setting the bit 2 of the interrupt edge selection register (address 003A16).
- ② Set the bit 0 of the interrupt interval determination control register (address 003116) to "1" (interrupt interval determination operating).
- ③ Select the sampling clock of 8-bit binary up counter by setting the bit 1 of the interrupt interval determination control register. When writing "0", $f(X_{IN})/256$ is selected (the sampling interval: 32 μ s at $f(X_{IN}) = 8.38$ MHz); when "1", $f(X_{IN})/512$ is selected (the sampling interval: 64 μ s at $f(X_{IN}) = 8.38$ MHz).
- ④ When the signal of polarity which is set on the INT2 pin (rising or falling transition) is input, the 8-bit binary up counter starts counting up of the selected counter sampling clock.
- ⑤ When the signal of polarity above ④ is input again, the value of the 8-bit binary up counter is transferred to the interrupt interval

determination register (address 003016), and the remote control interrupt request occurs. Immediately after that, the 8-bit binary up counter is cleared to "0016". The 8-bit binary up counter continues to count up again from "0016".

- ⑥ When count value reaches "FF16", the 8-bit binary up counter stops counting up. Then, simultaneously when the next counter sampling clock is input, the counter sets value "FF16" to the interrupt interval determination register to generate the counter overflow interrupt request.

Noise filter

The P42/INT2 pin builds in the noise filter.

The noise filter operation is described below.

- ① Select the sampling clock of the input signal with the bits 2 and 3 of the interrupt interval determination control register. When not using the noise filter, set "002".
- ② The P42/INT2 input signal is sampled in synchronization with the selected clock. When sampling the same level signal in series, the signal is recognized as the interrupt signal, and the interrupt request occurs.

When setting the bit 4 of interrupt interval determination control register to "1", the interrupt request can occur at both rising and falling edges.

When using the noise filter, set the minimum pulse width of the INT2 input signal to 2 cycles or more.

Note : In the low-speed mode (CM7=1), the interrupt interval determination function can not operate.

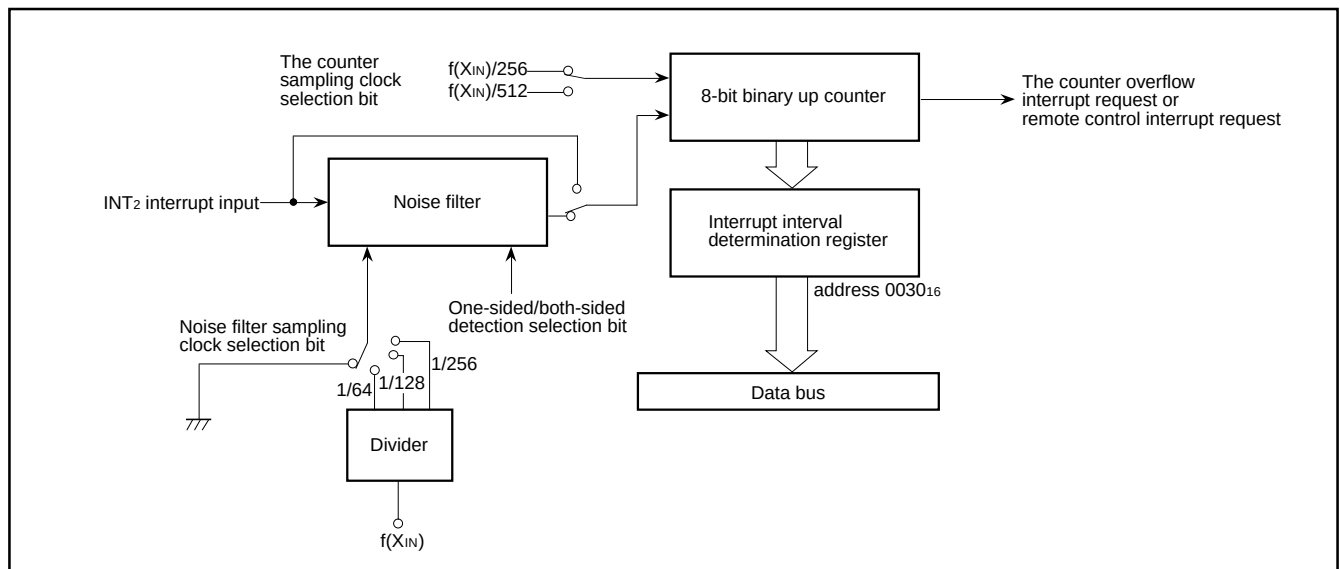


Fig. 35 Block diagram of interrupt interval determination circuit

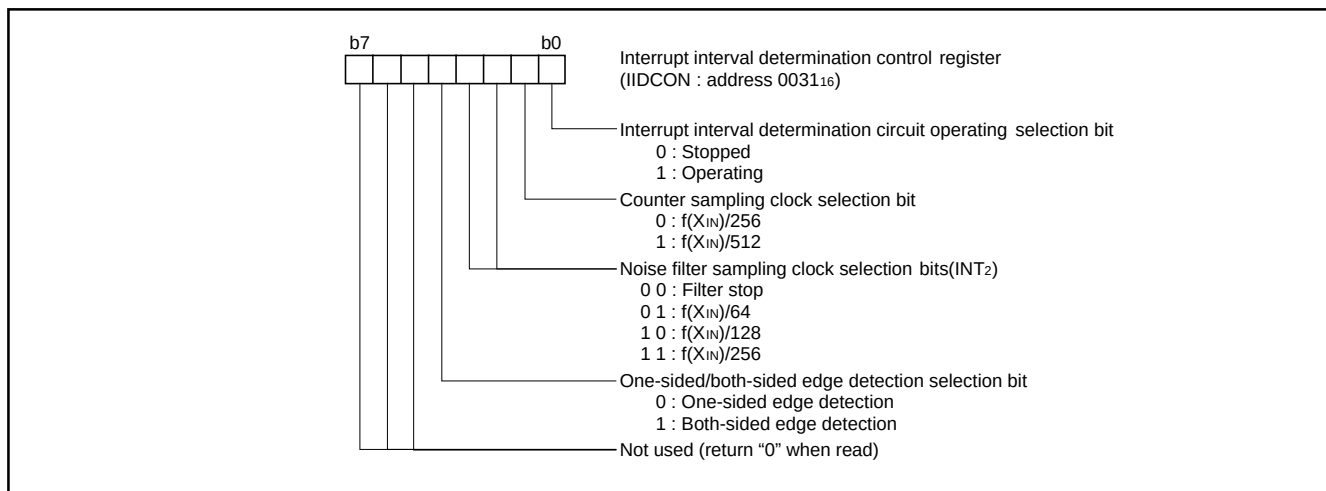


Fig. 36 Structure of interrupt interval determination control register

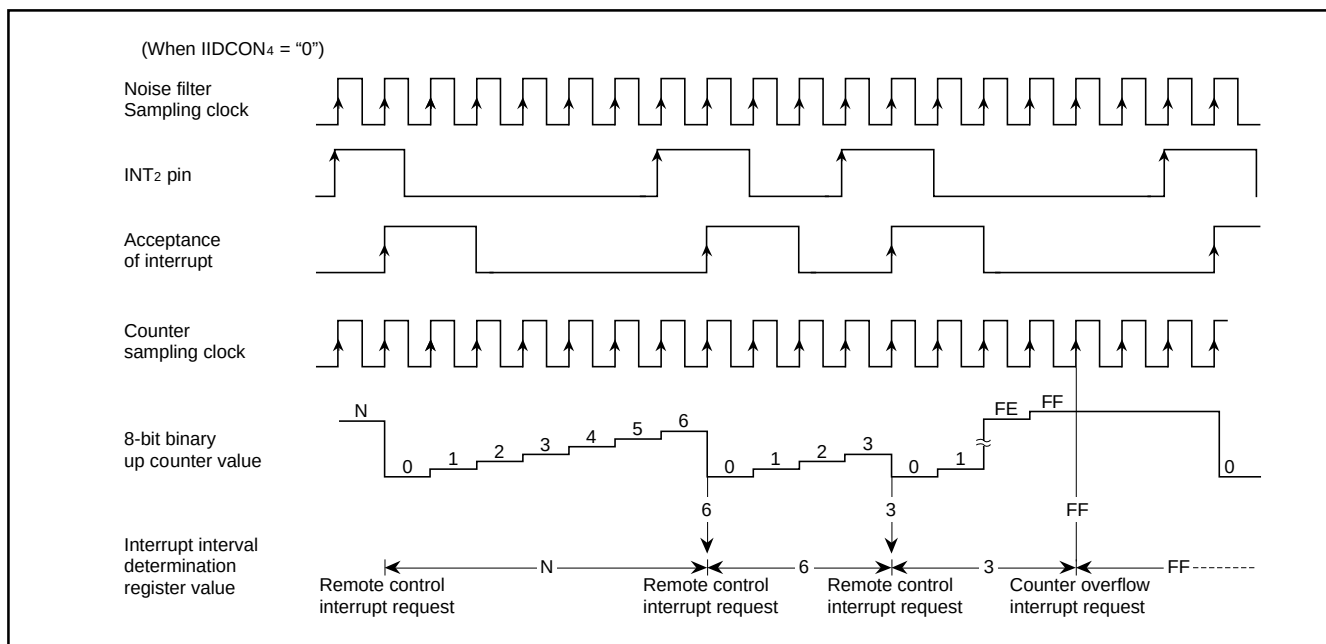


Fig. 37 Interrupt interval determination operation example (at rising edge active)

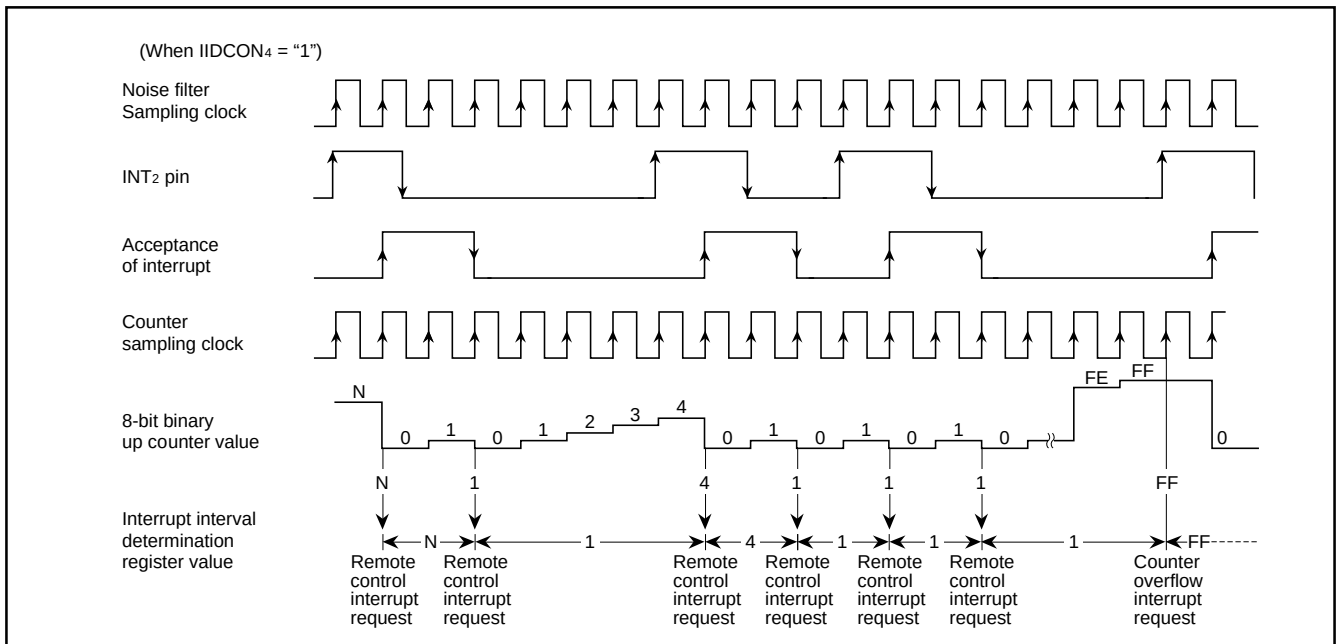


Fig. 38 Interrupt interval determination operation example (at both-sided edge active)

ZERO CROSS DETECTION CIRCUIT

The zero cross detection circuit compares the voltage applied to P45/INT1/ZCR pin and Vss. The result can be read from the zero cross detection circuit input bit (bit 7) of the zero cross detection control register. It is set to "1" when the input voltage is higher than Vss and to "0" when it is lower than Vss. The input signal to P45/INT1/ZCR pin can select to either pass through the zero cross detection comparator or not to do.

When using 100 V AC as input signal, insert an external circuit between it and P45/INT1/ZCR pin. Set the input current limiting resistors used in the external circuit to a value which satisfies the absolute maximum rating of port P45.

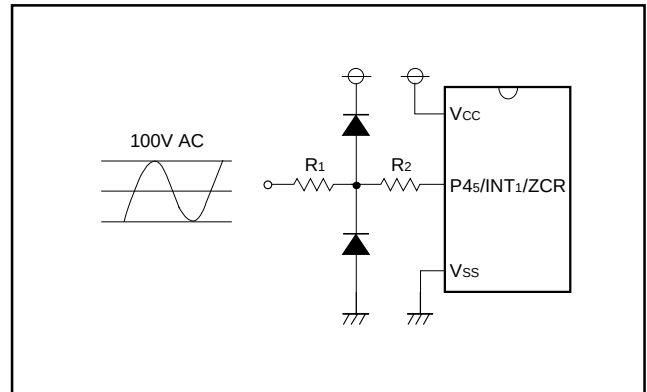


Fig. 39 External circuit example for zero cross detection

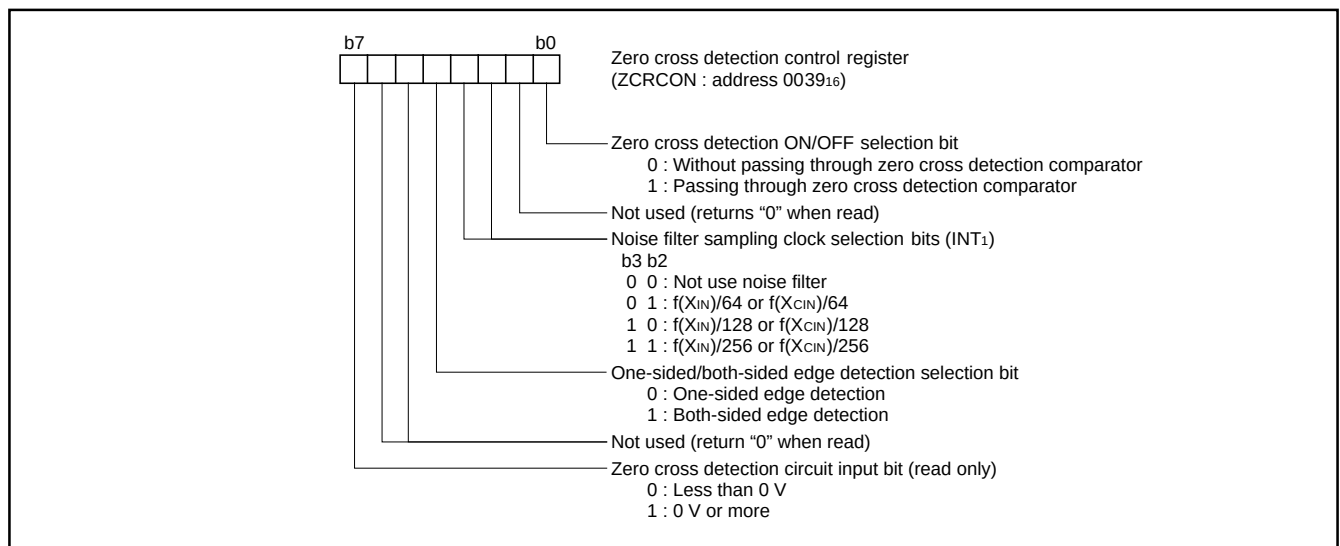


Fig. 40 Structure of zero cross detection control register

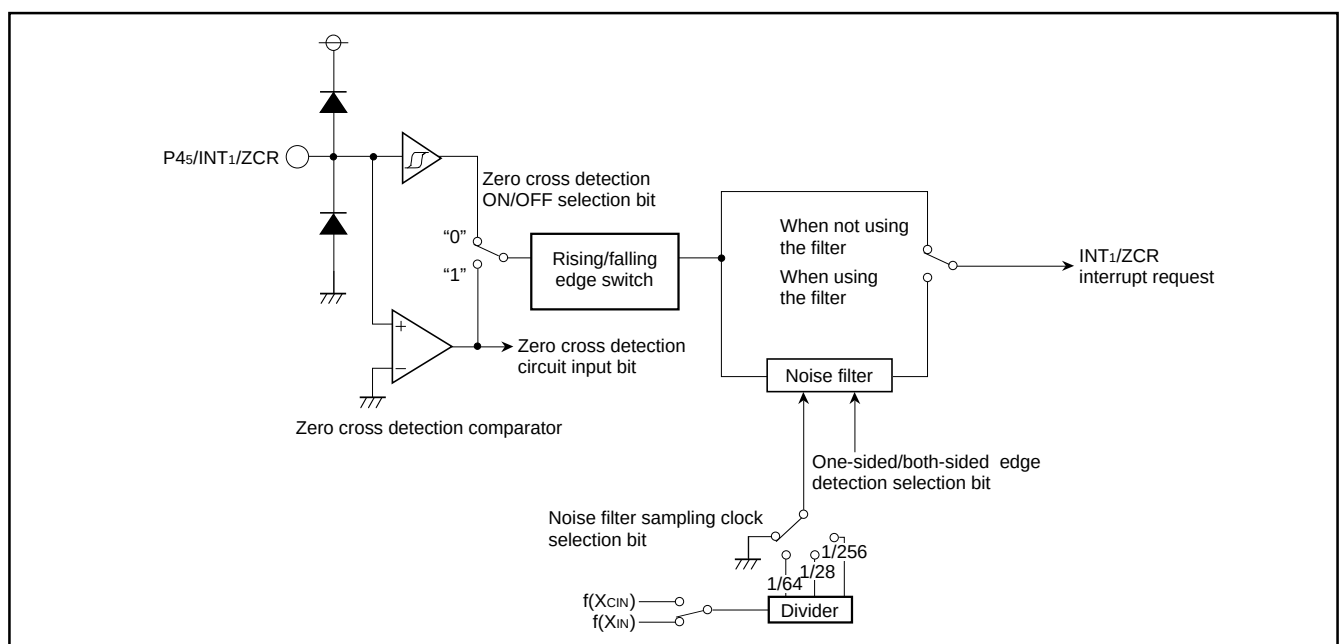


Fig. 41 Block diagram of zero cross detection circuit

NOISE FILTER

The noise filter uses a sampling clock to remove the noise component digitally from the input signal of P45/INT1/ZCR pin. The sampling clock can be selected from 8 μ s, 16 μ s, or 32 μ s (at $f(X_{IN}) = 8.38$ MHz) and this is used to change the noise component to be removed. It is also possible to generate an internal trigger and INT1/ZCR interrupt request directly without passing through

the noise filter. When passing through the noise filter, either both-sided edge detection or one-sided edge detection can be selected as the interrupt request generating source. The zero cross detection control register is used for this selection. Furthermore, switch between rising edge and falling edge is performed with the bit 1 of the interrupt edge selection register (address 003A16).

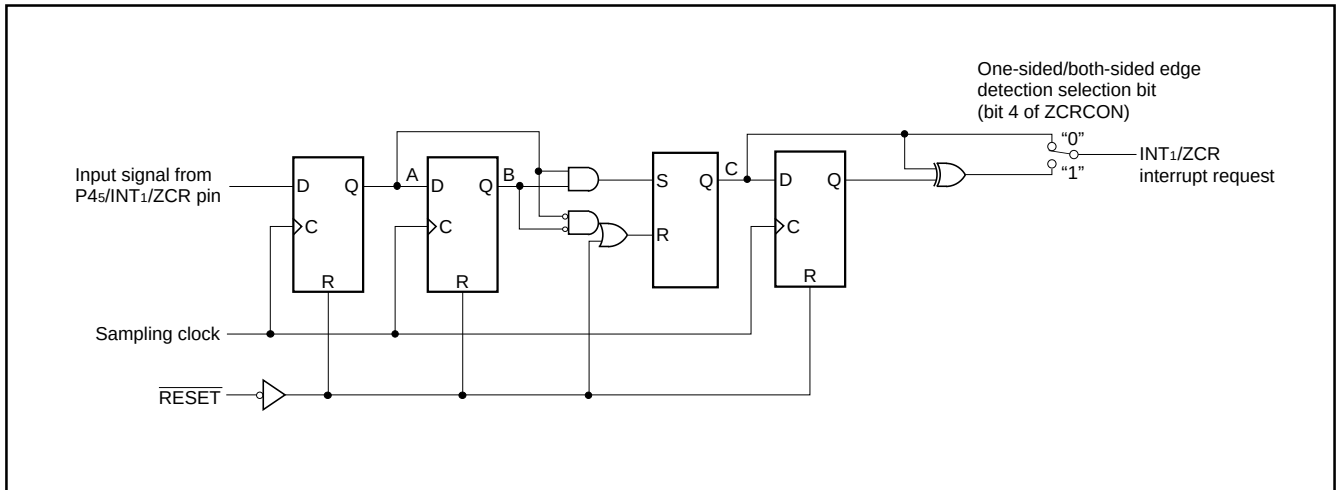


Fig. 42 Noise filter circuit diagram

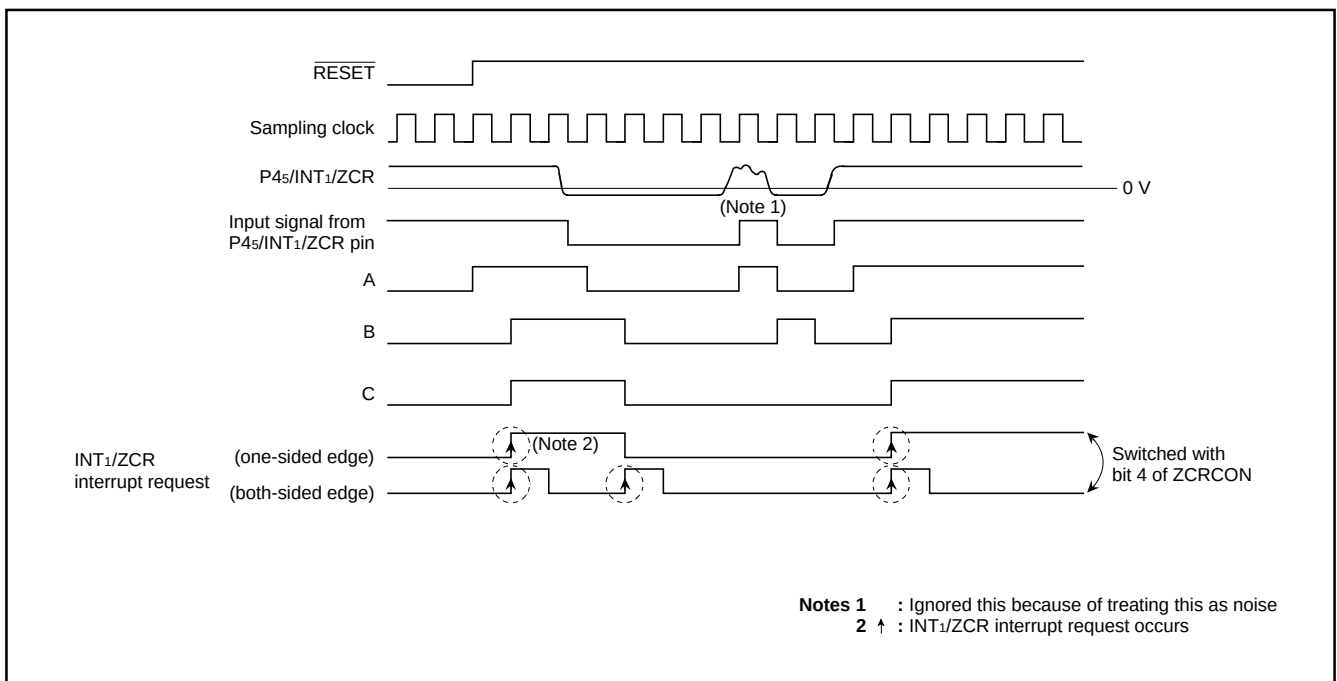


Fig. 43 Timing of noise filter circuit

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between 2.8 V and 5.5 V, and X_{IN} oscillation is stable), reset is released. In order to give the X_{IN} clock time to stabilize, internal operation does not begin until after about 4000 X_{IN} clock cycles (256 cycles of $f(X_{\text{IN}})/16$) are completed. After the reset is completed, the program starts from the address contained in address FFFD_{16} (high-order) and address FFFC_{16} (low-order). Make sure that the reset input voltage is 0.5 V or less for 2.8 V of V_{CC} .

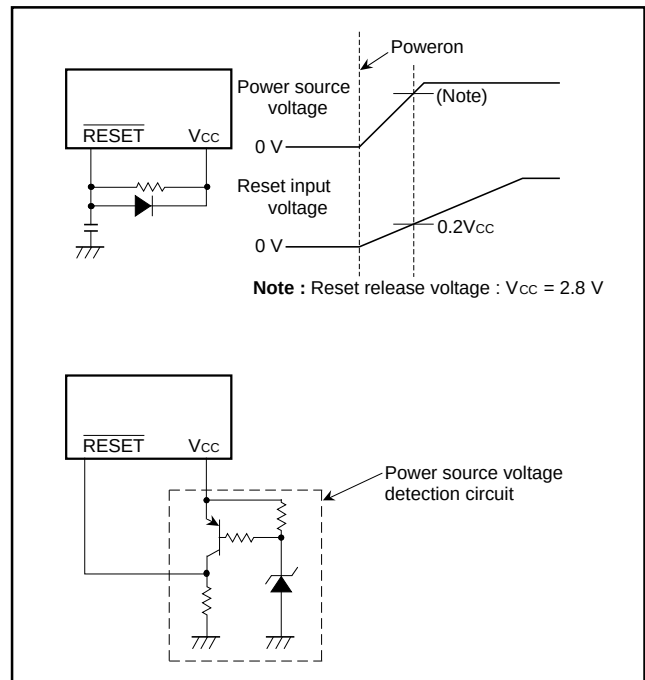


Fig. 44 Example of reset circuit

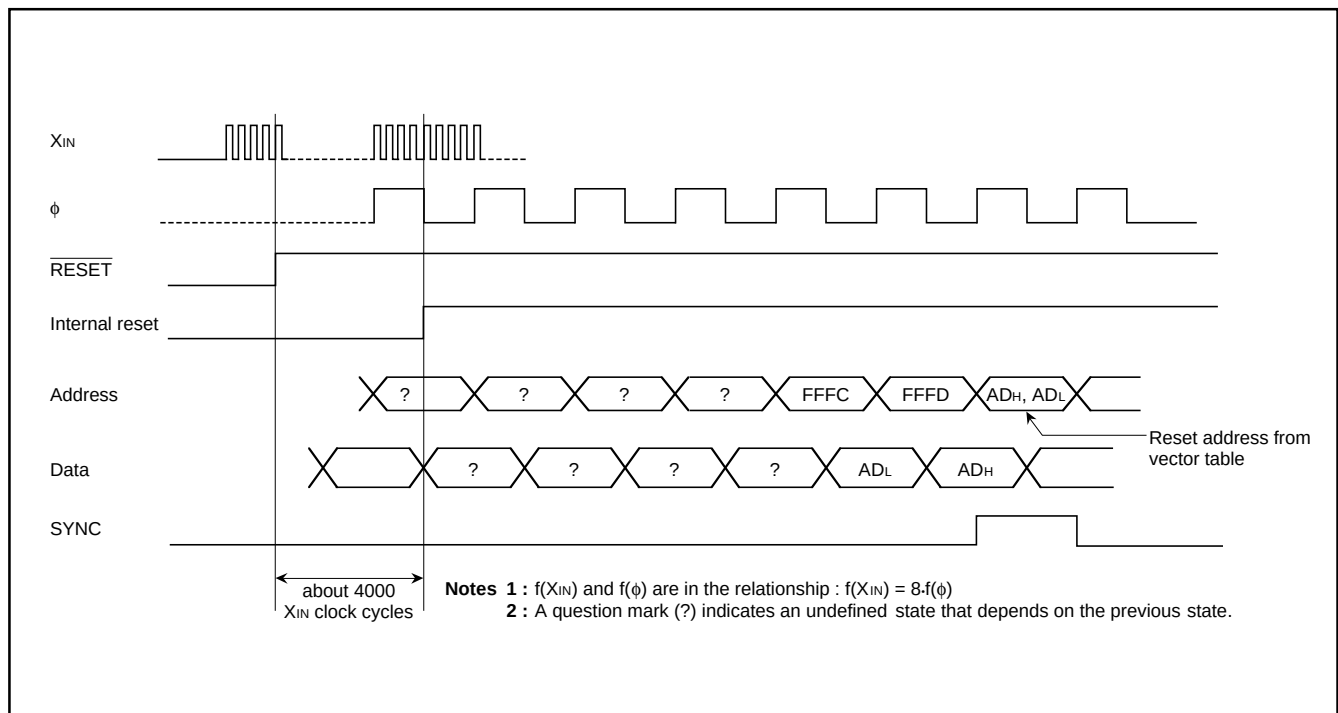


Fig. 45 Reset sequence

	Address	Register contents		Address	Register contents
(1) Port P0	(0000 ₁₆)...	00 ₁₆	(31) Timer 6	(0025 ₁₆)...	FF ₁₆
(2) Port P1	(0002 ₁₆)...	00 ₁₆	(32) Timer 12 mode register	(0028 ₁₆)...	00 ₁₆
(3) Port P2	(0004 ₁₆)...	00 ₁₆	(33) Timer 34 mode register	(0029 ₁₆)...	00 ₁₆
(4) Port P2 direction register	(0005 ₁₆)...	0F ₁₆	(34) Timer 56 mode register	(002A ₁₆)...	00 ₁₆
(5) Port P3	(0006 ₁₆)...	00 ₁₆	(35) D-A conversion register	(002B ₁₆)...	00 ₁₆
(6) Port P4	(0008 ₁₆)...	00 ₁₆	(36) AD/DA control register	(002C ₁₆)...	10 ₁₆
(7) Port P4 direction register	(0009 ₁₆)...	00 ₁₆	(37) Interrupt interval determination	(0031 ₁₆)...	00 ₁₆
(8) Port P5	(000A ₁₆)...	00 ₁₆	control register		
(9) Port P5 direction register	(000B ₁₆)...	00 ₁₆	(38) Port P0 segment/digit	(0032 ₁₆)...	00 ₁₆
(10) Port P6	(000C ₁₆)...	00 ₁₆	switch register		
(11) Port P6 direction register	(000D ₁₆)...	00 ₁₆	(39) Port P2 digit/port switching	(0033 ₁₆)...	00 ₁₆
(12) Port P7	(000E ₁₆)...	00 ₁₆	register		
(13) Port P7 direction register	(000F ₁₆)...	00 ₁₆	(40) Port P8 segment/port	(0034 ₁₆)...	00 ₁₆
(14) Port P8	(0010 ₁₆)...	00 ₁₆	switch register		
(15) Port P8 direction register	(0011 ₁₆)...	00 ₁₆	(41) Port PA segment/port switch	(0035 ₁₆)...	00 ₁₆
(16) Port P9	(0012 ₁₆)...	00 ₁₆	(42) FLDC mode register 1	(0036 ₁₆)...	00 ₁₆
(17) Port PA	(0014 ₁₆)...	00 ₁₆	(43) FLDC mode register 2	(0037 ₁₆)...	00 ₁₆
(18) Port PA direction register	(0015 ₁₆)...	00 ₁₆	(44) Zero cross detection control	(0039 ₁₆)...	00 ₁₆
(19) Port PB	(0016 ₁₆)...	00 ₁₆	register		
(20) Port PB direction register	(0017 ₁₆)...	00 ₁₆	(45) Interrupt edge selection register	(003A ₁₆)...	00 ₁₆
(21) Serial I/O1 control register	(0019 ₁₆)...	00 ₁₆	(46) CPU mode register	(003B ₁₆)...	0 1 0 0 1 0 0 0
(22) Serial I/O automatic transfer	(001A ₁₆)...	00 ₁₆	(47) Interrupt request register 1	(003C ₁₆)...	00 ₁₆
control register			(48) Interrupt request register 2	(003D ₁₆)...	00 ₁₆
(23) Serial I/O automatic transfer	(001C ₁₆)...	00 ₁₆	(49) Interrupt control register 1	(003E ₁₆)...	00 ₁₆
interval register			(50) Interrupt control register 2	(003F ₁₆)...	00 ₁₆
(24) Serial I/O2 control register	(001D ₁₆)...	00 ₁₆	(51) Processor status register	(PS)...	X X X X X 1 X X
(25) Serial I/O3 control register	(001E ₁₆)...	00 ₁₆	(52) Program counter	(PC _H)...	Contents of address FFFD ₁₆
(26) Timer 1	(0020 ₁₆)...	FF ₁₆		(PC _L)...	Contents of address FFFC ₁₆
(27) Timer 2	(0021 ₁₆)...	01 ₁₆			
(28) Timer 3	(0022 ₁₆)...	FF ₁₆			
(29) Timer 4	(0023 ₁₆)...	FF ₁₆			
(30) Timer 5	(0024 ₁₆)...	FF ₁₆			

Note : X : Undefined
The contents of all other registers and RAM are undefined at reset, so set their initial values.

Fig. 46 Internal status at reset

CLOCK GENERATING CIRCUIT

The 3819 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between X_{IN} and X_{OUT} (X_{CIN} and X_{COUT}). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between X_{IN} and X_{OUT} since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between X_{CIN} and X_{COUT} .

Immediately after poweron, only the X_{IN} oscillation circuit starts oscillation, and X_{CIN} and X_{COUT} pins function as I/O ports.

Frequency Control

Middle-speed mode

The internal clock ϕ is the frequency of X_{IN} divided by 8. After reset, this mode is selected.

High-speed mode

The internal clock ϕ is half the frequency of X_{IN} .

Low-speed mode

The internal clock ϕ is half the frequency of X_{CIN} .

Note : If you switch the mode between middle/high-speed and low-speed, stabilize both X_{IN} and X_{CIN} oscillations. The sufficient time is required for the X_{CIN} oscillation to stabilize, especially immediately after poweron and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that $f(X_{IN}) > 3 \cdot f(X_{CIN})$.

Low-power dissipation mode

When stopping the main clock X_{IN} in the low-speed mode, the low-power dissipation operation starts. To stop the main clock, set the bit 5 of the CPU mode register to "1". When the main clock X_{IN} is restarted, set enough time for oscillation to stabilize by programming.

The low-power dissipation operation 200 μ A or less (at $f(X_{IN}) = 32$ kHz) can be realized by reducing the X_{CIN} – X_{COUT} drivability. To reduce the X_{CIN} – X_{COUT} drivability, clear the bit 3 of the CPU mode register to "0". At reset or when executing the STP instruction, this bit is set to "1" and strong drivability is selected to help the oscillation to start.

Oscillation Control

Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and X_{IN} and X_{CIN} oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116". Either X_{IN} or X_{CIN} divided by 16 is input to timer 1, and the output of timer 1 is connected to timer 2. The bits of the timer 12 mode register are cleared to "0". Set the timer 1 and timer 2 interrupt enable bits to disabled ("0") before executing the STP instruction.

Oscillator restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 1 underflows. When using an external resonator, it is necessary for oscillating to stabilize.

Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level. The states of X_{IN} and X_{CIN} are the same as the state before executing the WIT instruction. The internal clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

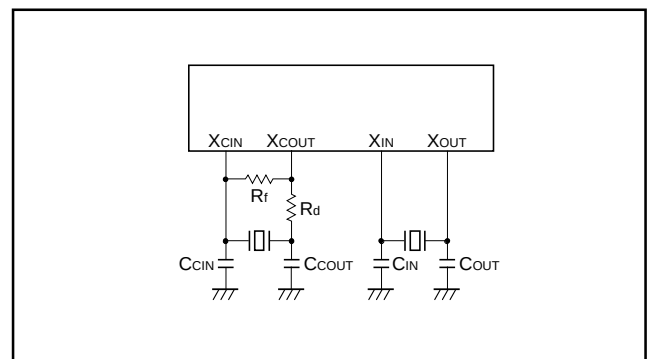


Fig. 47 Ceramic resonator external circuit

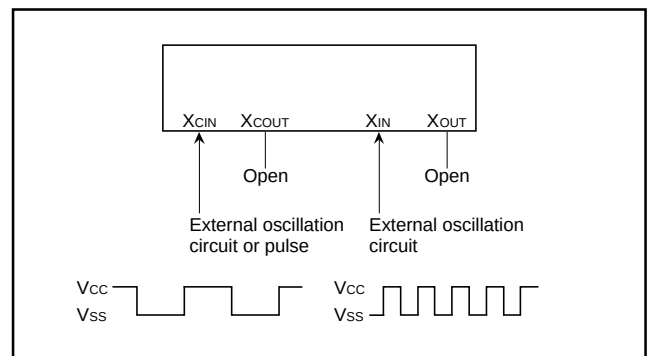


Fig. 48 External clock input circuit

Fig. 49 Clock generating circuit block diagram

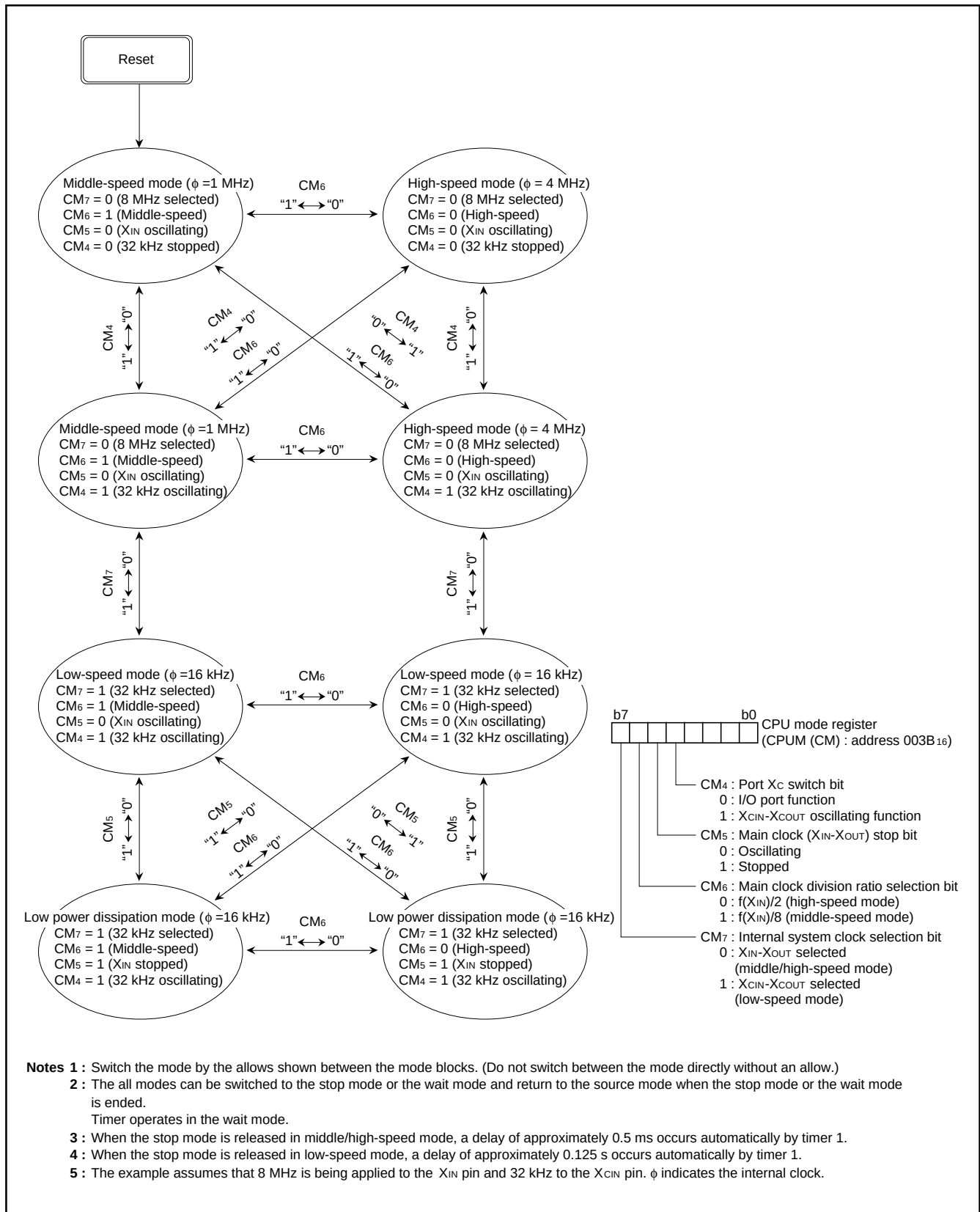


Fig. 50 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flag are invalid.

The carry flag can be used to indicate whether a carry or borrow has occurred. Initialize the carry flag before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- the data transfer instruction (LDA, etc.)
- the operation instruction when the index X mode flag (T) is "1"
- the addressing mode which uses the value of a direction register as an index
- the bit-test instruction (BBC or BBS, etc.) to a direction register
- the read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing serial I/O transfer and serial I/O automatic transfer.

When using the internal clock, set the synchronous clock to internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer and serial I/O automatic transfer.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Make sure that $f(X_{IN})$ is 500 kHz or more during an A-D conversion.

Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions. The frequency of the internal clock ϕ is half of the X_{IN} or X_{CIN} frequency.

At the STP Instruction Release

At the STP instruction release, all bits of the timer 12 mode register are cleared.

The X_{COUT} drivability selection bit (the CPU mode register) is set to "1" (high drive) in order to start oscillating.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- (1) Mask ROM Order Confirmation Form
- (2) Mask Specification Form
- (3) Data to be written to ROM, in EPROM form (three identical copies)

PROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Package	Name of Programming Adapter
100P6S-A	PCA4738F-100A
100D0	PCA4738L-100A

Set the address of PROM programmer in the user ROM area. The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after writing, the procedure shown in Figure 51 is recommended to verify programming.

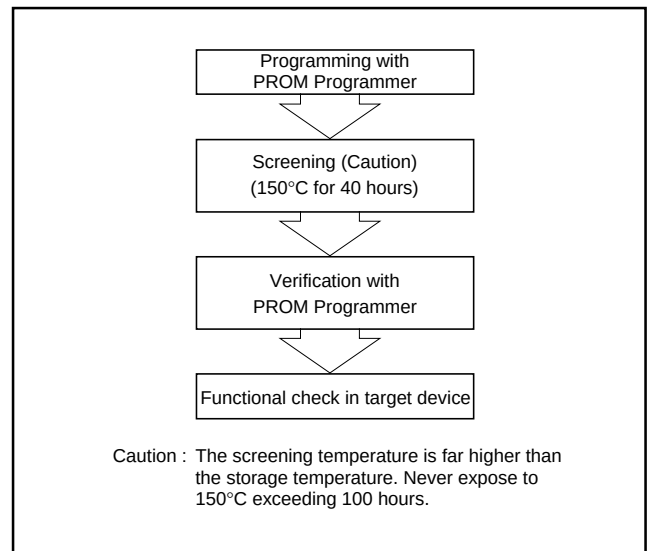


Fig. 51 Programming and testing of One Time PROM version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Power source voltage	All voltages are based on VSS. Output transistors are cut off.	−0.3 to 7.0	V
VEE	Pull-down power source voltage		VCC−40 to VCC+0.3	V
VI	Input voltage P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3		−0.3 to VCC+0.3	V
VI	Input voltage P40, P45		−0.3 to VCC+0.3	V
VI	Input voltage P80–P87, PA0–PA7		VCC−40 to VCC+0.3	V
VI	Input voltage RESET, XIN		−0.3 to VCC+0.3	V
VI	Input voltage XCIN		−0.3 to VCC+0.3	V
VO	Output voltage P00–P07, P10–P17, P20–P23, P30–P37, P80–P87, P90–P97, PA0–PA7		VCC−40 to VCC+0.3	V
VO	Output voltage P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3, XOUT, XCOUT		−0.3 to VCC+0.3	V
Pd	Power dissipation	Ta = 25°C	600	mW
Topr	Operating temperature		−10 to 85	°C
Tstg	Storage temperature		−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (VCC = 4.0 to 5.5 V, Ta = −10 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
VCC	Power source voltage	High-speed mode	4.0	5.0	5.5	V
		Middle/Low-speed mode	2.8	5.0	5.5	V
VSS	Power source voltage			0		V
VEE	Pull-down power source voltage		VCC−38		VCC	V
VREF	Analog reference voltage (when using A-D converter)		2.0		VCC	V
	Analog reference voltage (when using D-A converter)		3.0		VCC	V
AVSS	Analog power source voltage			0		V
VIA	Analog input voltage AN0–AN15		0		VCC	V
VIH	"H" input voltage	P40–P47, P50–P57, P60–P67, P70–P77, PB0–PB3	0.75VCC		VCC	V
VIH	"H" input voltage	P24–P27	0.4VCC		VCC	V
VIH	"H" input voltage	P80–P87, PA0–PA7	0.8VCC		VCC	V
VIH	"H" input voltage	RESET	0.8VCC		VCC	V
VIH	"H" input voltage	XIN, XCIN	0.8VCC		VCC	V
VIL	"L" input voltage	P40–P47, P50–P57, P60–P67, P70–P77, PB0–PB3	0		0.25VCC	V
VIL	"L" input voltage	P24–P27	0		0.16VCC	V
VIL	"L" input voltage	P80–P87, PA0–PA7	0		0.2VCC	V
VIL	"L" input voltage	RESET	0		0.2VCC	V
VIL	"L" input voltage	XIN, XCIN	0		0.2VCC	V

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.0 to 5.5 V, T_a = –10 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	“H” total peak output current (Note 1) P00–P07, P10–P17, P20–P27, P30–P37, P80–P87, P90–P97, PA6, PA7			–240	mA
	“H” total peak output current (Note 1) P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PA0–PA5, PB0–PB3			–60	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current (Note 1) P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3			100	mA
$\Sigma I_{OH(avg)}$	“H” total average output current (Note 1) P00–P07, P10–P17, P20–P27, P30–P37, P80–P87, P90–P97, PA6, PA7			–120	mA
	“H” total average output current (Note 1) P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PA0–PA5, PB0–PB3			–30	mA
$\Sigma I_{OL(avg)}$	“L” total average output current (Note 1) P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3			50	mA
$I_{OH(peak)}$	“H” peak output current (Note 2) P00–P07, P10–P17, P20–P23, P30–P37, P80–P87, P90–P97, PA0–PA7			–40	mA
$I_{OH(peak)}$	“H” peak output current (Note 2) P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3			–10	mA
$I_{OL(peak)}$	“L” peak output current (Note 3) P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3			10	mA
$I_{OH(avg)}$	“H” average output current (Note 3) P00–P07, P10–P17, P20–P23, P30–P37, P80–P87, P90–P97, PA0–PA7			–18	mA
$I_{OH(avg)}$	“H” average output current (Note 3) P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3			–5.0	mA
$I_{OL(avg)}$	“L” average output current (Note 3) P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3			5.0	mA
f(CNTR0) f(CNTR1)	Clock input frequency for timers 2 and 4 (duty cycle 50%)			250	kHz
f(XIN)	Main clock input oscillation frequency (Note 4)			8.4	MHz
f(XCIN)	Sub-clock input oscillation frequency (Note 4, 5)		32.768	50	kHz

Notes 1 : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2 : The peak output current is the peak current flowing in each port.

3 : The average output current is an average value measured over 100 ms.

4 : When the oscillation frequency has a 50% duty cycle.

5 : When using the microcomputer in low-speed operation mode, set the sub-clock input oscillation frequency on condition that $f(XCIN) < f(XIN)/3$.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -10$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage P00–P07, P10–P17, P20–P23, P30–P37, P80–P87, P90–P97, PA0–PA7	$I_{OH} = -18$ mA	$V_{CC} - 2.0$			V
V_{OH}	"H" output voltage P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3	$I_{OH} = -10$ mA	$V_{CC} - 2.0$			V
V_{OL}	"L" output voltage P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3	$I_{OL} = 10$ mA			2.0	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{INT0} - \overline{INT4}$, SIN1, SIN2, SIN3, SCLK11, SCLK2, SCLK3, CS, CNTR0, CNTR1	When using a non-port function		0.4		V
$V_{T+} - V_{T-}$	Hysteresis RESET, XIN			0.5		V
$V_{T+} - V_{T-}$	Hysteresis XCIN			0.5		V
I_H	"H" input current P24–P27, P40–P47, P50–P57, P60–P67, P70–P77, PB0–PB3	$V_i = V_{CC}$			5.0	μA
I_H	"H" input current P80–P87, PA0–PA7 (Note)	$V_i = V_{CC}$			5.0	μA
I_H	"H" input current RESET, XCIN	$V_i = V_{CC}$			5.0	μA
I_H	"H" input current XIN	$V_i = V_{CC}$		4.0		μA
I_L	"L" input current P24–P27, P40–P47, P50–P57, P60–P67, P70–P77, PB0–PB3	$V_i = V_{SS}$			-5.0	μA
I_L	"L" input current P80–P87, PA0–PA7 (Note)	$V_i = V_{SS}$			-5.0	μA
I_L	"L" input current RESET, XCIN	$V_i = V_{SS}$			-5.0	μA
I_L	"L" input current XIN	$V_i = V_{SS}$		-4.0		μA
I_{LOAD}	Output load current P00–P07, P10–P17, P20–P23, P30–P37, P90–P97	$V_{EE} = V_{CC} - 36$ V, $V_{OL} = V_{CC}$, Output transistors "off"	150	500	900	μA
I_{LEAK}	Output leakage current P00–P07, P10–P17, P20–P23, P30–P37, P80–P87, P90–P97, PA0–PA7	$V_{EE} = V_{CC} - 38$ V, $V_{OL} = V_{CC} - 38$ V, Output transistors "off"			-10	μA
VRAM	RAM hold voltage	When clock is stopped	2		5.5	V

Note : Except when reading ports P8 or PA.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -10$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{CC}	Power source current	- High-speed mode - f(X_{IN}) = 8.4 MHz - f(X_{CIN}) = 32 kHz - Output transistors "off"		7.5	15	mA
		- High-speed mode - f(X_{IN}) = 8.4 MHz (in WIT state) - f(X_{CIN}) = 32 kHz - Output transistors "off"		1		mA
		- Middle-speed mode - f(X_{IN}) = 8.4 MHz - f(X_{CIN}) = stopped - Output transistors "off"		3		mA
		- Middle-speed mode - f(X_{IN}) = 8.4 MHz (in WIT state) - f(X_{CIN}) = stopped - Output transistors "off"		1		mA
		- Low-speed mode - f(X_{IN}) = stopped, f(X_{CIN}) = 32 kHz - Low-power dissipation mode set (CM₃) = 0 - Output transistors "off"		60	200	μA
		- Low-speed mode - f(X_{IN}) = stopped - f(X_{CIN}) = 32 kHz (in WIT state) - Low-power dissipation mode set (CM₃) = 0 - Output transistors "off"		20	40	μA
		Increase at A-D converter operating f(X _{IN}) = 8.4 MHz		0.6		mA
		Increase at zero cross detection (P ₄₅ = V _{CC})		1		mA
		All oscillation stopped (in STP state)	T _a = 25°C	0.1	1	μA
		Output transistors "off"	T _a = 85°C		10	

ZERO CROSS DETECTION INPUT CHARACTERISTICS

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = -10 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
f _{ZCR}	Input frequency of zero cross detection			50, 60	1000	Hz
ΔV _T	Voltage error of zero cross detection distinction	50 Hz or 60 Hz	-100	0	100	mV

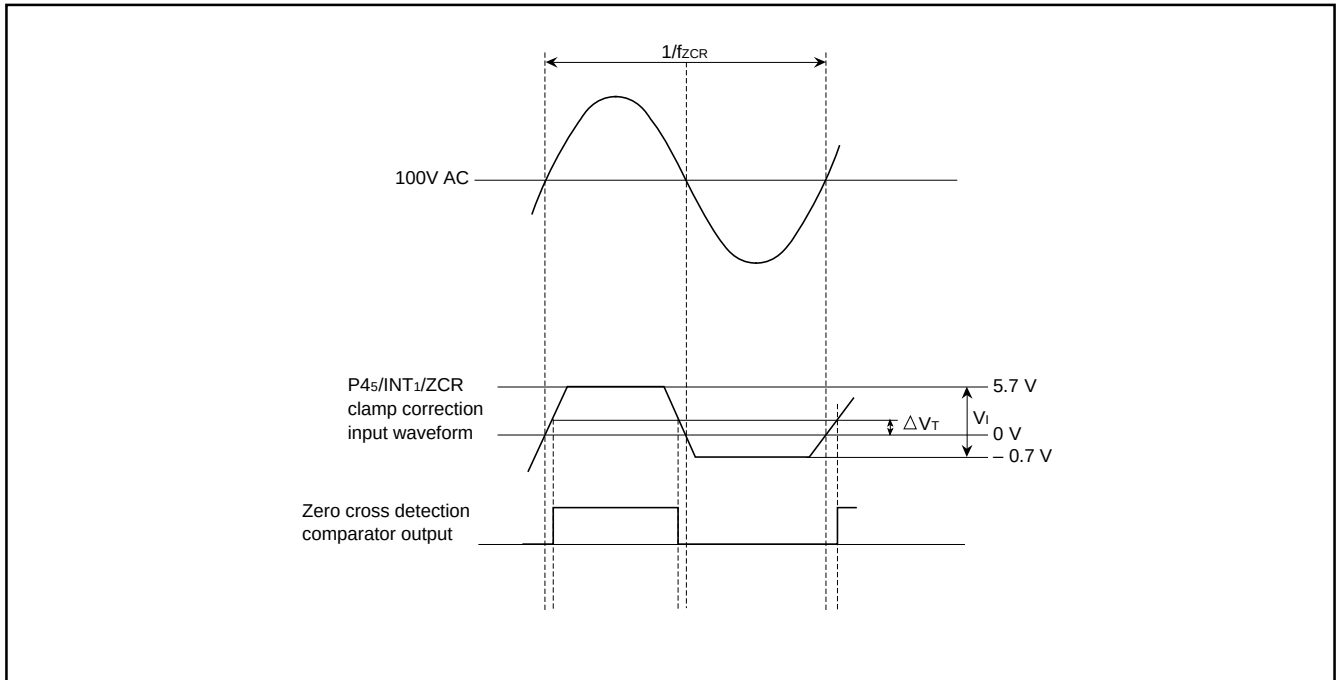


Fig. 52 Zero cross detection input characteristics

A-D CONVERTER CHARACTERISTICS

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = -10 to 85°C, high-speed operation mode f(X_{IN}) = 500 kHz to 8.4 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)	V _{CC} = V _{REF} = 5.12 V		±1	±2.5	LSB
T _{CONV}	Conversion time		49		50	tc (φ)
I _{VREF}	Reference power source input current	V _{REF} = 5 V	50	150	200	μA
I _{IA}	Analog port input current			0.5	5.0	μA
RLADDER	Ladder resistor			35		kΩ

D-A CONVERTER CHARACTERISTICS

(V_{CC} = 4.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{REF} = 3.0 to V_{CC}, T_a = -10 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy	V _{CC} = 4.0 to 5.5 V			1.0	%
		V _{CC} = 3.0 to 5.5 V			2.5	%
T _{SU}	Setting time				3	μs
R _O	Output resistor		1	2.5	4	kΩ
I _{VREF}	Reference power source input current (Note)				3.2	mA

Note : Exclude currents flowing through the A-D converter ladder resistor

TIMING REQUIREMENTS ($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -10$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\text{RESET})$	Reset input "L" pulse width	2.0			μs
$t_c(X_{IN})$	Main clock input cycle time (X_{IN} input)	119			ns
$t_{WH}(X_{IN})$	Main clock input "H" pulse width	30			ns
$t_{WL}(X_{IN})$	Main clock input "L" pulse width	30			ns
$t_c(X_{CIN})$	Sub-clock input cycle time (X_{CIN} input)	20			μs
$t_{WH}(X_{CIN})$	Sub-clock input "H" pulse width	5.0			μs
$t_{WL}(X_{CIN})$	Sub-clock input "L" pulse width	5.0			μs
$t_c(\text{CNTR})$	CNTR0, CNTR1 input cycle time	4.0			μs
$t_{WH}(\text{CNTR})$	CNTR0, CNTR1 input "H" pulse width	1.6			μs
$t_{WL}(\text{CNTR})$	CNTR0, CNTR1 input "L" pulse width	1.6			μs
$t_{WH}(\text{INT})$	INT0–INT4 input "H" pulse width	80			ns
$t_{WL}(\text{INT})$	INT0–INT4 input "L" pulse width	80			ns
$t_c(\text{SCLK})$	Serial I/O clock input cycle time	1.0			μs
$t_{WH}(\text{SCLK})$	Serial I/O clock input "H" pulse width	400			ns
$t_{WL}(\text{SCLK})$	Serial I/O clock input "L" pulse width	400			ns
$t_{su}(\text{SCLK} \rightarrow \text{SIN})$	Serial I/O input setup time	200			ns
$t_h(\text{SCLK} \rightarrow \text{SIN})$	Serial I/O input hold time	200			ns

SWITCHING CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -10$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH}(\text{SCLK})$	Serial I/O clock output "H" pulse width	$C_L = 100$ pF	$t_c(\text{SCLK}) / 2 \sim 160$			ns
$t_{WL}(\text{SCLK})$	Serial I/O clock output "L" pulse width	$C_L = 100$ pF	$t_c(\text{SCLK}) / 2 \sim 160$			ns
$t_d(\text{SCLK} \rightarrow \text{SOUT})$	Serial I/O output delay time				$0.2t_c(\text{SCLK})$	ns
$t_v(\text{SCLK} \rightarrow \text{SOUT})$	Serial I/O output hold time		0			ns
$t_r(\text{SCLK})$	Serial I/O clock output rising time	$C_L = 100$ pF			40	ns
$t_f(\text{SCLK})$	Serial I/O clock output falling time	$C_L = 100$ pF			40	ns
$t_r(\text{Pch-strg})$	High-breakdown-voltage P-channel open-drain output rising time (Note 1)	$C_L = 100$ pF $V_{EE} = V_{CC} - 36$ V		55		ns
$t_f(\text{Pch-weak})$	High-breakdown-voltage P-channel open-drain output falling time (Note 2)	$C_L = 100$ pF $V_{EE} = V_{CC} - 36$ V		1.8		μs

Notes 1: When the bit 7 of the FLDC mode register 1 (address 003616) is at "0".

2: When the bit 7 of the FLDC mode register 1 (address 003616) is at "1".

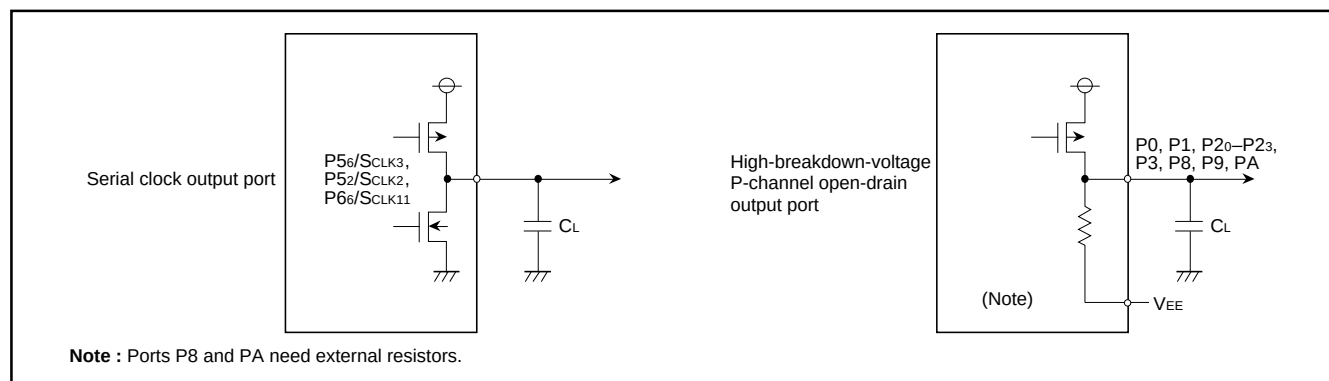
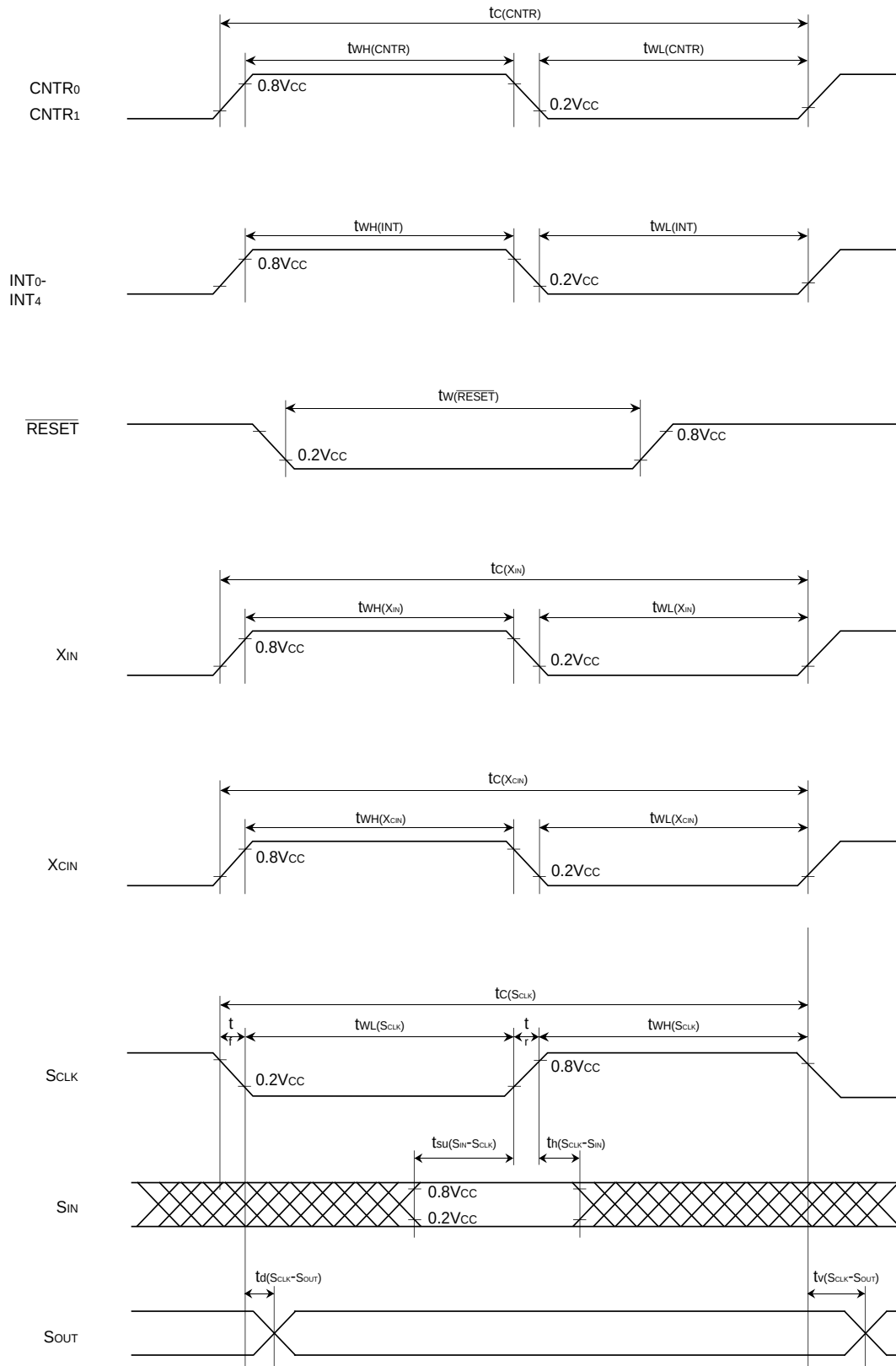


Fig. 53 Circuit for measuring output switching characteristics

TIMING DIAGRAM



Power source current characteristic examples

Figures 54 and 55 show power source current characteristic examples.

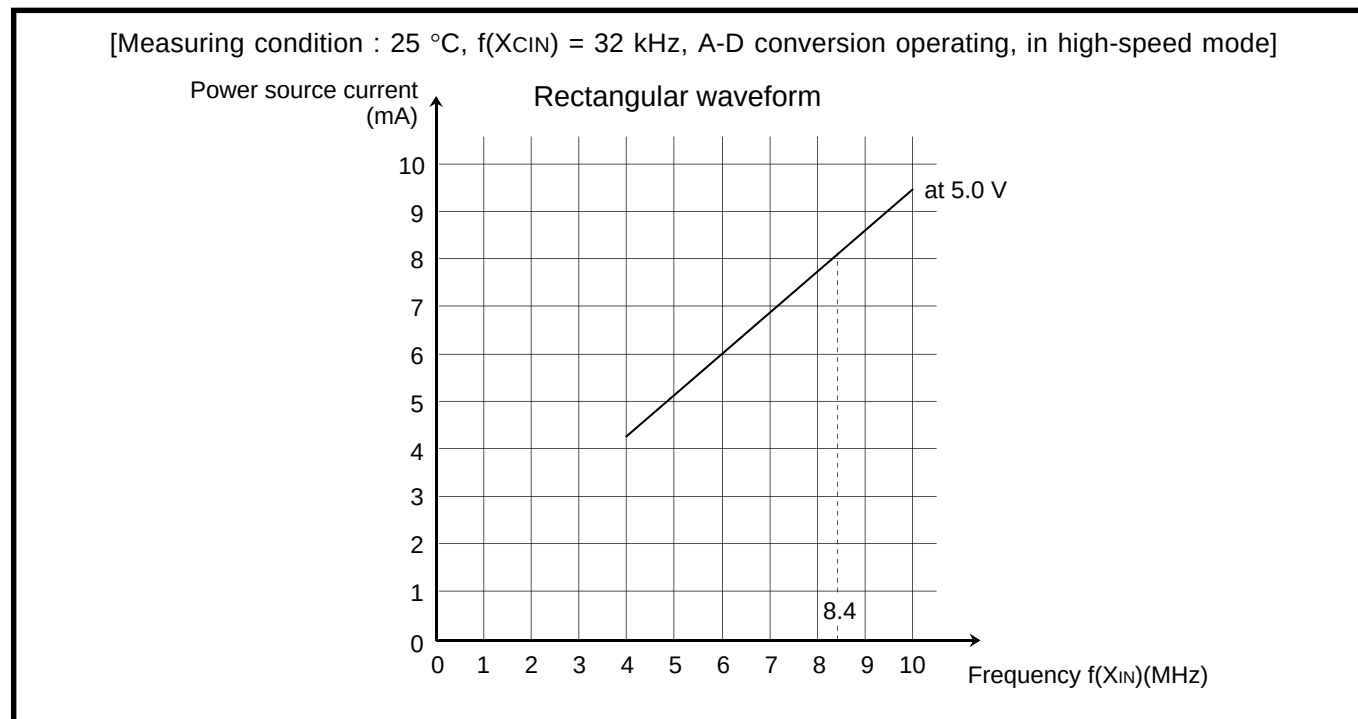


Fig. 54 Power source current characteristic example

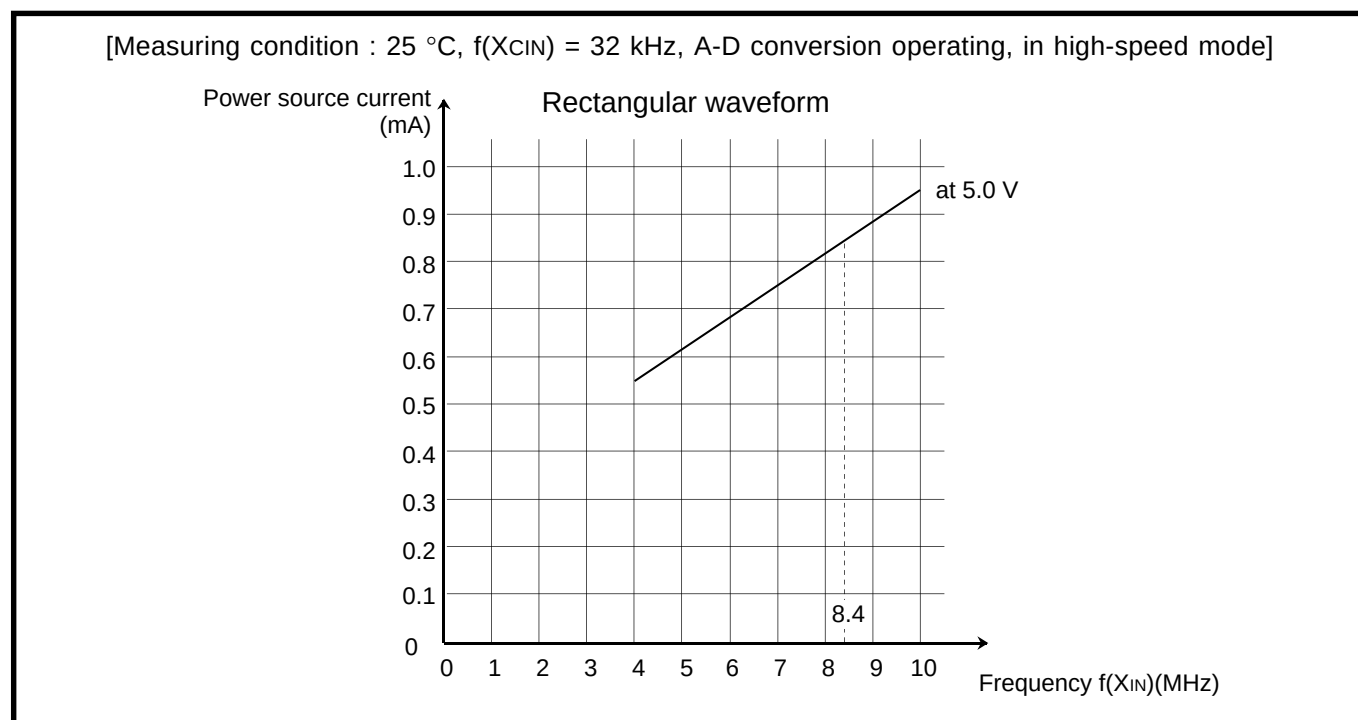


Fig. 55 Power source current characteristic example (in wait mode)

Port standard characteristic examples

Figures 56, 57, and 58 show port standard characteristic examples.

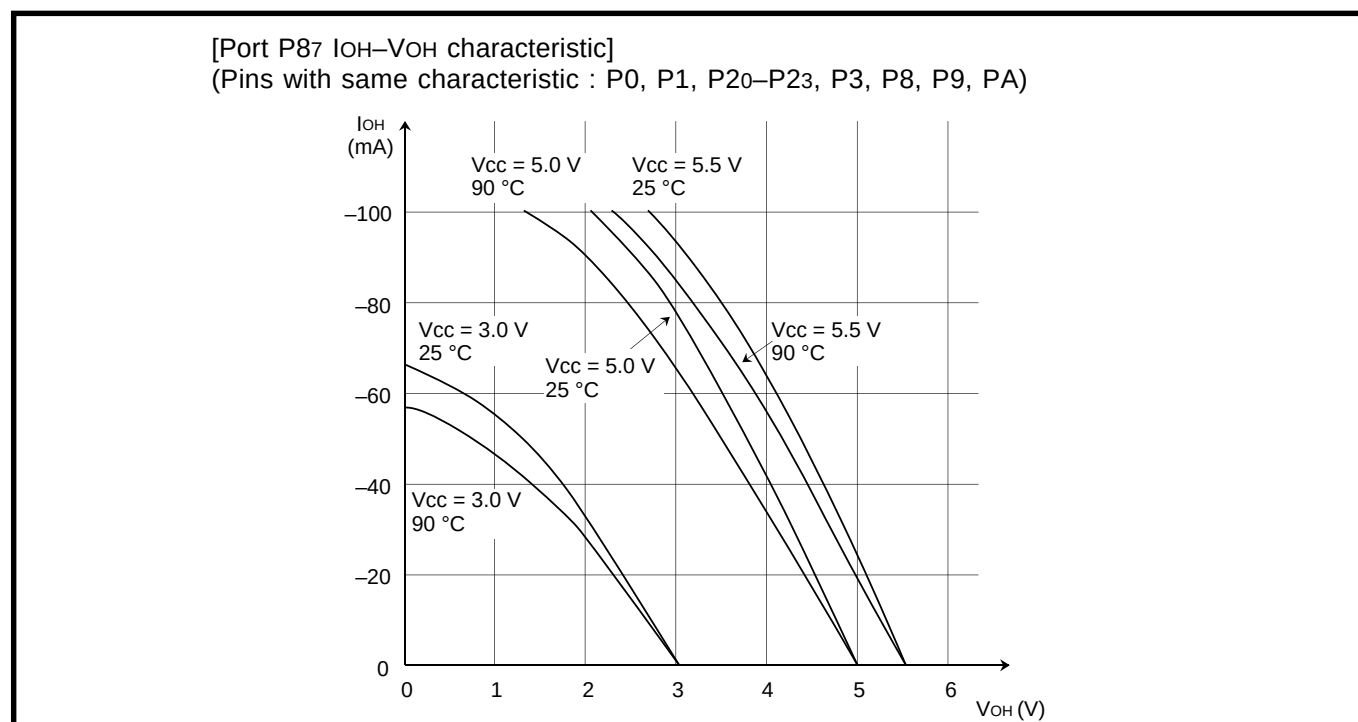


Fig. 56 Standard characteristic example of High-breakdown-voltage P-channel open-drain output port

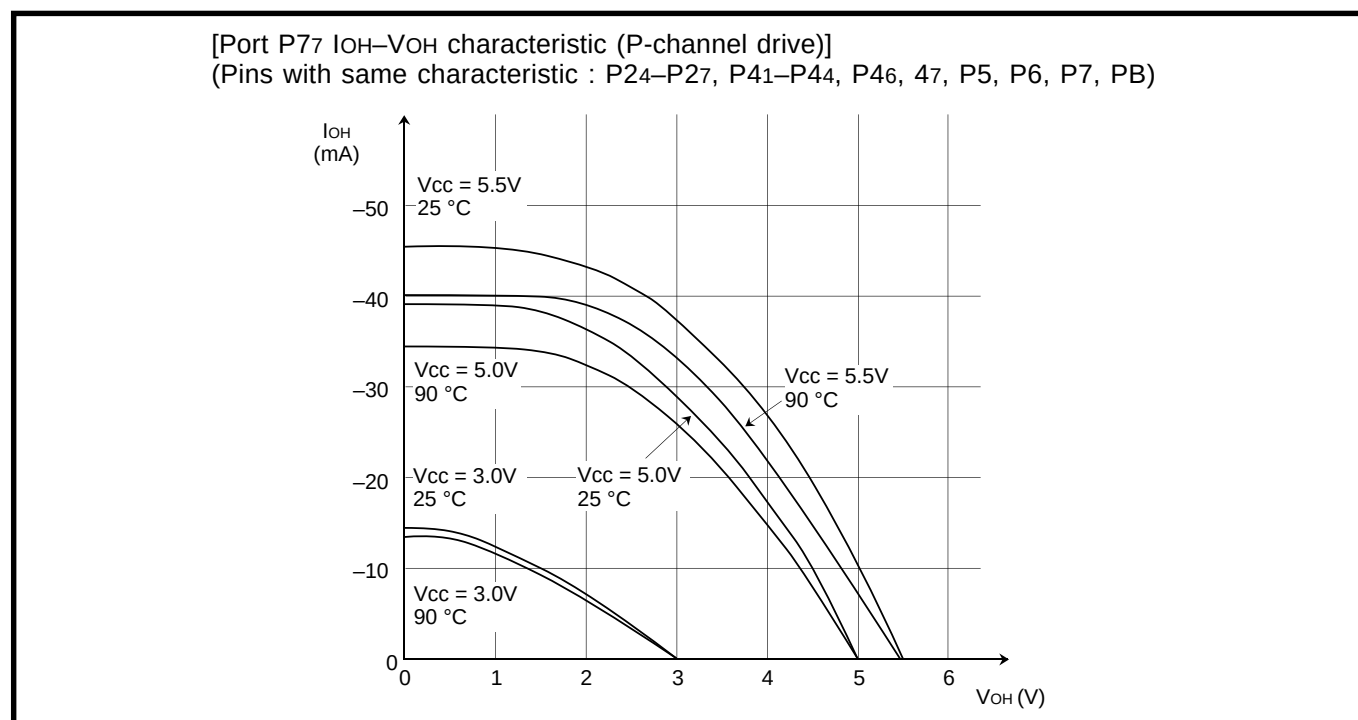


Fig. 57 Standard characteristic example of CMOS output port at P-channel drive

[Port P77 I_{OL} - V_{OL} characteristic (N-channel drive)]
 (Pins with same characteristic : P24-P27, P41-P44, P46, 47, P5, P6, P7, PB)

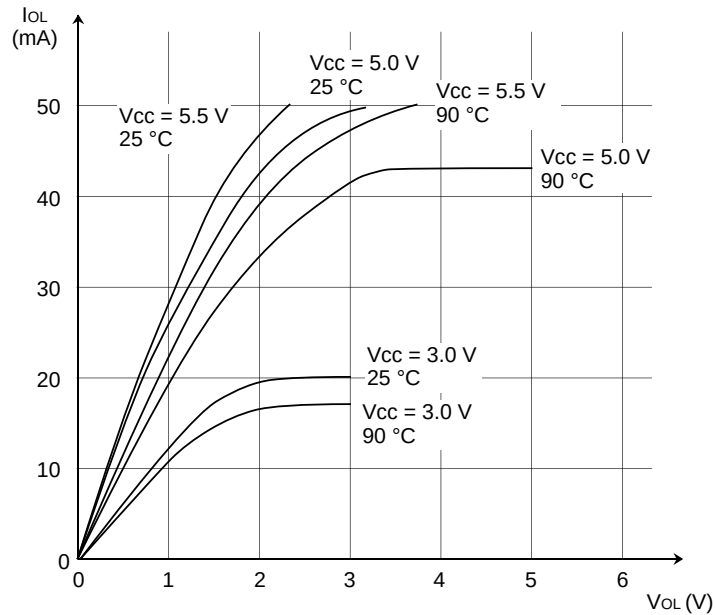


Fig. 58 Standard characteristic example of CMOS output port at N-channel drive

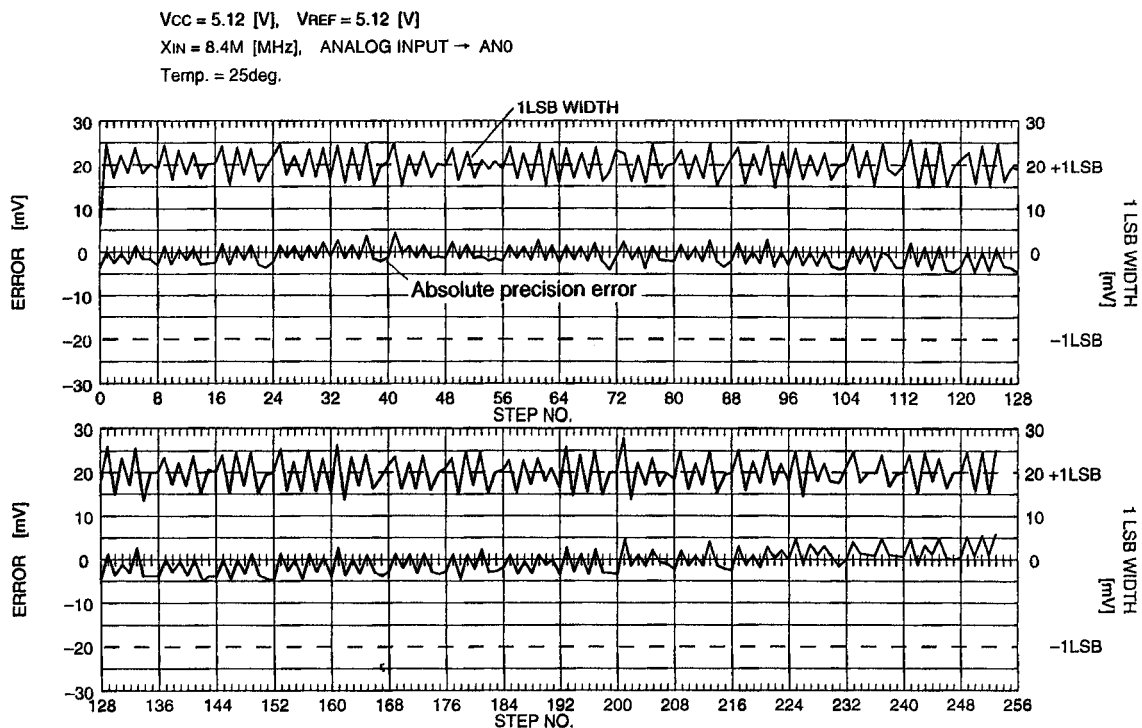
A-D conversion standard characteristics

Figure 59 shows the A-D conversion standard characteristics.

The lower-side line on the graph indicates the absolute precision error. It represents the deviation from the ideal value. For example, the conversion of output code from 00₁₆ to 01₁₆ occurs ideally at the point of AN₀ = 10 mV, but the measured value is -4 mV. Accordingly, the measured point of conversion is represented as "10 - 4 = 6 mV".

The upper-side line on the graph indicates the width of input voltages equivalent to output codes. For example, the measured width of the input voltage for output code 49₁₆ is 23 mV, so the differential nonlinear error is represented as "23 - 20 = 3 mV" (0.1 LSB).

M38197MA-000FP A-D CONVERTER STEP WIDTH MEASUREMENT



Measured when a power source voltage is stable in the high-speed mode

Fig. 59 A-D conversion standard characteristics

D-A conversion standard characteristics

Figure 60 shows the D-A conversion standard characteristics. The lower-side line on the graph indicates the absolute precision error. In this case, it represents the difference between the ideal analog output value for an input code and the measured value.

The upper-side line on the graph indicates the change width of output analog value to a one-bit change of input code.

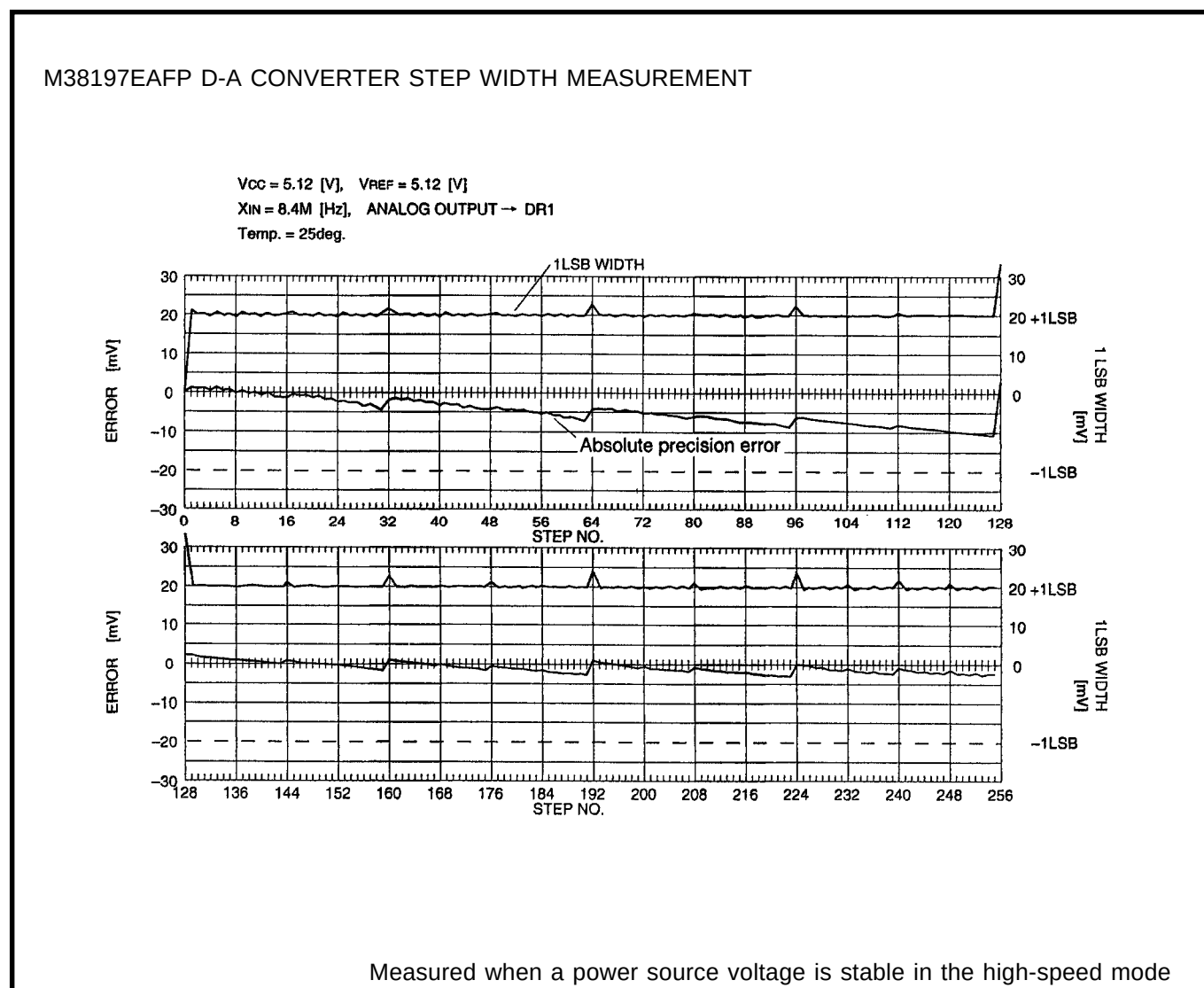


Fig. 60 D-A conversion standard characteristics

Functional description supplement

Interrupt

3819 group permits interrupts on the basis of 20 sources. It is vector interrupts with a fixed priority system. Accordingly, when two or more interrupt requests occur during the same sampling, the higher-priority interrupt is accepted first. This priority is determined by hardware, but variety of priority processing can be performed by software, using an interrupt enable bit and an interrupt disable flag.

For interrupt sources, vector addresses and interrupt priority, refer to “Table 5.”

Table 5. Interrupt sources, vector addresses and interrupt priority

Priority	Interrupt sources	Vector addresses		Remarks
		High-order	Low-order	
1	Reset (Note)	FFFD ₁₆	FFFC ₁₆	Non-maskable
2	INT0 interrupt	FFFB ₁₆	FFFA ₁₆	External interrupt (active edge selectable)
3	INT1/ZCR interrupt	FFF9 ₁₆	FFF8 ₁₆	External interrupt (active edge selectable)
4	INT2 interrupt	FFF7 ₁₆	FFF6 ₁₆	External interrupt (active edge selectable)
	Remote control/counter overflow interrupt			Valid when interrupt interval determination operates
5	Serial I/O 1 interrupt	FFF5 ₁₆	FFF4 ₁₆	Valid when serial I/O ordinary mode is selected
	Serial I/O 1 automatic transfer interrupt			Valid when serial I/O automatic transfer mode is selected
6	Serial I/O 2 interrupt	FFF3 ₁₆	FFF2 ₁₆	Valid when serial I/O 2 is selected
7	Serial I/O 3 interrupt	FFF1 ₁₆	FFF0 ₁₆	Valid when serial I/O 3 is selected
8	Timer 1 interrupt	FFEF ₁₆	FFEE ₁₆	STP release timer underflow
9	Timer 2 interrupt	FFED ₁₆	FFEC ₁₆	
10	Timer 3 interrupt	FFEB ₁₆	FFEA ₁₆	
11	Timer 4 interrupt	FFE9 ₁₆	FFE8 ₁₆	
12	Timer 5 interrupt	FFE7 ₁₆	FFE6 ₁₆	
13	Timer 6 interrupt	FFE5 ₁₆	FFE4 ₁₆	
14	INT3 interrupt	FFE3 ₁₆	FFE2 ₁₆	External interrupt (active edge selectable)
15	INT4 interrupt	FFE1 ₁₆	FFE0 ₁₆	Valid when INT4 interrupt is selected
	A-D conversion interrupt			External interrupt (active edge selectable) Valid when A-D converter interrupt is selected
16	FLD blanking interrupt	FFDF ₁₆	FFDE ₁₆	Valid when FLD blanking interrupt is selected
	FLD digit interrupt			Valid when FLD digit interrupt is selected
17	BRK instruction interrupt	FFDD ₁₆	FFDC ₁₆	Non-maskable software interrupt

Note : Reset functions in the same way as an interrupt with the highest priority.

Timing after interrupt

The interrupt processing routine begins with the machine cycle following the completion of the instruction that is currently in execution.

Figure 61 shows a timing chart after an interrupt occurs, and figure 62 shows the time up to execution of the interrupt processing routine.

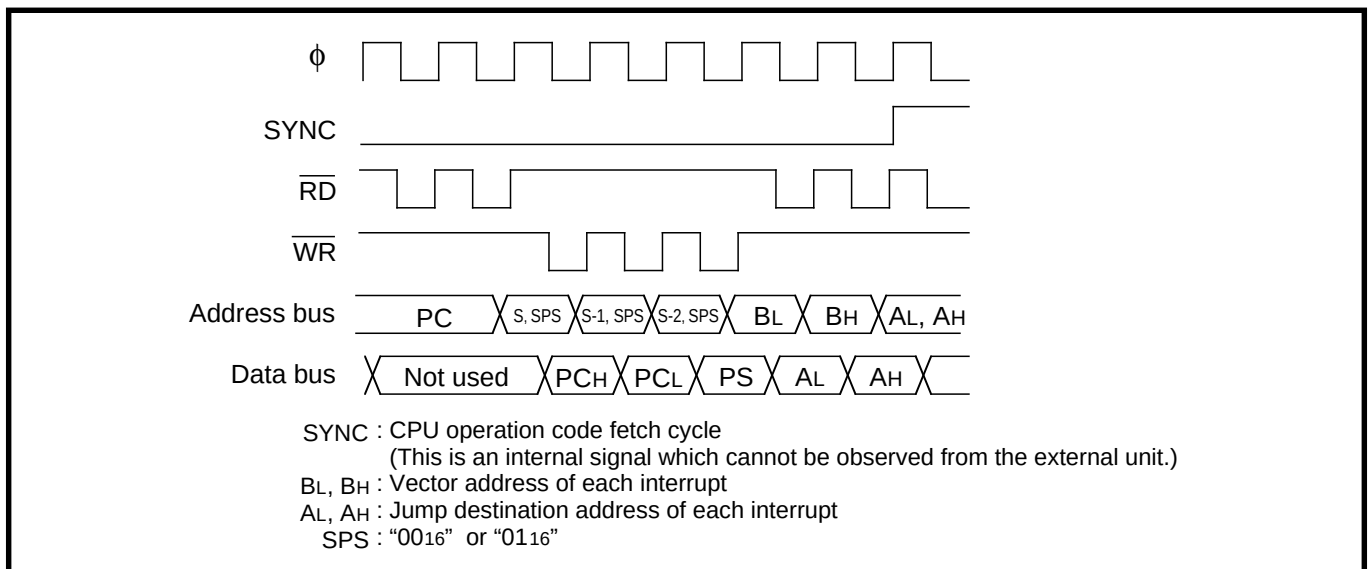


Fig. 61 Timing chart after an interrupt occurs

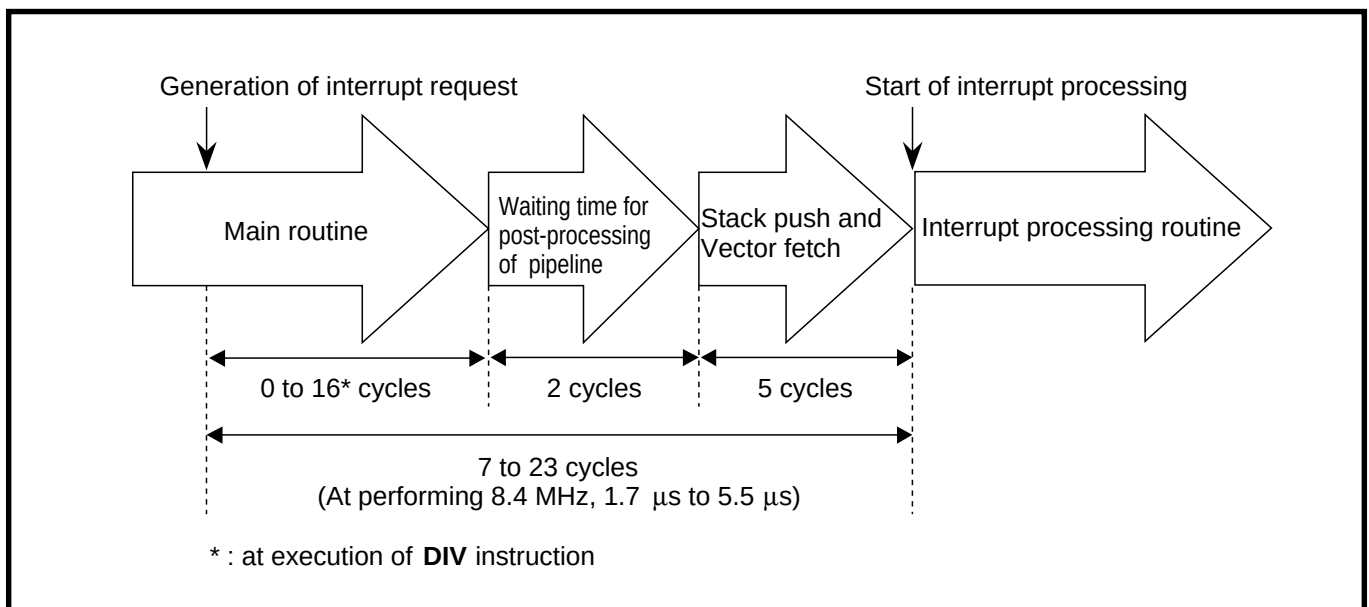


Fig. 62 Time up to execution of the interrupt processing routine

A-D converter

A-D conversion is started by setting A-D conversion completion bit to "0". During A-D conversion, internal operations are performed as follows.

1. After the start of A-D conversion, A-D conversion register goes to "0016."
2. The highest-order bit of A-D conversion register is set to "1", and the comparison voltage Vref is input to the comparator. Then, Vref is compared with analog input voltage VIN.
3. As a result of comparison, when Vref < VIN, the highest-order bit of A-D conversion register becomes "1." When Vref > VIN, the highest-order bit becomes "0."

By repeating the above operations up to the lowest-order bit of the A-D conversion register, an analog value converts into a digital value.

A-D conversion completes at 50 clock cycles (11.9 μs at f(XIN) = 8.4 MHz) after it is started, and the result of the conversion is stored into the A-D conversion register.

Concurrently with the completion of A-D conversion, A-D conversion interrupt request occurs, so that the A-D conversion interrupt request bit is set to "1".

Relative formula for a reference voltage VREF of A-D converter and Vref

$$\begin{aligned} \text{When } n = 0 & \quad V_{\text{ref}} = 0 \\ \text{When } n = 1 \text{ to } 255 & \quad V_{\text{ref}} = \frac{V_{\text{REF}}}{256} \times (n - 0.5) \\ & \quad n : \text{the value of A-D converter (decimal numeral)} \end{aligned}$$

Table 6. Change of A-D conversion register during A-D conversion

	Change of A-D conversion register	Value of comparison voltage (Vref)
At start of conversion	0 0 0 0 0 0 0 0	0
First comparison	1 0 0 0 0 0 0 0	$\frac{V_{\text{REF}}}{2} - \frac{V_{\text{REF}}}{512}$
Second comparison	*1 1 0 0 0 0 0 0	$\frac{V_{\text{REF}}}{2} \pm \frac{V_{\text{REF}}}{4} - \frac{V_{\text{REF}}}{512}$
Third comparison	*1 *2 1 0 0 0 0 0	$\frac{V_{\text{REF}}}{2} \pm \frac{V_{\text{REF}}}{4} \pm \frac{V_{\text{REF}}}{8} - \frac{V_{\text{REF}}}{512}$
After completion of eighth comparison	A result of A-D conversion *1 *2 *3 *4 *5 *6 *7 *8	

*1 : A result of the first comparison

*3 : A result of the third comparison

*5 : A result of the fifth comparison

*7 : A result of the seventh comparison

*2 : A result of the second comparison

*4 : A result of the fourth comparison

*6 : A result of the sixth comparison

*8 : A result of the eighth comparison

Figures 63 shows A-D conversion equivalent circuit, and figure 64 shows A-D conversion timing chart.

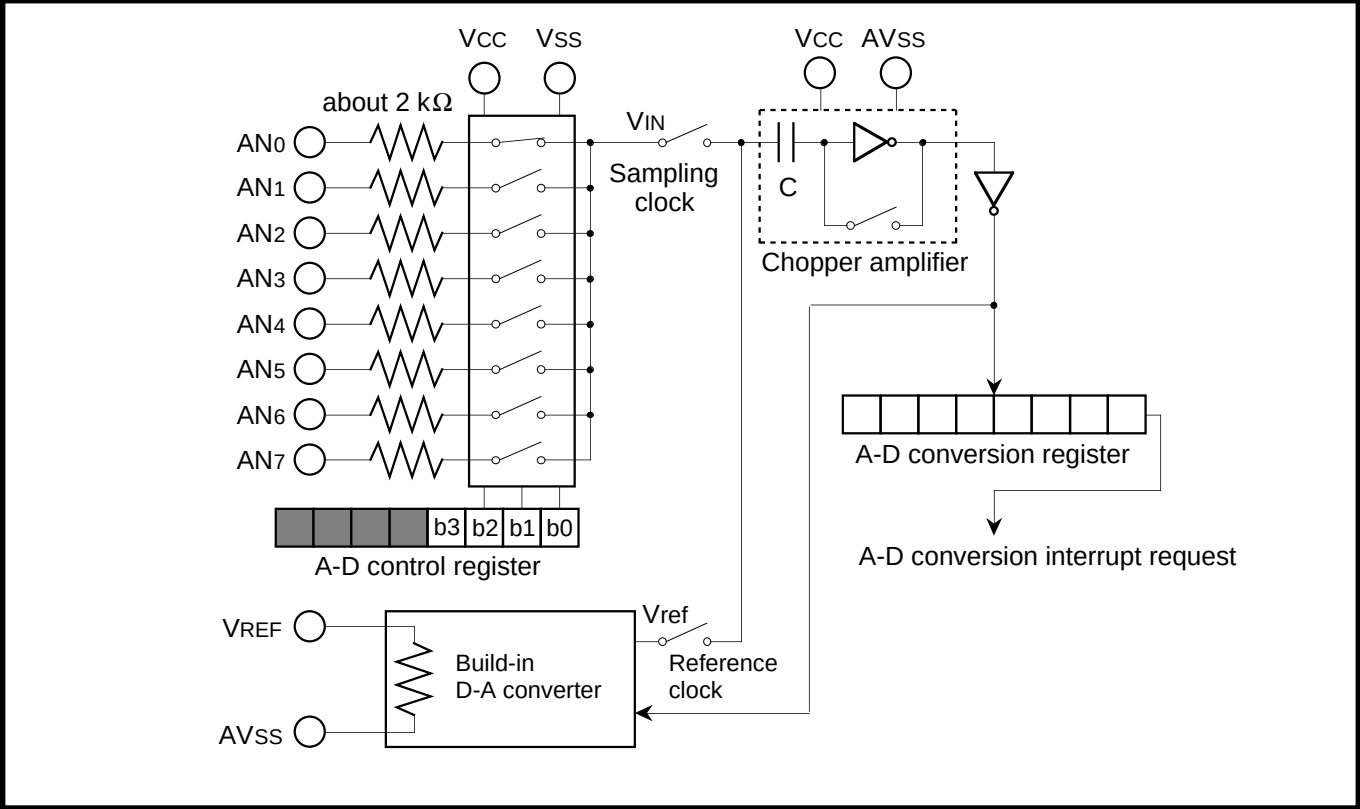


Fig. 63 A-D conversion equivalent circuit

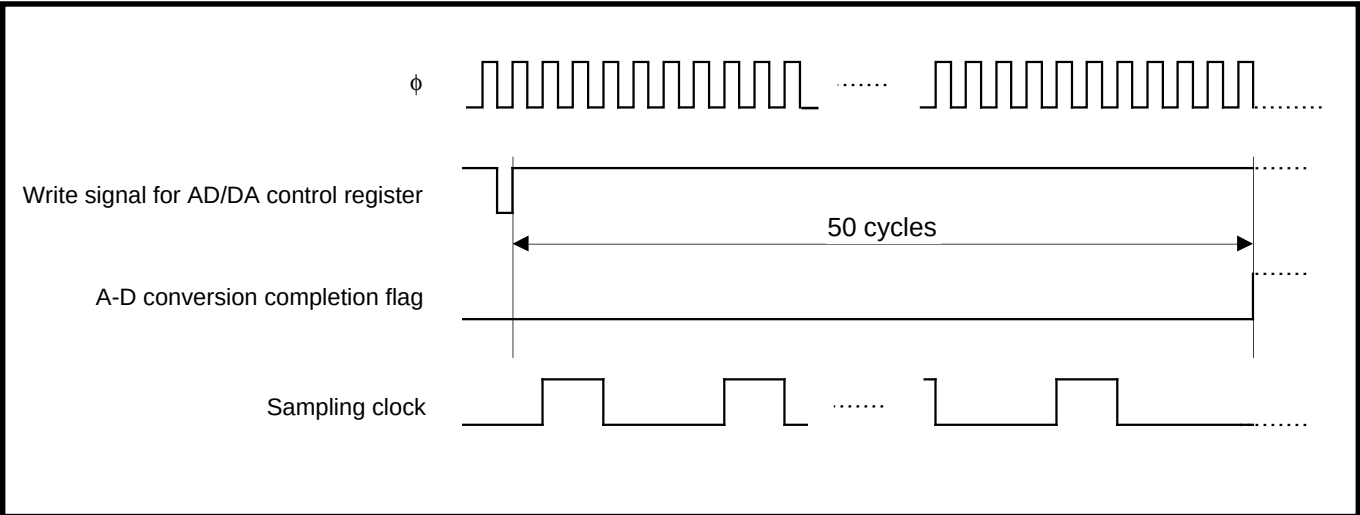
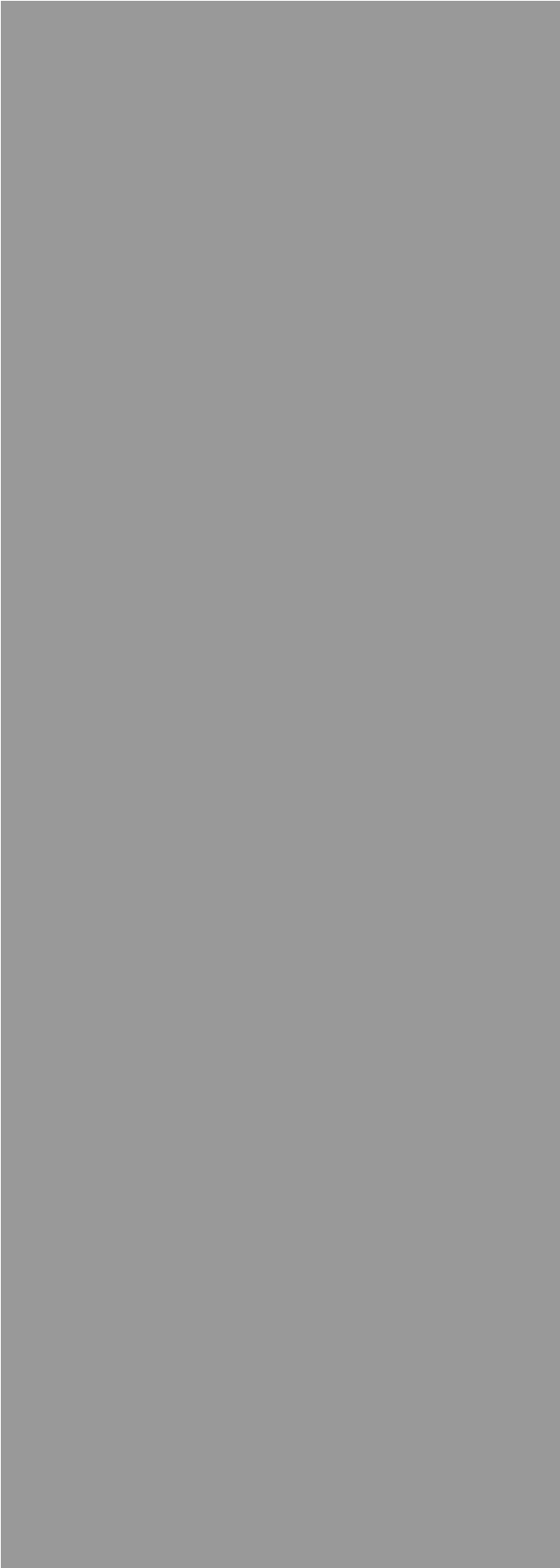


Fig. 64 A-D conversion timing chart



CHAPTER 2

APPLICATION

- 2.1 I/O port
- 2.2 Timer
- 2.3 Serial I/O
- 2.4 A-D conversion
- 2.5 FLD controller
- 2.6 Interrupt interval
determination function
- 2.7 Zero cross detection circuit
- 2.8 Reset
- 2.9 Clock generating circuit

3819 Group

2.1 I/O port

2. APPLICATION

2.1 I/O Port

2.1.1 Related registers

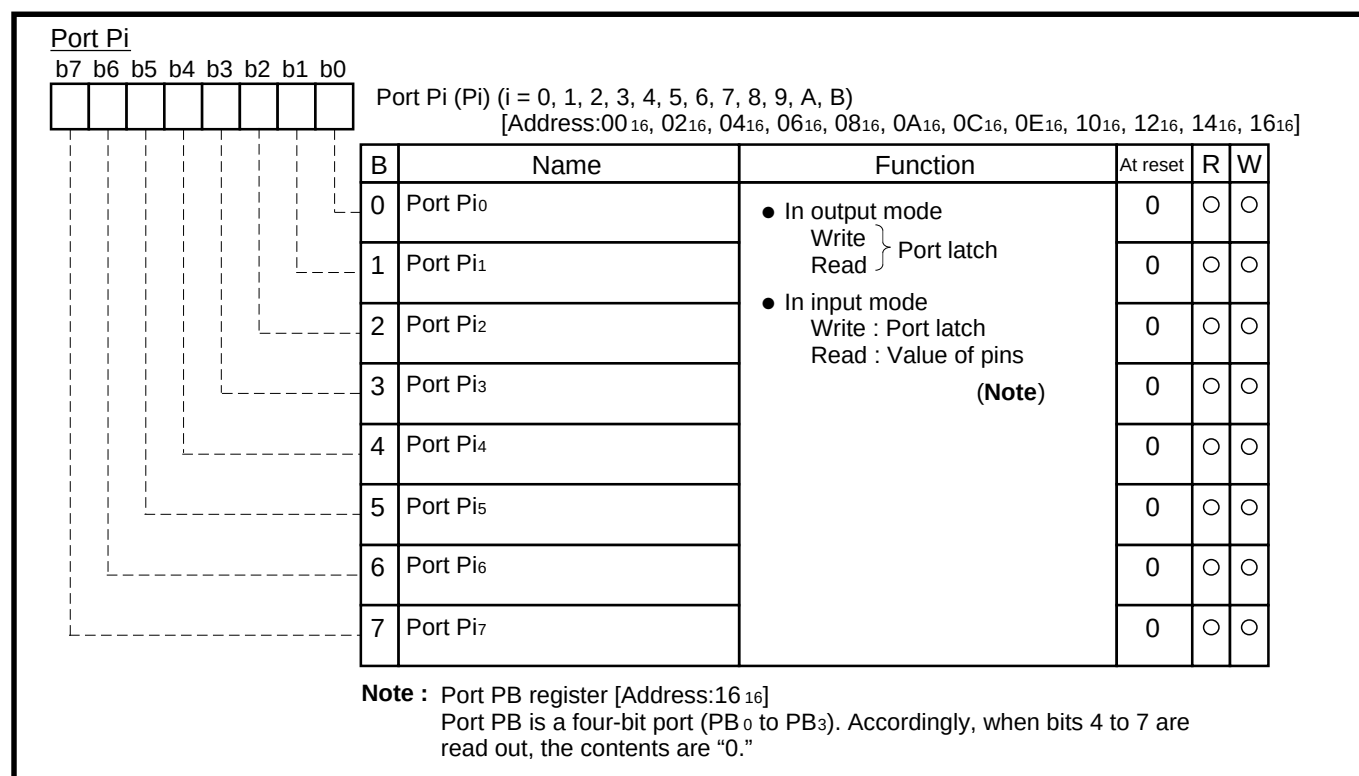


Fig. 2.1.1 Structure of Port Pi (i = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B)

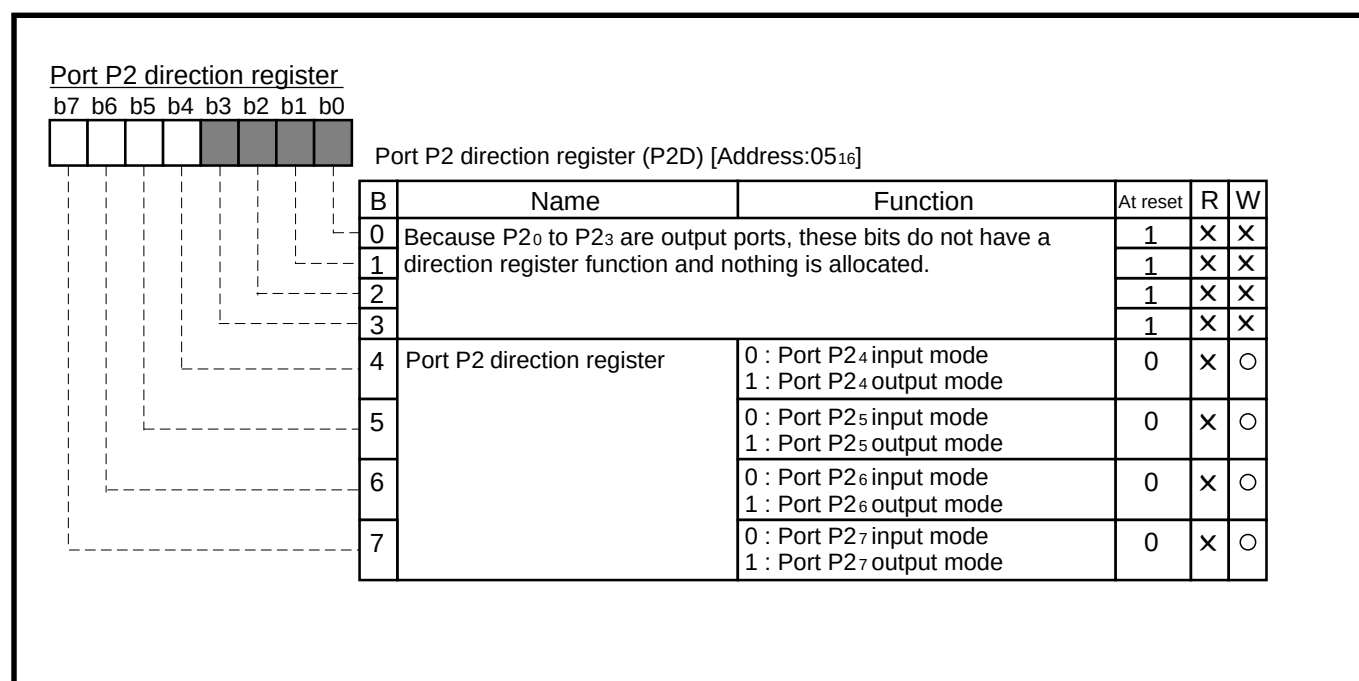


Fig. 2.1.2 Structure of Port P2 direction register

2. APPLICATION

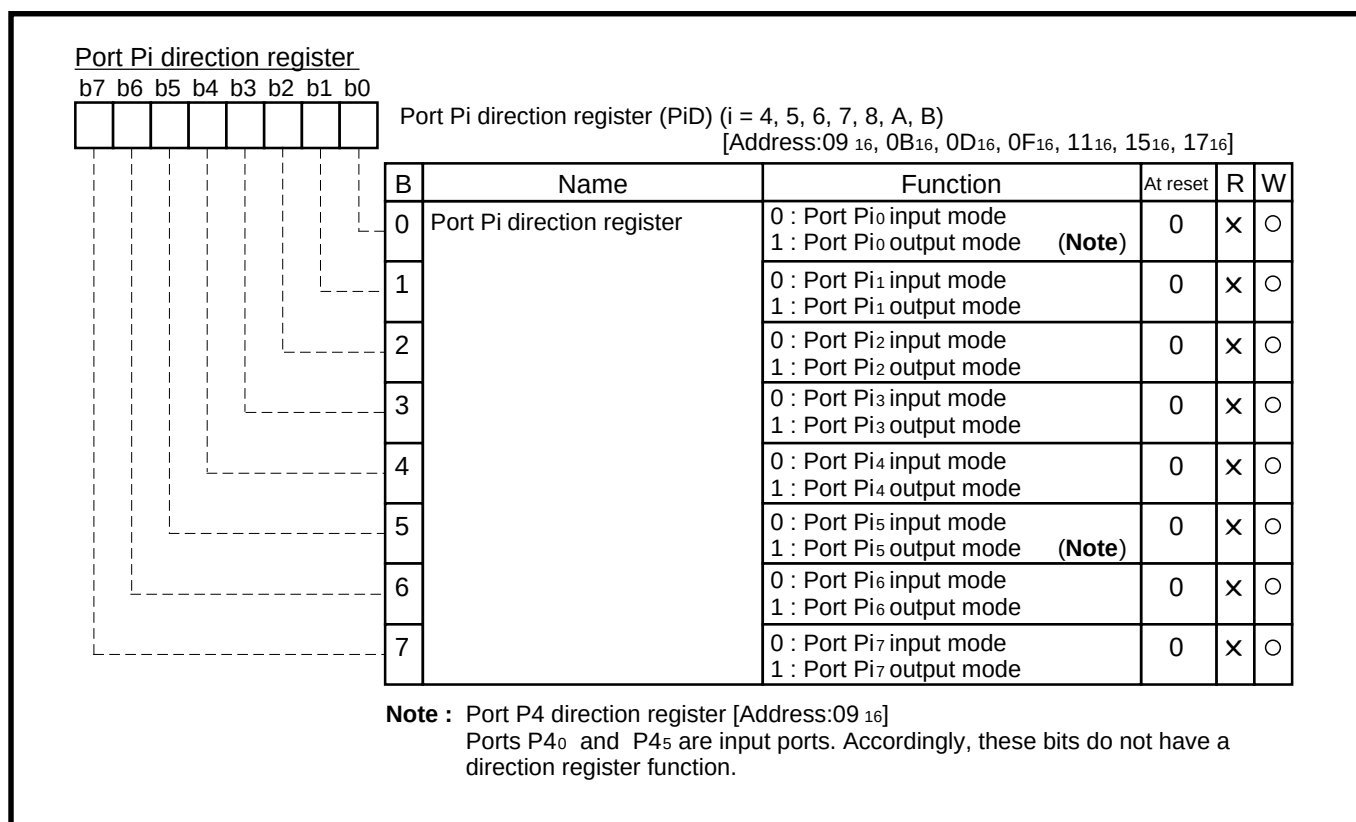


Fig. 2.1.3 Structure of Port Pi direction register (i = 4, 5, 6, 7, 8, A, B)

2.1.2 Handling of unused pins

Table 2.1.1 Handling of unused pins

Name of Pins/Ports	Handling
P0, P1, P20–P23, P3, P9	Open
P24–P27, P41–P44, P46, P47, P5, P6, P7, P8, PA, PB	- Set to the input mode and connect to Vcc or Vss through each resistor. - Set to the output mode and open at “L” or “H.”
P40	Connect to Vss(GND) through the resistor.
P45	Connect to Vcc through the resistor.
VEE, AVSS	Connect to Vss(GND).
VREF	Connect to Vss(GND) through the resistor.

2. APPLICATION

2.2 Timer

2.2.1 Related registers

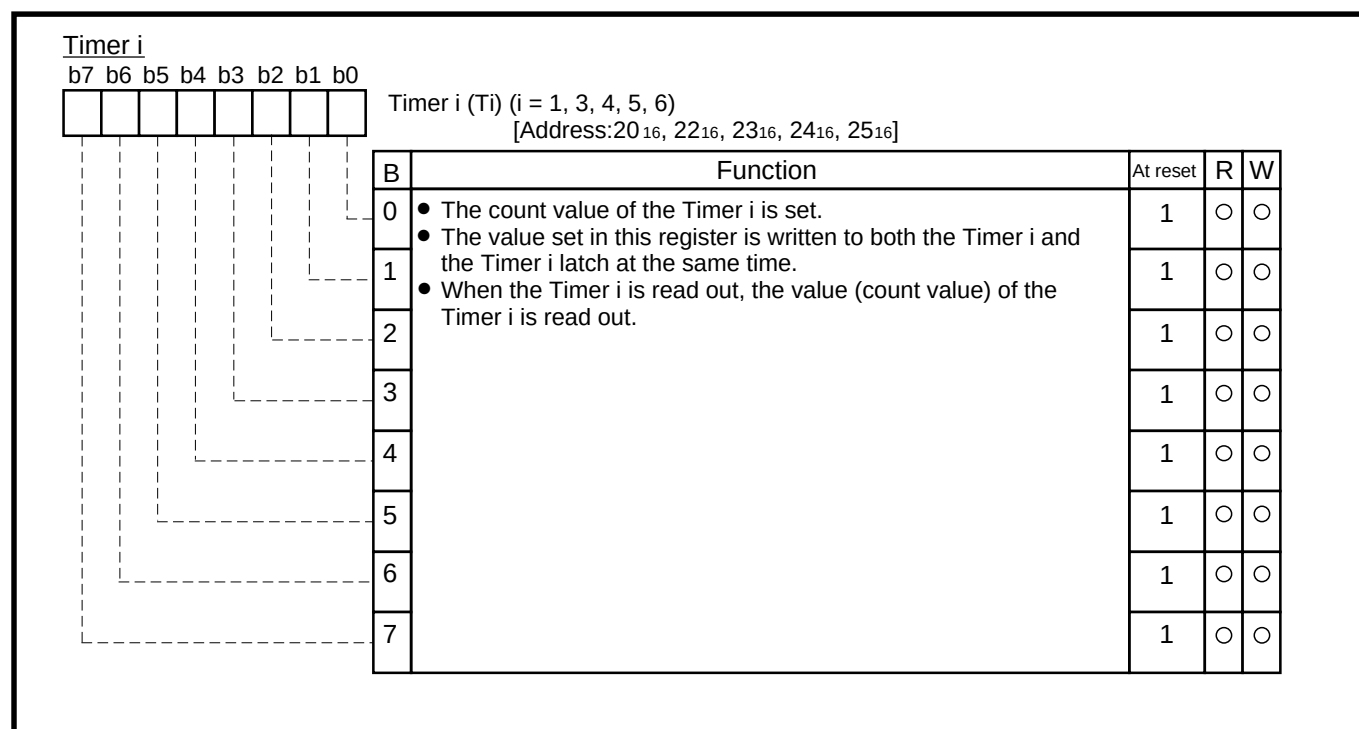


Fig. 2.2.1 Structure of Timer i (i = 1, 3, 4, 5, 6)

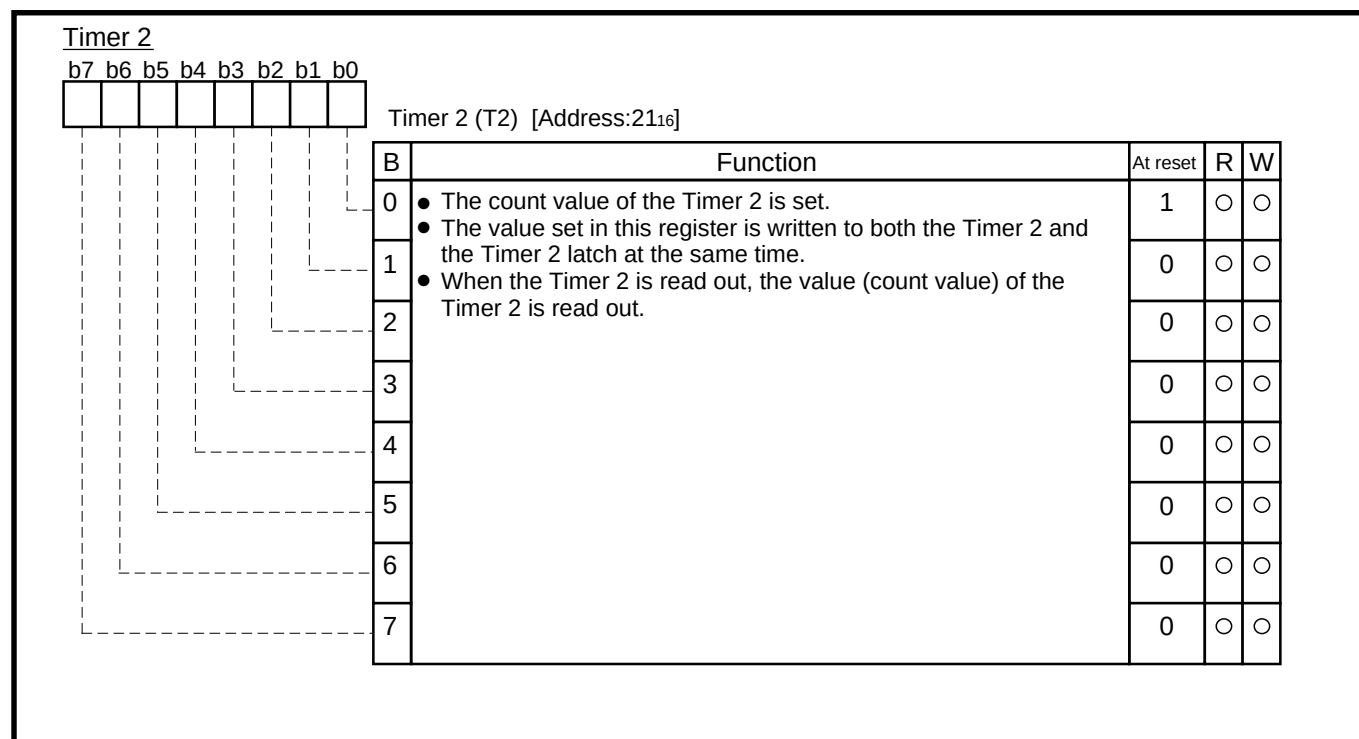


Fig. 2.2.2 Structure of Timer 2

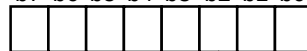
3819 Group

2.2 Timer

2. APPLICATION

Timer 6 PWM register

b7 b6 b5 b4 b3 b2 b1 b0



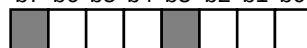
Timer 6 PWM register (T6PWM) [Address:27₁₆]

B	Function	At reset	R	W
0	In Timer 6 PWM mode Set the width of "L" of the PWM rectangular waveform.	?	○	○
1	Duty of the PWM rectangular waveform : $n/(n + m)$ Cycle : $(n + m) \times t_s$ n = a set value of the Timer 6 m = a set value of the Timer 6 PWM register ts = a cycle of the Timer 6 count source	?	○	○
2		?	○	○
3	Selection of the Timer 6 PWM mode	?	○	○
4	Set the Timer 6 operation mode selection bit of the Timer 56 mode register (Address : 2A₁₆) to "1".	?	○	○
5		?	○	○
6		?	○	○
7		?	○	○

Fig. 2.2.3 Structure of Timer 6 PWM register

Timer 12 mode register

b7 b6 b5 b4 b3 b2 b1 b0



Timer 12 mode register (T12M) [Address:28₁₆]

B	Name	Function	At reset	R	W
0	Timer 1 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 2 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 1 count source selection bit	0 : $f(X_{IN})/16$ or $f(X_{CIN})/16$ 1 : $f(X_{CIN})$	0	○	○
3	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0. "		0	○	×
4	Timer 2 count source selection bits	00 : Timer 1 underflow	0	○	○
5		01 : $f(X_{CIN})$ 10 : External count input CNTR ₀ 11 : Not available	0	○	○
6	Timer 1 output selection bit (P4 ₆)	0 : I/O port 1 : Timer 1 output	0	○	○
7	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0. "		0	○	×

Fig. 2.2.4 Structure of Timer 12 mode register

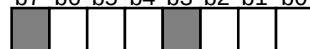
3819 Group

2.2 Timer

2. APPLICATION

Timer 34 mode register

b7 b6 b5 b4 b3 b2 b1 b0



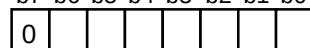
Timer 34 mode register (T34M) [Address:29₁₆]

B	Name	Function	At reset	R	W
0	Timer 3 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 4 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 3 count source selection bit	0 : f(X _{IN})/16 or f(X _{CIN})/16 1 : Timer 2 underflow	0	○	○
3	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
4	Timer 4 count source selection bits	b5 b4 00 : f(X _{IN})/16 or f(X _{CIN})/16 01 : Timer 3 underflow 10 : External count input CNTR ₁ 11 : Not available	0	○	○
5			0	○	○
6	Timer 3 output selection bit (P4 ₇)	0 : I/O port 1 : Timer 3 output	0	○	○
7	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0."		0	○	×

Fig. 2.2.5 Structure of Timer 34 mode register

Timer 56 mode register

b7 b6 b5 b4 b3 b2 b1 b0



Timer 56 mode register (T56M) [Address:2A₁₆]

B	Name	Function	At reset	R	W
0	Timer 5 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 6 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 5 count source selection bit	0 : f(X _{IN})/16 or f(X _{CIN})/16 1 : Timer 4 underflow	0	○	○
3	Timer 6 operation mode selection bit	0 : Timer mode 1 : PWM mode	0	○	○
4	Timer 6 count source selection bits	b5 b4 00 : f(X _{IN})/16 or f(X _{CIN})/16 01 : Timer 5 underflow 10 : Timer 4 underflow 11 : Not available	0	○	○
5			0	○	○
6	Timer 6 (PWM) output selection bit (P6 ₁)	0 : I/O port 1 : Timer 6 output	0	○	○
7	Fix this bit to "0."		0	○	○

Fig. 2.2.6 Structure of Timer 56 mode register

2. APPLICATION

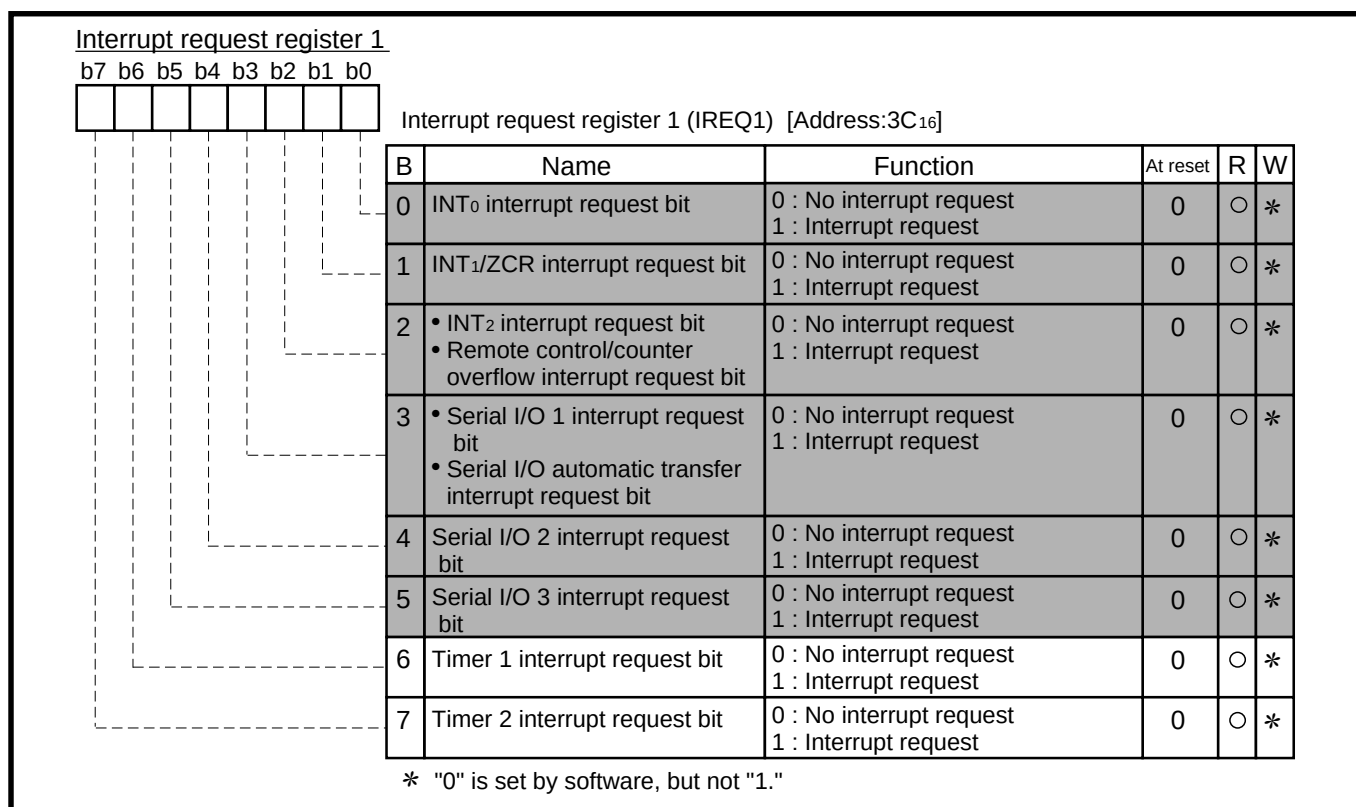


Fig. 2.2.7 Structure of Interrupt request register 1

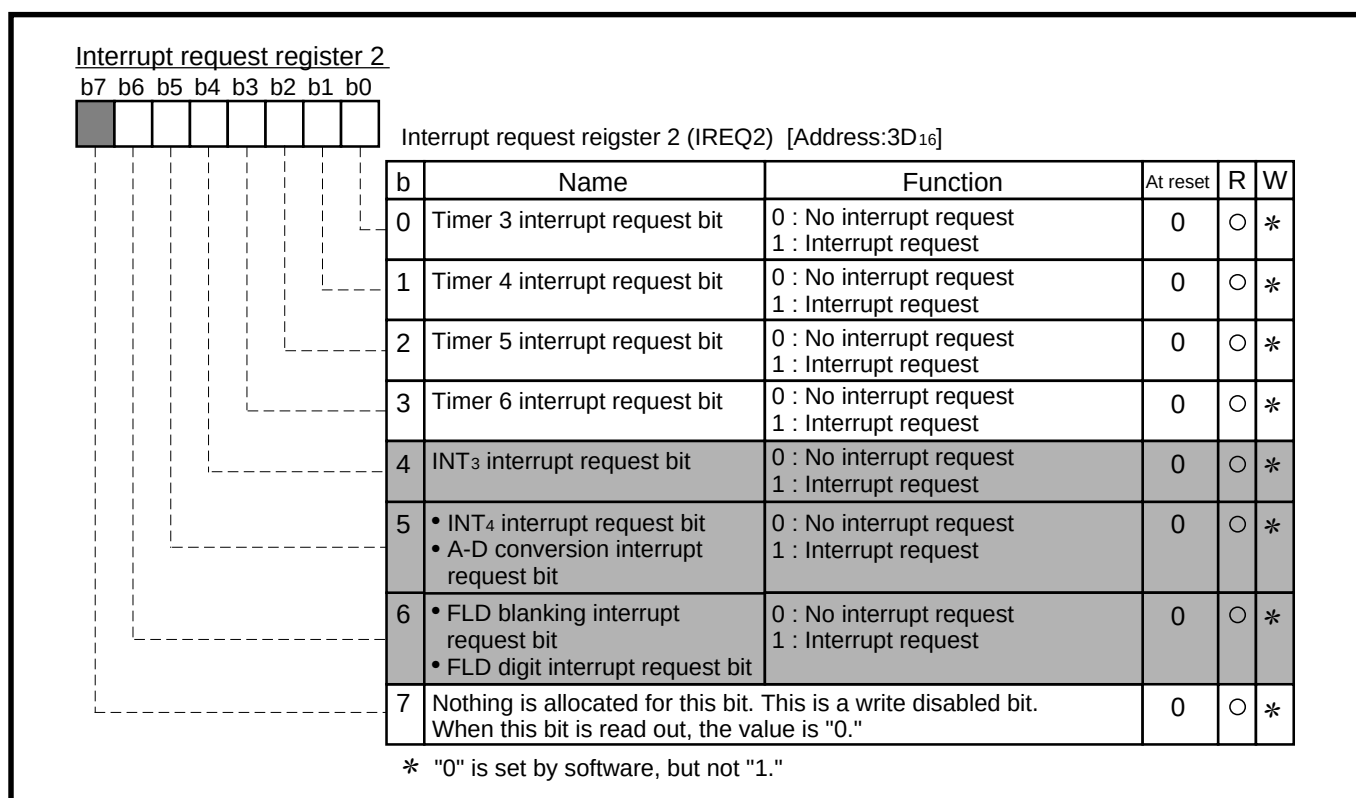


Fig. 2.2.8 Structure of Interrupt request register 2

2. APPLICATION

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

--	--	--	--	--	--	--	--

Interrupt control register 1 (ICON1) [Address:3E₁₆]

b	Name	Function	At reset	R	W
0	INT ₀ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT ₁ /ZCR interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	• INT ₂ interrupt enable bit • Remote control/counter overflow interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	• Serial I/O 1 interrupt enable bit • Serial I/O automatic transfer interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Serial I/O 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Serial I/O 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 2.2.9 Structure of Interrupt control register 1

Interrupt control register 2

b7 b6 b5 b4 b3 b2 b1 b0

0							
---	--	--	--	--	--	--	--

Interrupt control register 2 (ICON2) [Address:3F₁₆]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Timer 4 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Timer 5 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Timer 6 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT ₃ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	• INT ₄ interrupt enable bit • A-D conversion interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	• FLD blanking interrupt enable bit • FLD digit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix this bit to "0."		0	○	○

Fig. 2.2.10 Structure of Interrupt control register 2

2. APPLICATION

2.2.2 Timer application examples

(1) Basic functions and uses

[Function 1] Control of Event interval (Timers 1 to 6)

The Timer count stop bit is set to "0" after setting a count value to a timer. Then a timer interrupt request occurs after a certain period.

- [Use] • Generation of an output signal timing
 • Generation of a waiting time

[Function 2] Control of Cyclic operation : Generation of synchronous timing (Timers 1 to 6)

The value of a timer latch is automatically written to a timer each time a timer underflows, and a timer interrupt request occurs.

- [Use] • Generation of cyclic interrupts
 • Clock function (measurement of one second) → Application example 1
 • Control of a main routine cycle

[Function 3] Output of Rectangular waveform (Timers 1 and 3)

The output level of the TOUT pin is inverted every time a timer underflows. To output long-interval rectangular waveforms (when division of 8 bits or more is necessary), the Timers 2 and 3 are connected .

- [Use] • A piezoelectric buzzer output → Application example 2
 • Generation of the remote-control carrier waveforms

[Function 4] Count of External pulse (Timers 2 and 4)

External pulses input to the CNTR pin are selected as a timer count source.

- [Use] • Measurement of frequency (judging if the Video synchronization signal exits) → Application example 3
 • Division of external pulses and generation of interrupts in a cycle based on an external pulse.
 (count of a reel pulse)

[Function 5] Output of PWM signal (Timer 6)

The pulses with each specified intervals of "H" and "L" are output.

- [Use] • Control of an electronic volume (connected with VCA)

2. APPLICATION

(2) Timer application example 1: Clock function (measurement of one second)

Outline : The input clock is divided by a timer so that the clock counts up every second.

- Specifications :**
- The clock $f(X_{IN}) = 4.19 \text{ MHz}$ (2^{22}) is divided by a timer.
 - The Timer 3 interrupt request bit is checked in the main routine, and the clock is counted up when an interrupt request occurs.
 - Another interrupt processing is executed in a parallel, so a timer interrupt occurs every $244 \mu\text{s}$.

Figure 2.2.11 shows a connection of timers and a setting of division ratios, Figures 2.2.12 and 2.2.13 show a setting of related registers, and Figure 2.2.14 shows a control procedure.

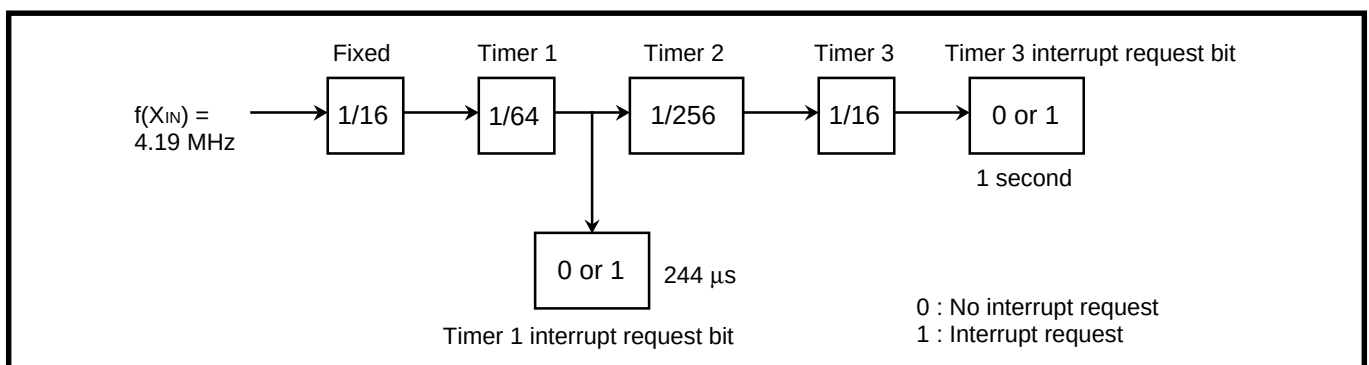


Fig. 2.2.11 Connection of timers and setting of division ratios [Clock function]

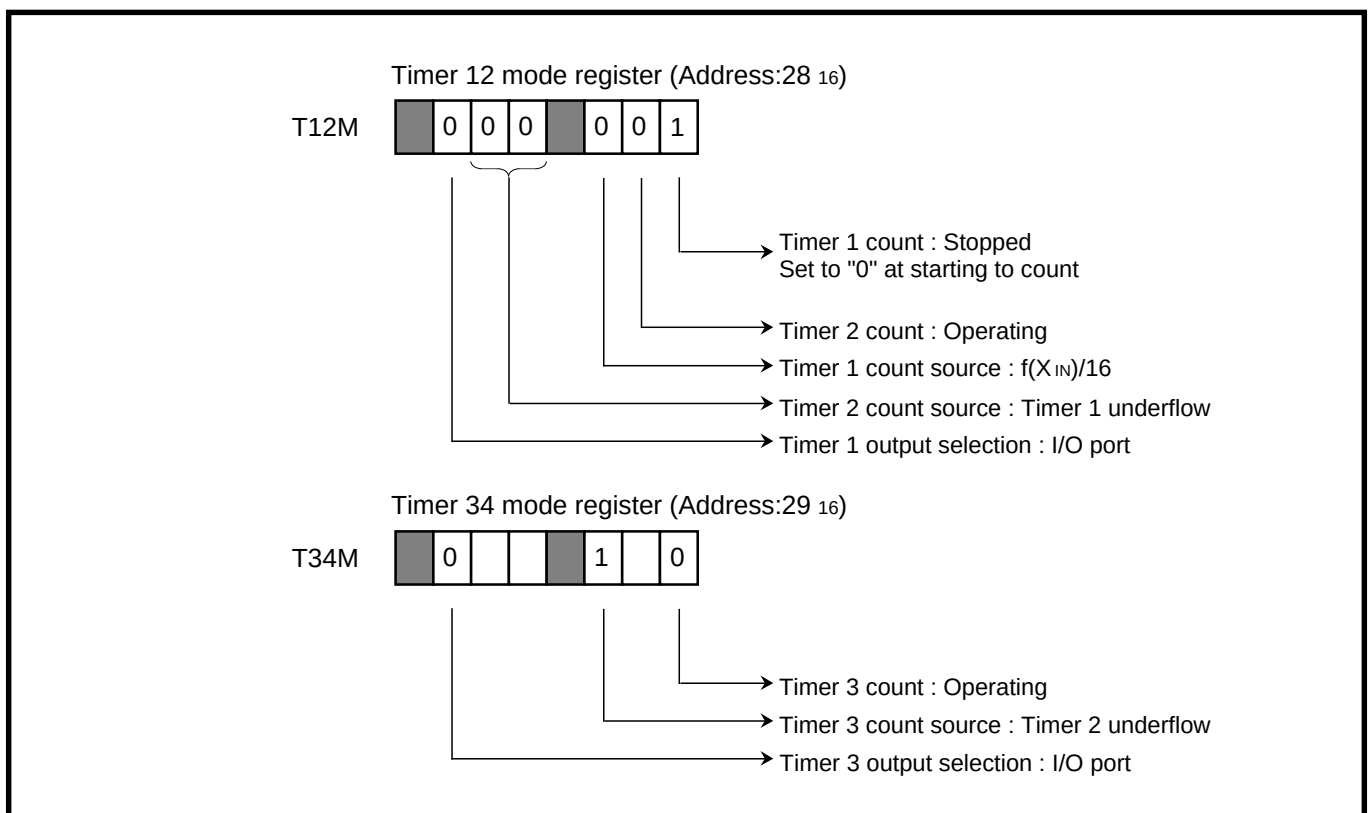


Fig. 2.2.12 Setting of related registers (1) [Clock function]

2. APPLICATION

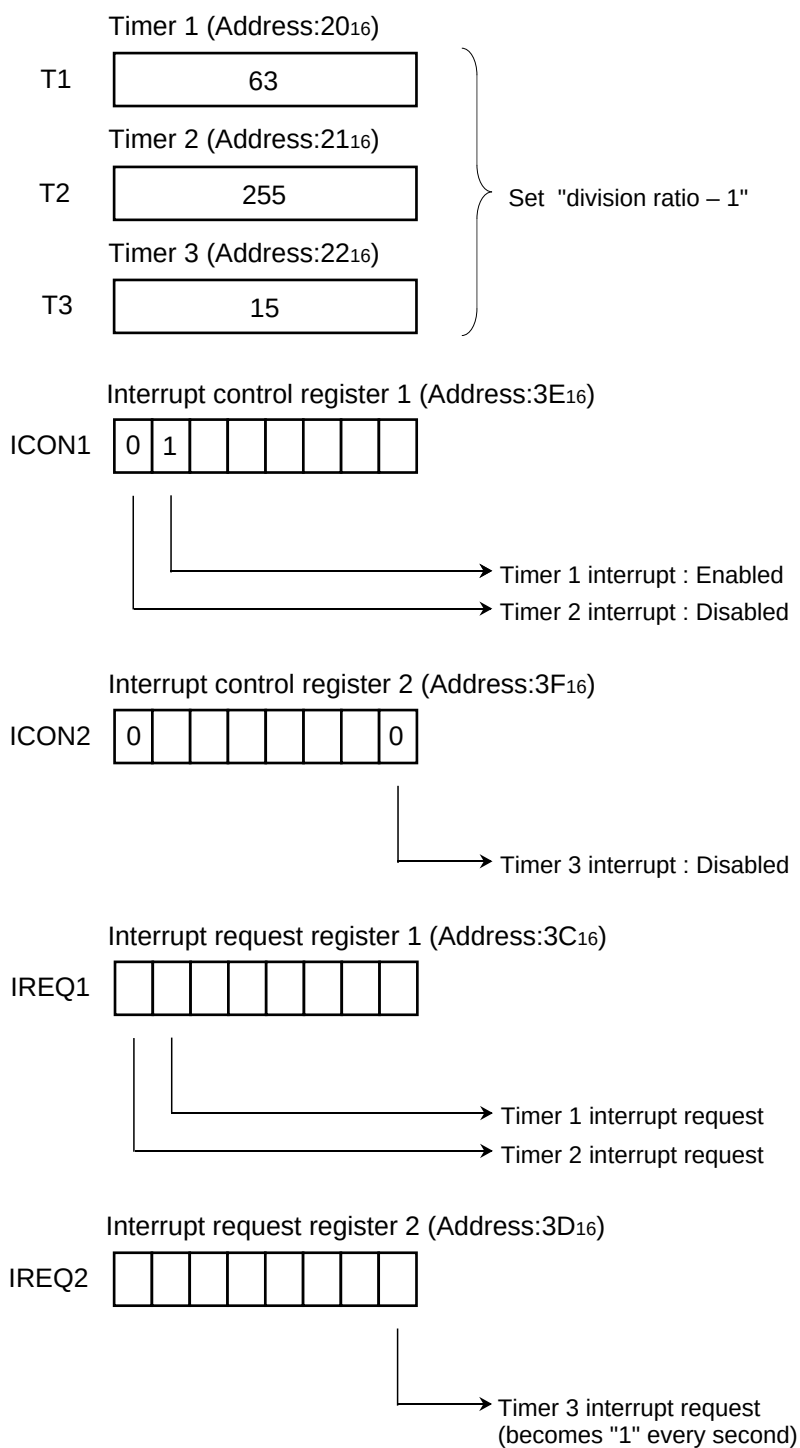


Fig. 2.2.13 Setting of related registers (2) [Clock function]

2. APPLICATION

Control procedure :

Figure 2.2.14 shows a control procedure.

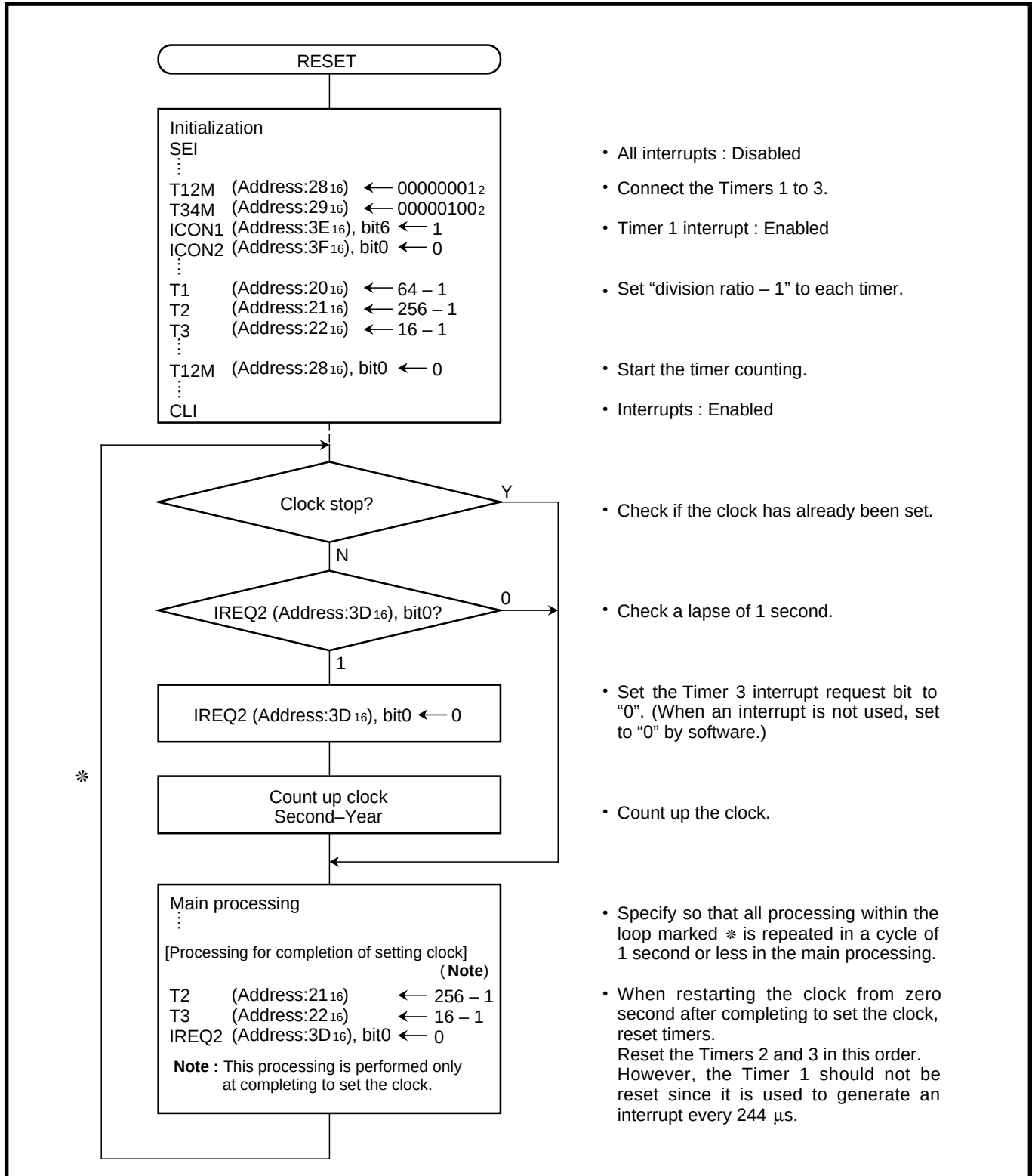


Fig. 2.2.14 Control procedure [Clock function]

2. APPLICATION

(3) Timer application example 2: Piezoelectric buzzer output

Outline : The rectangular waveform output function of a timer is applied for a piezoelectric buzzer output.

- Specifications :**
- The rectangular waveform, 2 kHz (2048 Hz) which is divided clock $f(X_{IN}) = 4.19 \text{ MHz}$ is output from the T3OUT pin.
 - The level of the T3OUT pin fixes to "H" while a piezoelectric buzzer output is stopped.

Figure 2.2.15 shows an example of a peripheral circuit, and Figure 2.2.16 shows a connection of the timer and setting of the division ratio.

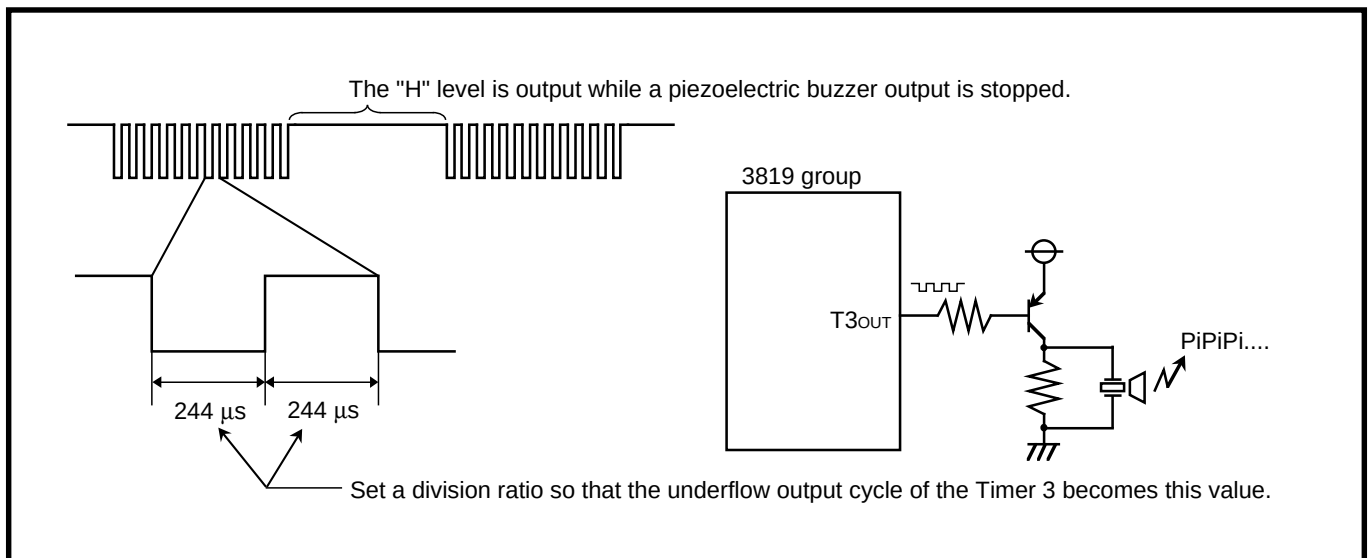


Fig. 2.2.15 Example of a peripheral circuit

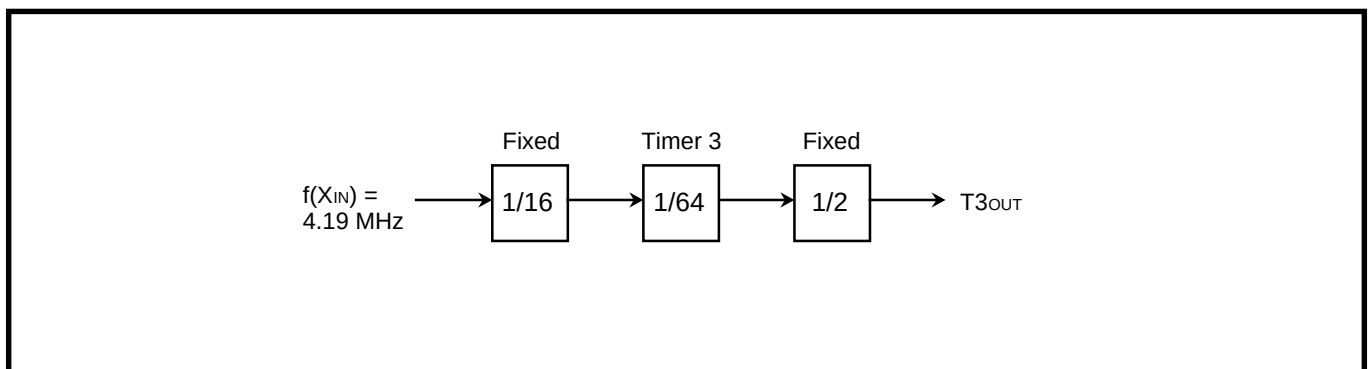


Fig. 2.2.16 Connection of the timer and setting of the division ratio [Piezoelectric buzzer output]

2. APPLICATION

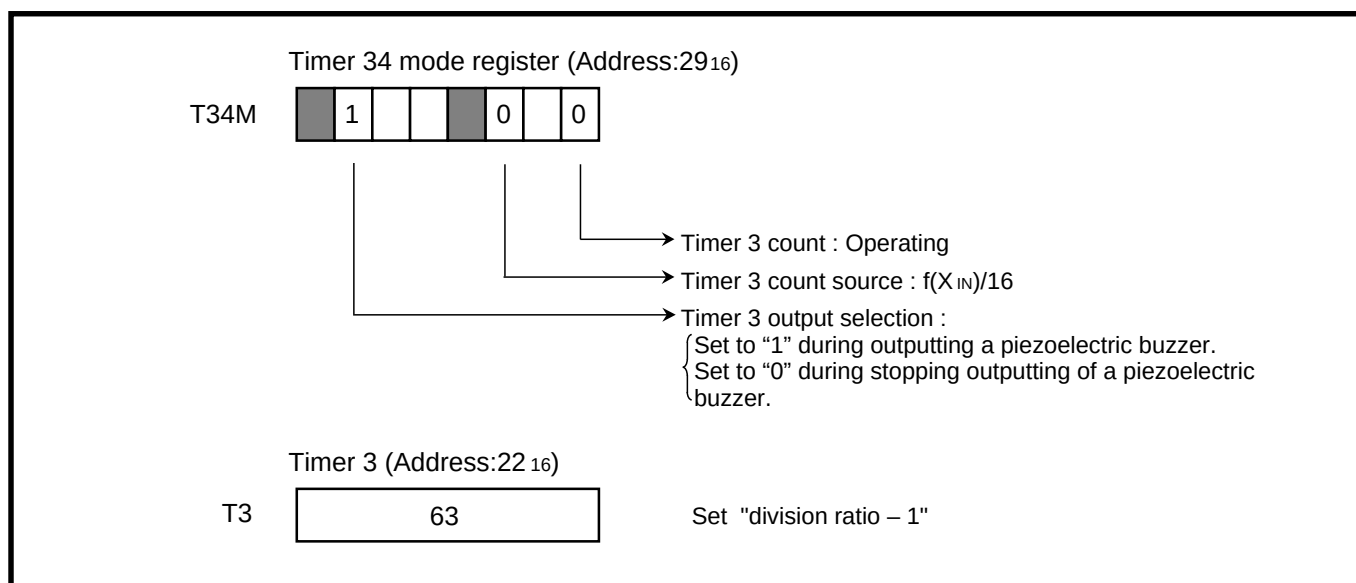


Fig. 2.2.17 Setting of related registers [Piezoelectric buzzer output]

Control procedure :

Figure 2.2.18 shows a control procedure.

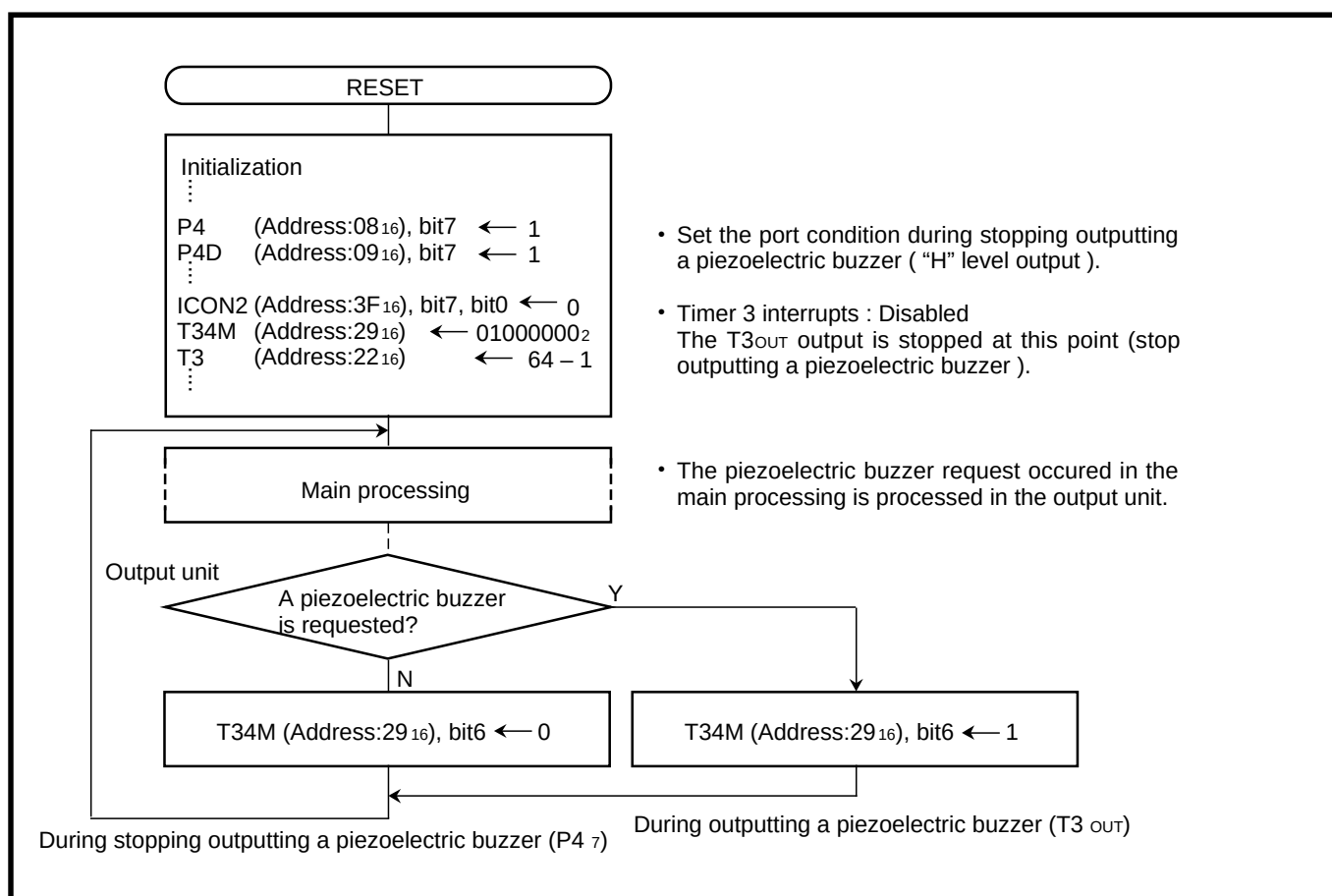


Fig. 2.2.18 Control procedure [Piezoelectric buzzer output]

2. APPLICATION

(4) Timer application example 3 : Measurement of frequency (judging if Video synchronization signal exists)

Outline : The pulses input to the External count input pin (CNTR) are counted by a timer to judge if the frequency is within a certain range.

- Specifications** :
- The Video synchronization signal is input to the CNTR₁ pin and counted by the Timer 4.
 - A count value is read out at the interval of about 2 ms (Timer 1 interrupt interval : $244 \mu\text{s} \times 8$). When the count value is 28 to 40, it is regarded as the existence of the Video synchronization signal.
 - Because the timer is a down-counter, the count value is compared with 227 to 215.*
- * $227 \text{ to } 215 = 255 \text{ (initialized value of counter)} - 28 \text{ to } 40 \text{ (the number of valid value)}$.

Figure 2.2.19 shows a method for judging if Video synchronization signal exists, and Figure 2.2.20 shows a setting of related registers.

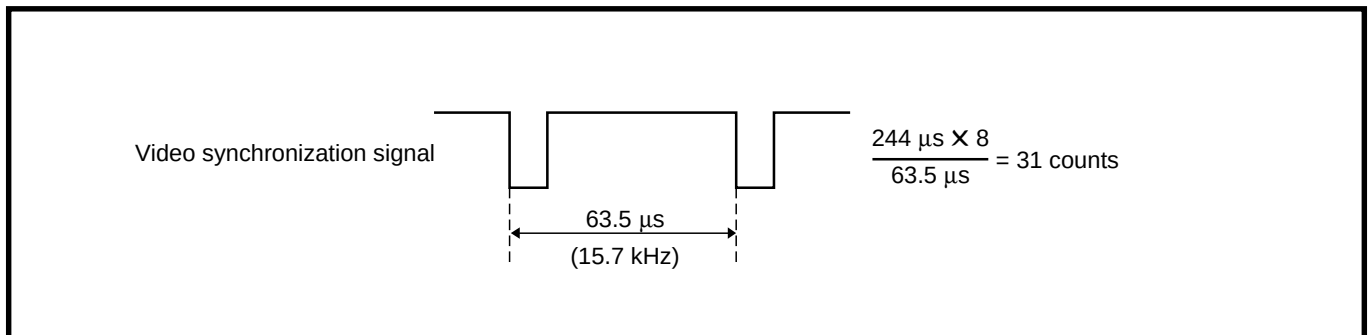


Fig 2.2.19 A method for judging if Video synchronization signal exists

2. APPLICATION

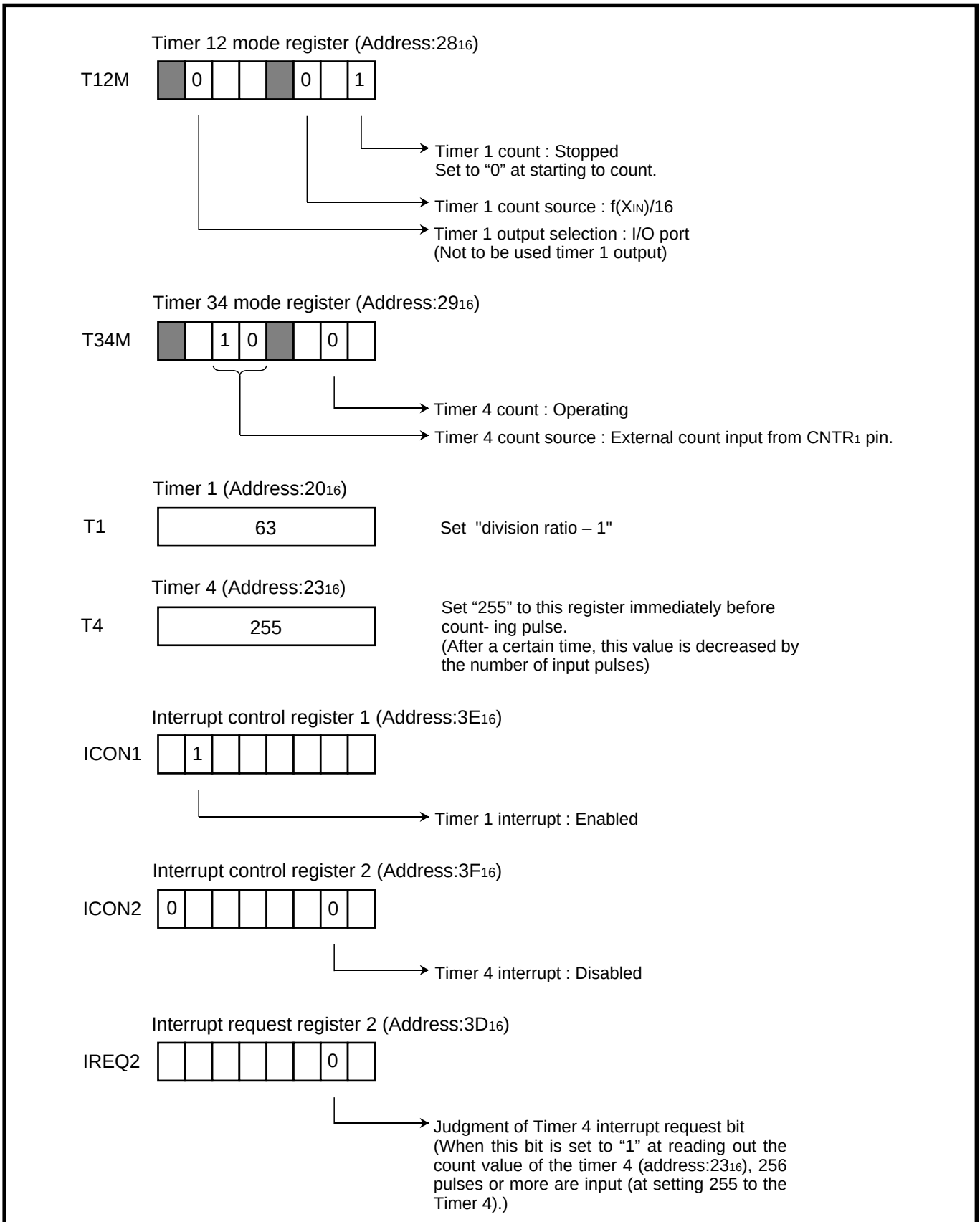


Fig. 2.2.20 Setting of related registers [Measurement of frequency]

2. APPLICATION

Control procedure :

Figure 2.2.21 shows a control procedure.

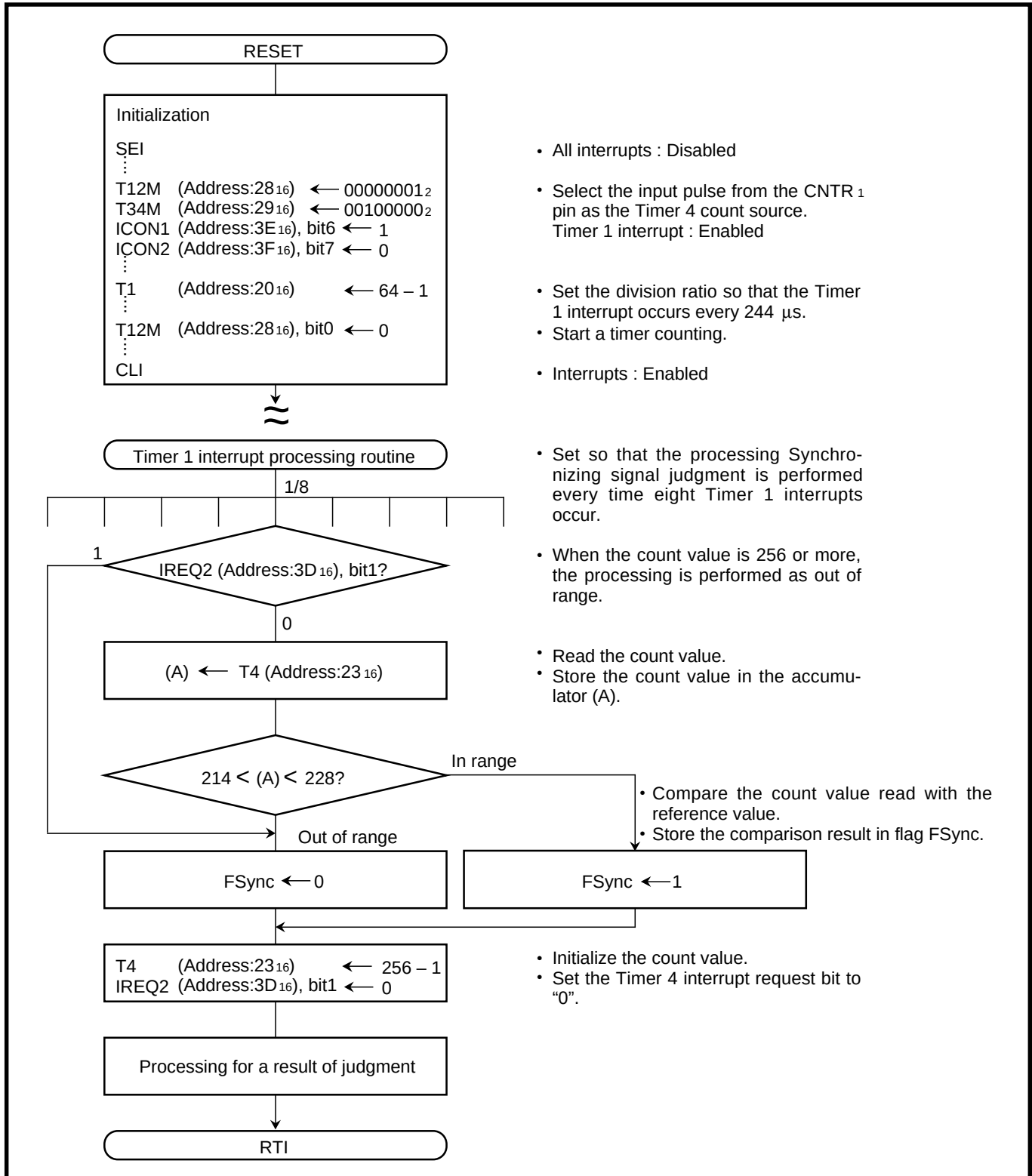


Fig. 2.2.21 Control procedure [Measurement of frequency]

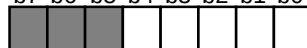
2. APPLICATION

2.3 Serial I/O

2.3.1 Related registers

Serial I/O automatic transfer data pointer

b7 b6 b5 b4 b3 b2 b1 b0



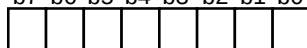
Serial I/O automatic transfer data pointer (SIODP) [Address:18₁₆]

B	Function	At reset	R	W
0	Indicate an address of Serial I/O automatic transfer RAM.	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."	0	○	×
6		0	○	×
7		0	○	×

Fig. 2.3.1 Structure of Serial I/O automatic transfer data pointer

Serial I/O 1 control register

b7 b6 b5 b4 b3 b2 b1 b0



Serial I/O 1 control register (SIO1CON) [Address:19₁₆]

B	Name	Function	At reset	R	W
0	Internal synchronous clock selection bits	b2 b1 b0 000 : f(X _{IN})/8 or f(X _{CIN})/8	0	○	○
1		001 : f(X _{IN})/16 or f(X _{CIN})/16	0	○	○
2		010 : f(X _{IN})/32 or f(X _{CIN})/32	0	○	○
		011 : f(X _{IN})/64 or f(X _{CIN})/64	0	○	○
		110 : f(X _{IN})/128 or f(X _{CIN})/128	0	○	○
		111 : f(X _{IN})/256 or f(X _{CIN})/256	0	○	○
3	Serial I/O 1 port selection bit (P6 ₅ , P6 ₆ , P6 ₇ *)	0 : I/O port 1 : SOUT ₁ , SCLK ₁₁ , SCLK ₁₂ * signal pins	0	○	○
4	SRDY ₁ output selection bit (P6 ₇)	0 : I/O port 1 : SRDY ₁ /CS* signal pin (Note)	0	○	○
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○
6	Synchronous clock selection bit	0 : External clock 1 : Internal clock	0	○	○
7	P6 ₅ /SOUT ₁ P-channel output disable bit	0 : CMOS output (in output mode) 1 : N-channel open-drain output (in output mode)	0	○	○

* Valid only in the Serial I/O automatic transfer mode

Note : When an external clock is selected in the serial I/O 1 automatic transfer mode, the SRDY₁ signal pin is used as the CS signal input pin.

Fig. 2.3.2 Structure of Serial I/O 1 control register

2. APPLICATION

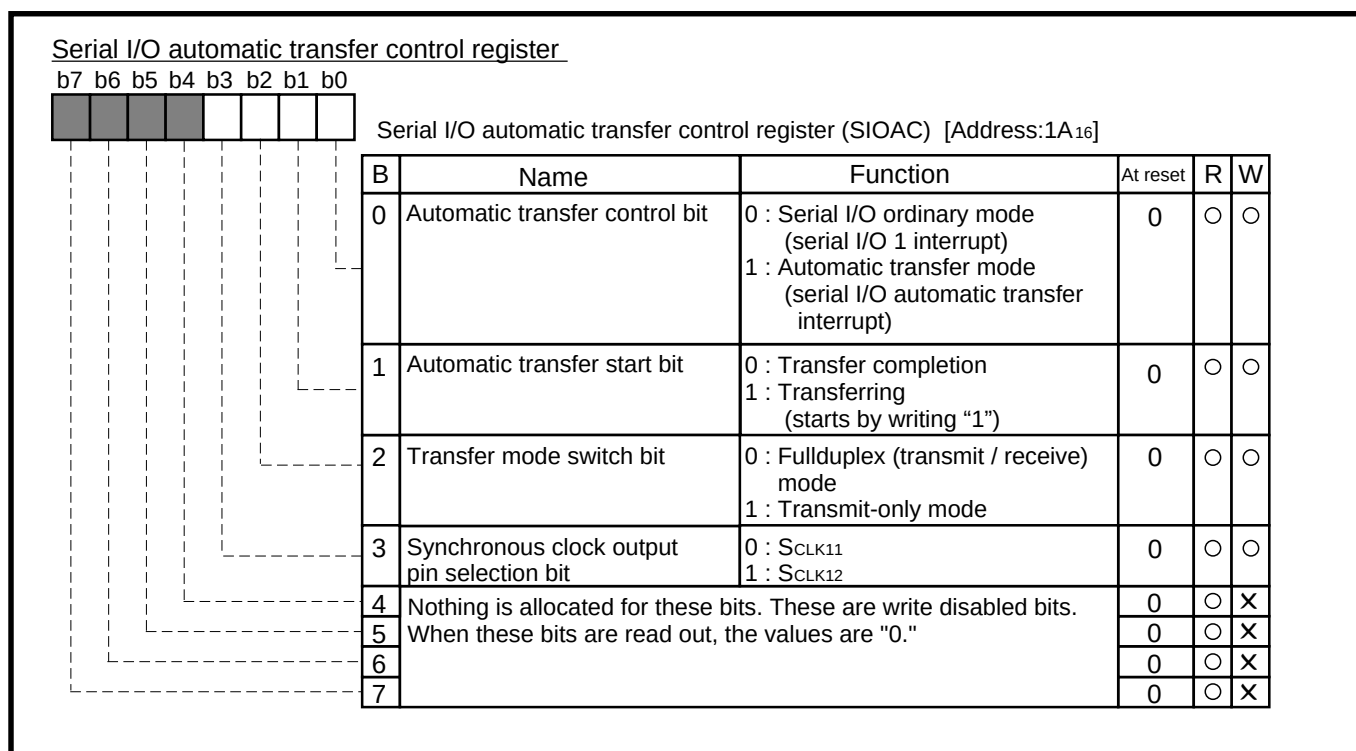


Fig. 2.3.3 Structure of Serial I/O automatic transfer control register

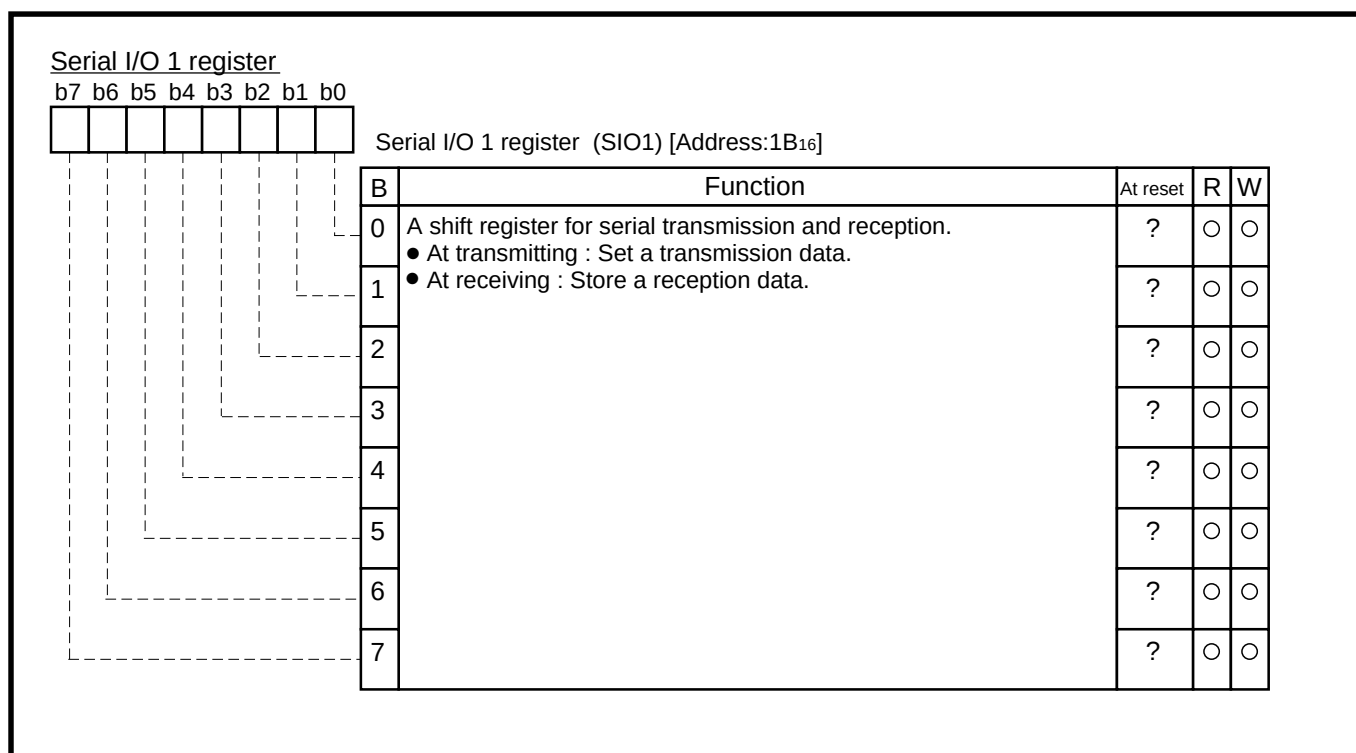
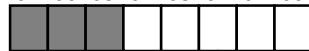


Fig. 2.3.4 Structure of Serial I/O 1 register

2. APPLICATION

Serial I/O automatic transfer interval register

b7 b6 b5 b4 b3 b2 b1 b0



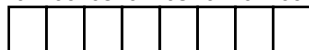
Serial I/O automatic transfer interval register (SIOAI) [Address:1C16]

B	Function	At reset	R	W
0	$T_i = (n + 2) \times T_c$ $\left\{ \begin{array}{l} T_i = \text{a length of transfer interval} \\ n = \text{a setting value} \\ T_c = \text{a length of a bit of transfer clock} \end{array} \right.$	0	○	○
1		0	○	○
2		0	○	○
3		0	○	○
4		0	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."	0	○	×
6		0	○	×
7		0	○	×

Fig. 2.3.5 Structure of Serial I/O automatic transfer interval register

Serial I/O 2 control register

b7 b6 b5 b4 b3 b2 b1 b0



Serial I/O 2 control register (SIO2CON) [Address:1D16]

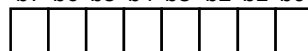
B	Name	Function	At reset	R	W
0	Internal synchronous clock selection bits	b2 b1 b0 000 : $f(X_{IN})/8$ or $f(X_{CIN})/8$	0	○	○
1		001 : $f(X_{IN})/16$ or $f(X_{CIN})/16$	0	○	○
2		010 : $f(X_{IN})/32$ or $f(X_{CIN})/32$	0	○	○
		011 : $f(X_{IN})/64$ or $f(X_{CIN})/64$			
		110 : $f(X_{IN})/128$ or $f(X_{CIN})/128$			
		111 : $f(X_{IN})/256$ or $f(X_{CIN})/256$			
3	Serial I/O 2 port selection bit (P5 ₁ , P5 ₂)	0 : I/O port 1 : SOUT2, SCLK2 signal pins	0	○	○
4	$\overline{SRDY2}$ output selection bit (P5 ₃)	0 : I/O port 1 : $\overline{SRDY2}$ signal pin	0	○	○
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○
6	Synchronous clock selection bit	0 : External clock 1 : Internal clock	0	○	○
7	P5 ₁ /SOUT2 P-channel output disable bit	0 : CMOS output (in output mode) 1 : N-channel open-drain output (in output mode)	0	○	○

Fig. 2.3.6 Structure of Serial I/O 2 control register

2. APPLICATION

Serial I/O 3 control register

b7 b6 b5 b4 b3 b2 b1 b0



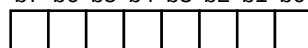
Serial I/O 3 control register (SIO3CON) [Address:1E16]

B	Name	Function	At reset	R	W
0	Internal synchronous clock selection bits	b2 b1 b0 000 : $f(X_{IN})/8$ or $f(X_{CIN})/8$	0	○	○
1		001 : $f(X_{IN})/16$ or $f(X_{CIN})/16$	0	○	○
2		010 : $f(X_{IN})/32$ or $f(X_{CIN})/32$	0	○	○
		011 : $f(X_{IN})/64$ or $f(X_{CIN})/64$			
		110 : $f(X_{IN})/128$ or $f(X_{CIN})/128$			
		111 : $f(X_{IN})/256$ or $f(X_{CIN})/256$			
3	Serial I/O 3 port selection bit (P5 ₅ , P5 ₆)	0 : I/O port 1 : SOUT ₃ , SCLK ₃ signal pins	0	○	○
4	SRDY ₃ output selection bit (P5 ₇)	0 : I/O port 1 : SRDY ₃ signal pin	0	○	○
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○
6	Synchronous clock selection bit	0 : External clock 1 : Internal clock	0	○	○
7	P5 ₅ /SOUT ₃ P-channel output disable bit	0 : CMOS output (in output mode) 1 : N-channel open-drain output (in output mode)	0	○	○

Fig. 2.3.7 Structure of Serial I/O 3 control register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0



Interrupt request register 1 (IREQ1) [Address:3C16]

B	Name	Function	At reset	R	W
0	INT ₀ interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	INT ₁ /ZCR interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	• INT ₂ interrupt request bit • Remote control/counter overflow interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	• Serial I/O 1 interrupt request bit • Serial I/O automatic transfer interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	Serial I/O 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	Serial I/O 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	Timer 1 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Timer 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*

* "0" is set by software, but not "1."

Fig. 2.3.8 Structure of Interrupt request register 1

2. APPLICATION

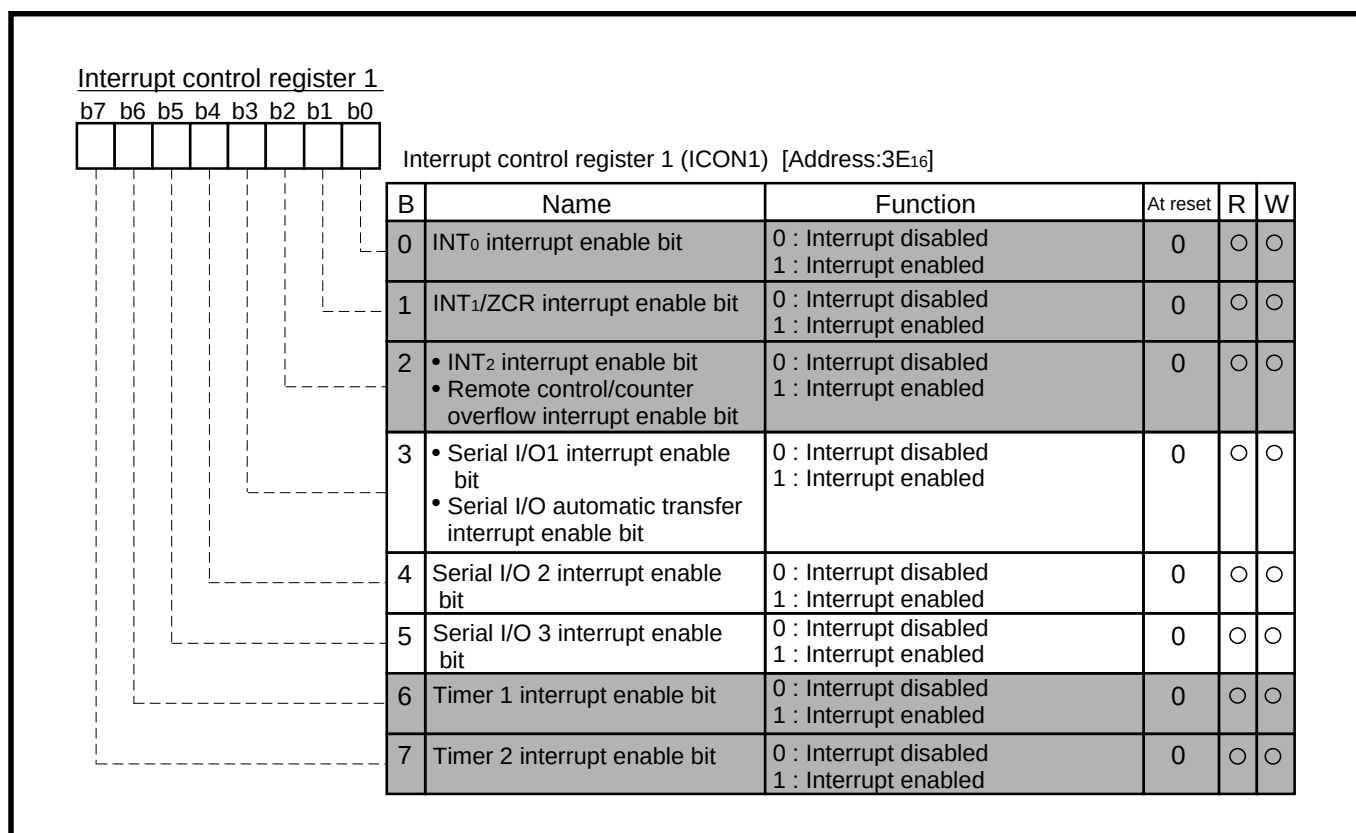


Fig. 2.3.9 Structure of Interrupt control register 1

2. APPLICATION

2.3.2 Serial I/O connection examples

(1) Control of peripheral IC equipped with CS pin

In any application, the automatic transfer function is available.

Figure 2.3.10 shows connection examples of a peripheral IC equipped with the CS pin.

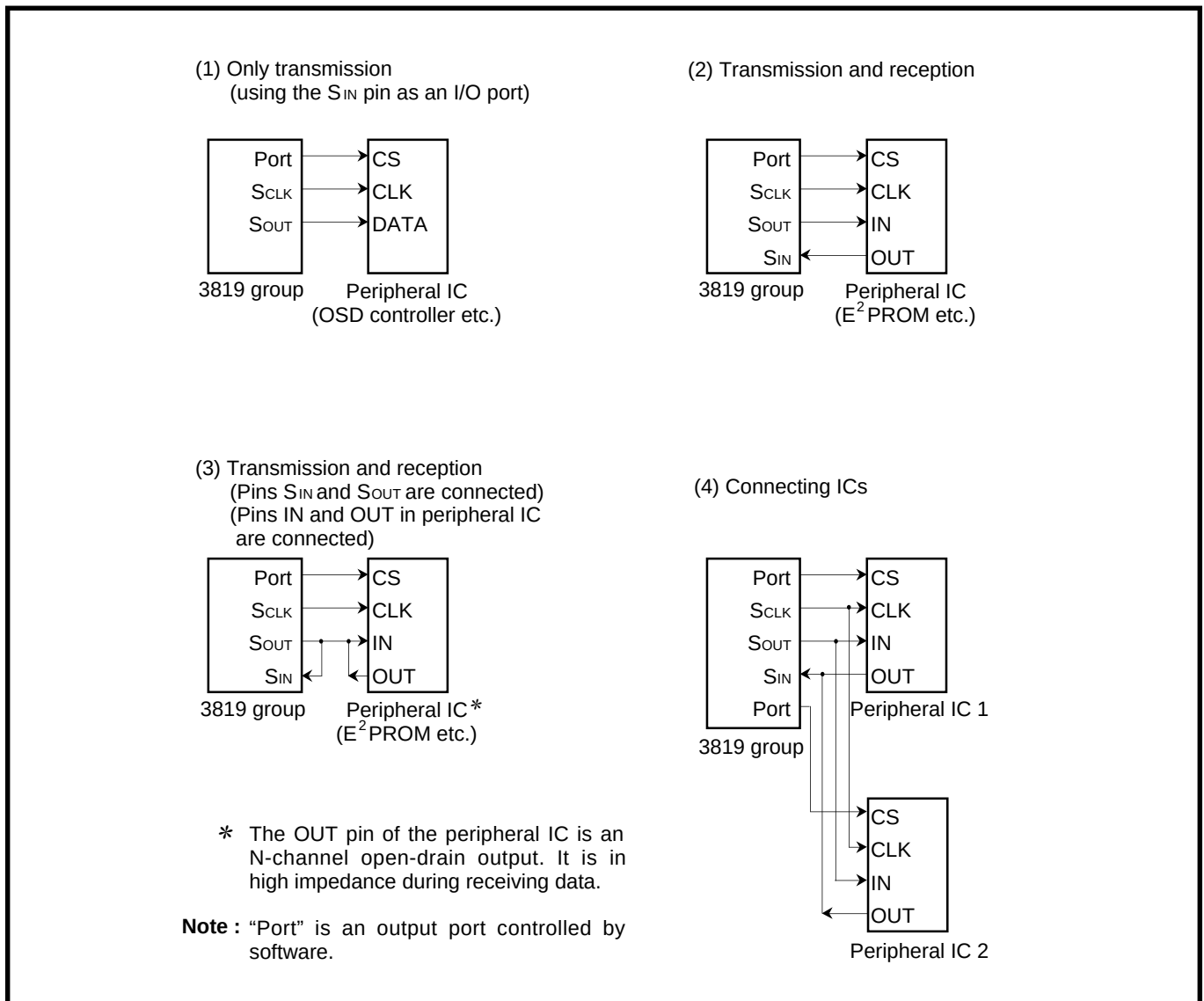


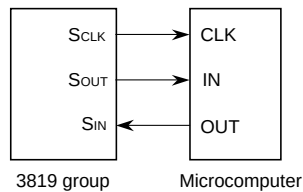
Fig. 2.3.10 Serial I/O connection examples (1)

2. APPLICATION

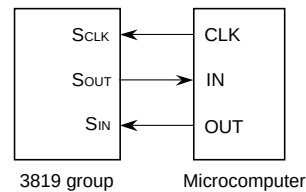
(2) Connection with microcomputer

Figure 2.3.11 shows connection examples of the other microcomputers.

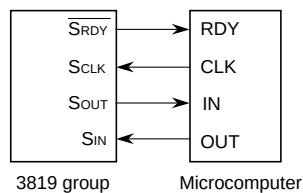
- (1) Selecting an internal clock
(Possible of using an automatic transfer function)



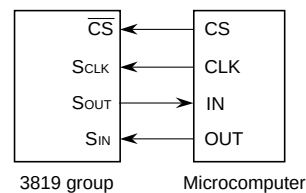
- (2) Selecting an external clock
(Possible of using an automatic transfer function)



- (3) Using the $\overline{\text{SRDY}}$ signal output function
(Selecting an external clock, and not using an automatic transfer function)



- (4) Using the $\overline{\text{CS}}$ signal reception function
(Selecting an external clock, and using an automatic transfer function)



- (5) Using the CLK signal output pin switch (SCLK₁₂) function
(Selecting an internal clock, and using an automatic transfer function)

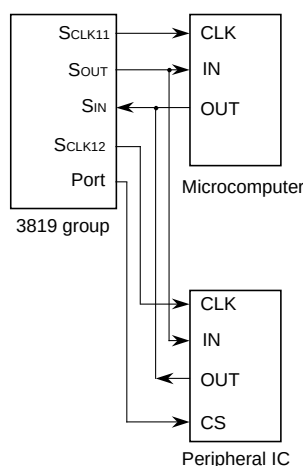


Fig. 2.3.11 Serial I/O connection examples (2)

2. APPLICATION

2.3.3 Setting of serial I/O mode

Whether $\overline{\text{SRDY}}$ signal output, $\overline{\text{CS}}$ signal receive and CLK signal output pin switch (SCLK12) functions can be selected to use or not by the following conditions:

- Serial I/O circuits (serial I/O 1 or serial I/O 2)
- The automatic transfer function is ON or OFF (at the serial I/O 1 only)
- Transfer clock (internal clock or external clock)

Figure 2.3.12 shows a setting of serial I/O mode.

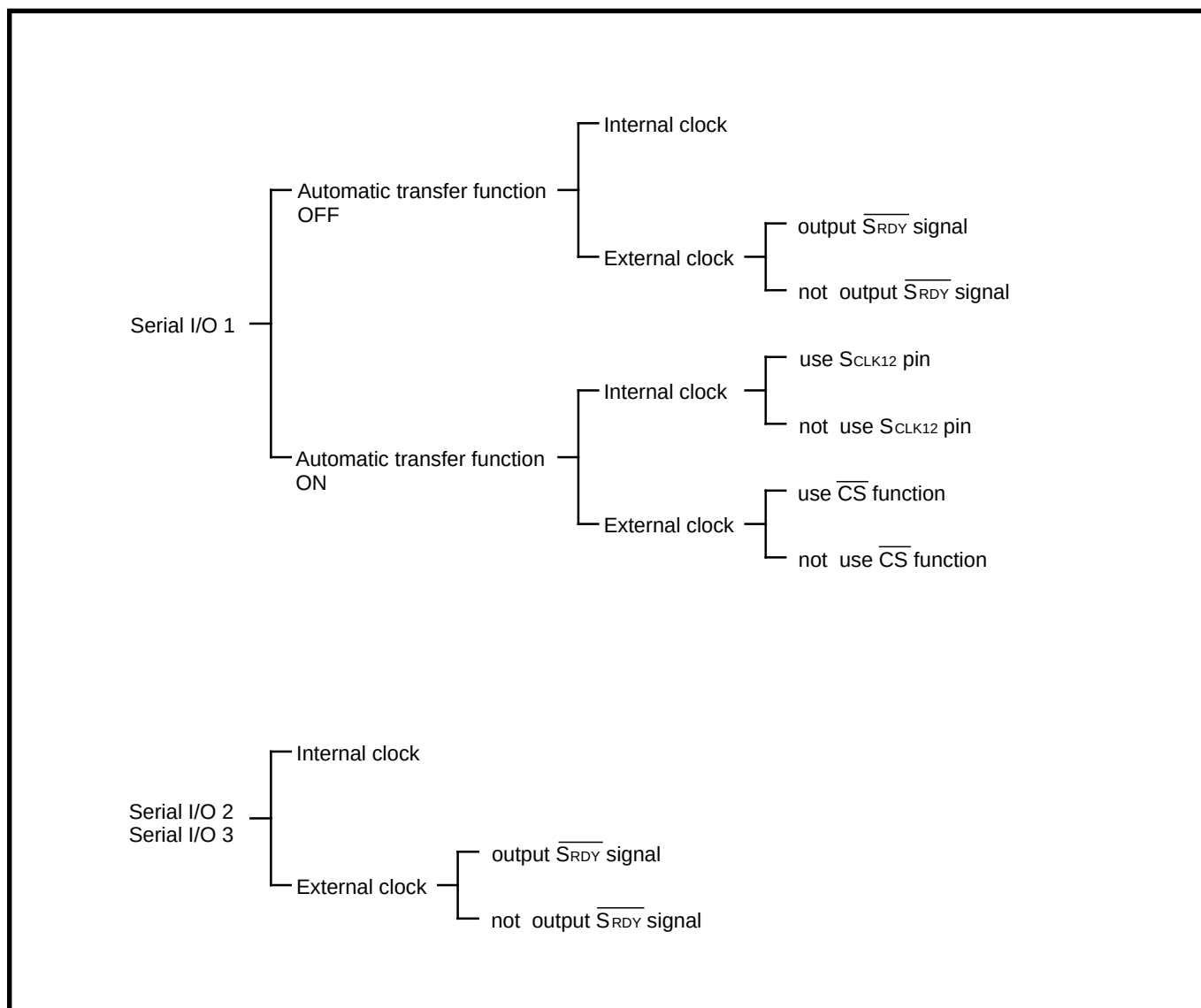


Fig. 2.3.12 Setting of Serial I/O mode

2. APPLICATION

2.3.4 Serial I/O application examples

(1) Output of serial data (control of a peripheral IC)

Outline : The port is connected to the $\overline{CS}$ pin of a peripheral IC and the serial transmission is controlled.

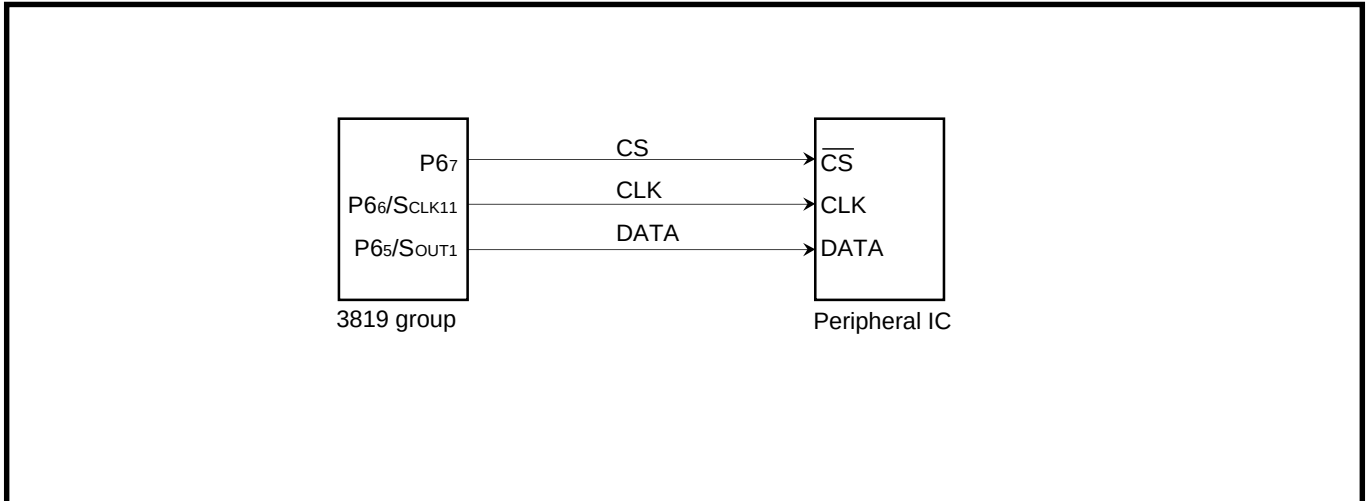


Fig. 2.3.13 Connection diagram [Output of serial data]

- Specifications :**
- The Serial I/O 1 is used (the automatic transfer function is not used)
 - Synchronous clock frequency: 131 kHz ($f(XIN) = 4.19 \text{ MHz}$ is divided by 32)
 - Transmission direction: LSB first
 - The Serial I/O 1 interrupt is not used.
 - The Port P67 is connected to the $\overline{CS}$ pin ("L" active) of the peripheral IC for a transmission control (the output level of the port P67 is controlled by software).

Figure 2.3.14 shows an output timing chart of serial data.

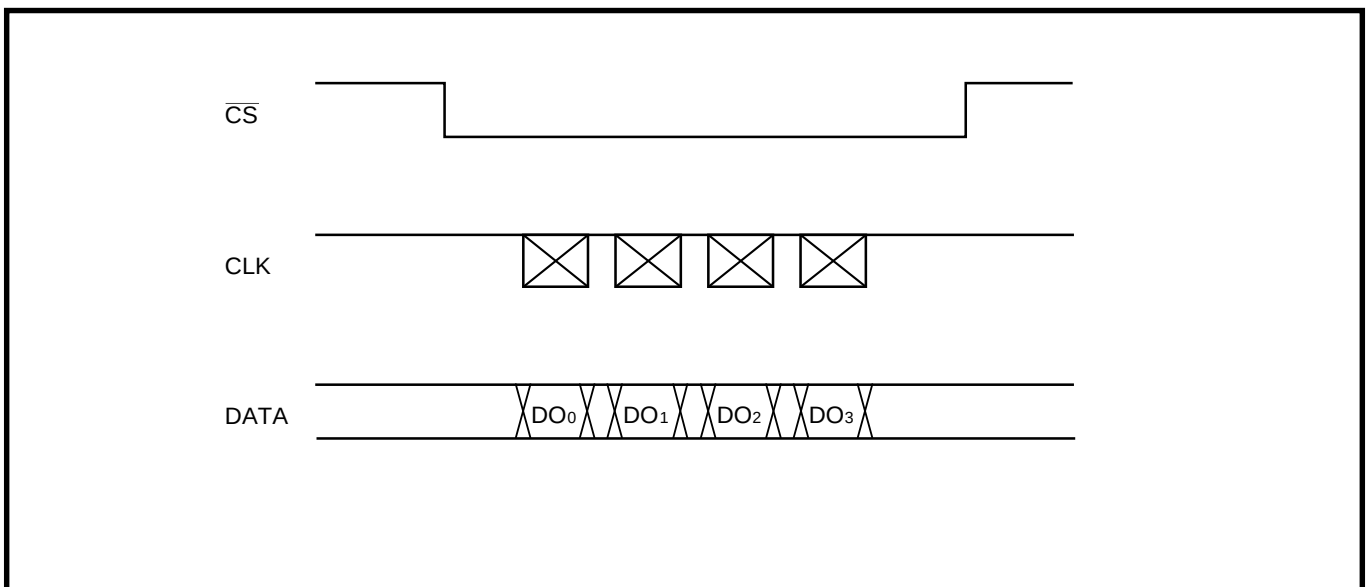


Fig. 2.3.14 Timing chart [Output of serial data]

2. APPLICATION

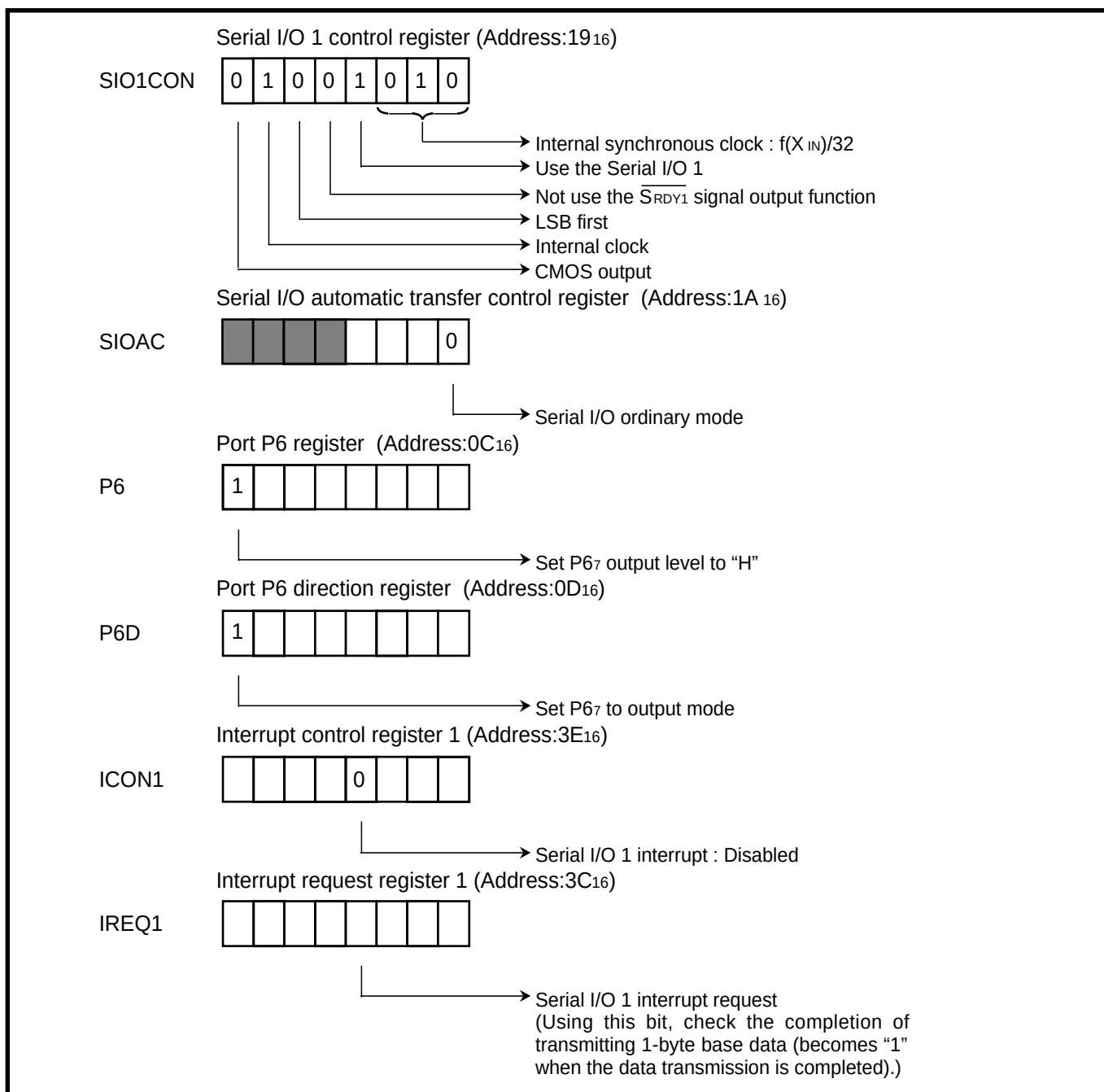


Fig. 2.3.15 Setting of related registers [Output of serial data]

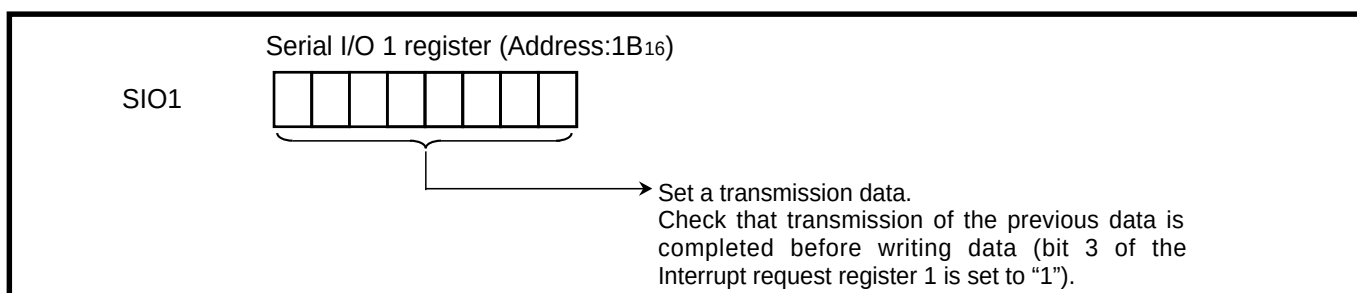


Fig. 2.3.16 Setting of transmission data [Output of serial data]

2. APPLICATION

Control procedure :When the registers are set as shown in Fig. 2.3.15, the Serial I/O 1 can transmit one-byte data simply by writing data to the Serial I/O 1 register.

Thus, after setting the CS signal to "L", write the transmission data to the Serial I/O 1 register and return the CS signal to "H" when the desired number of bytes have been transmitted.

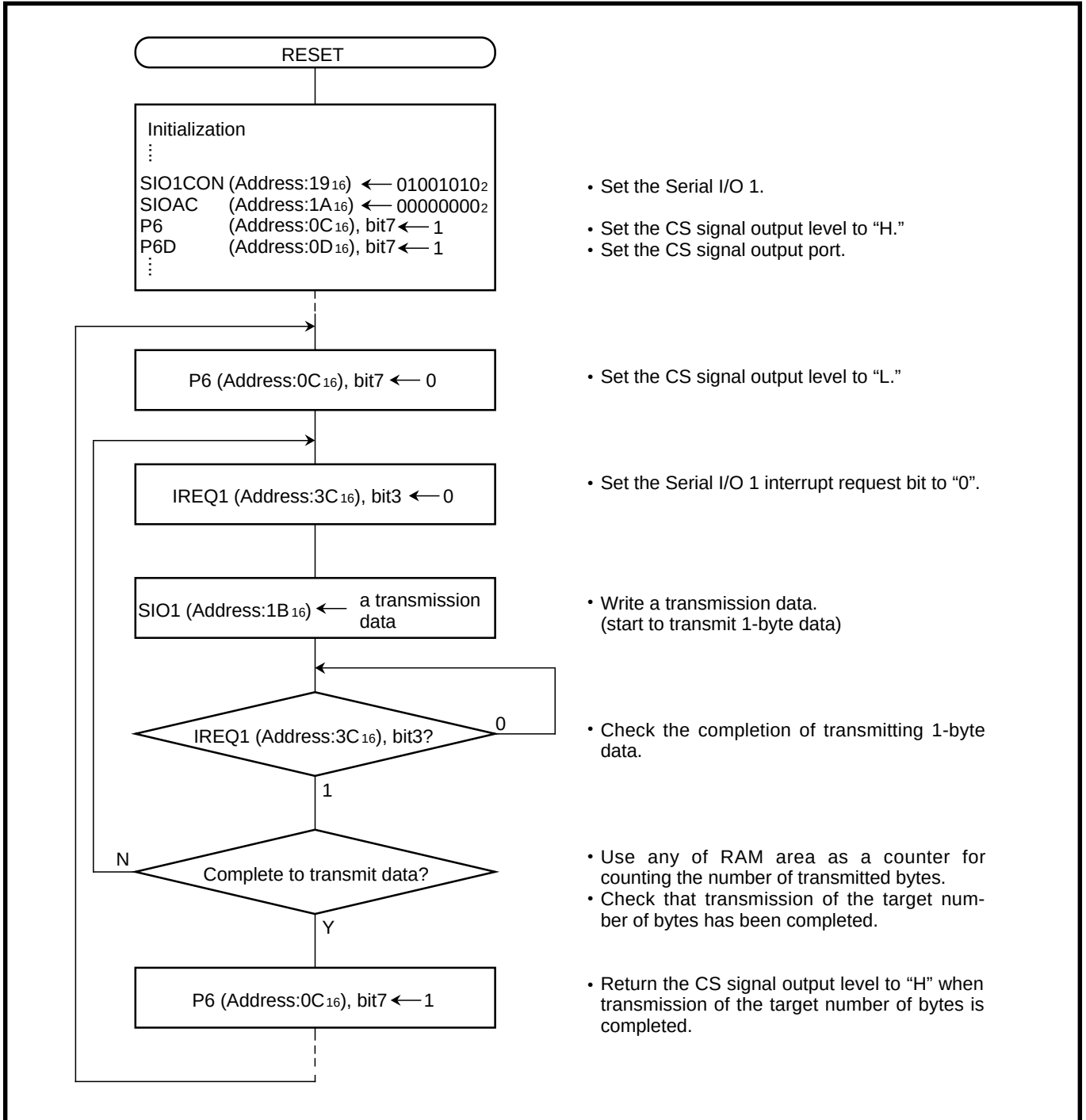


Fig. 2.3.17 Control procedure [Output of serial data]

2. APPLICATION

(2) Data transmission or reception using automatic transfer

Outline : Serial transmission or reception is controlled by using a serial automatic transfer function.

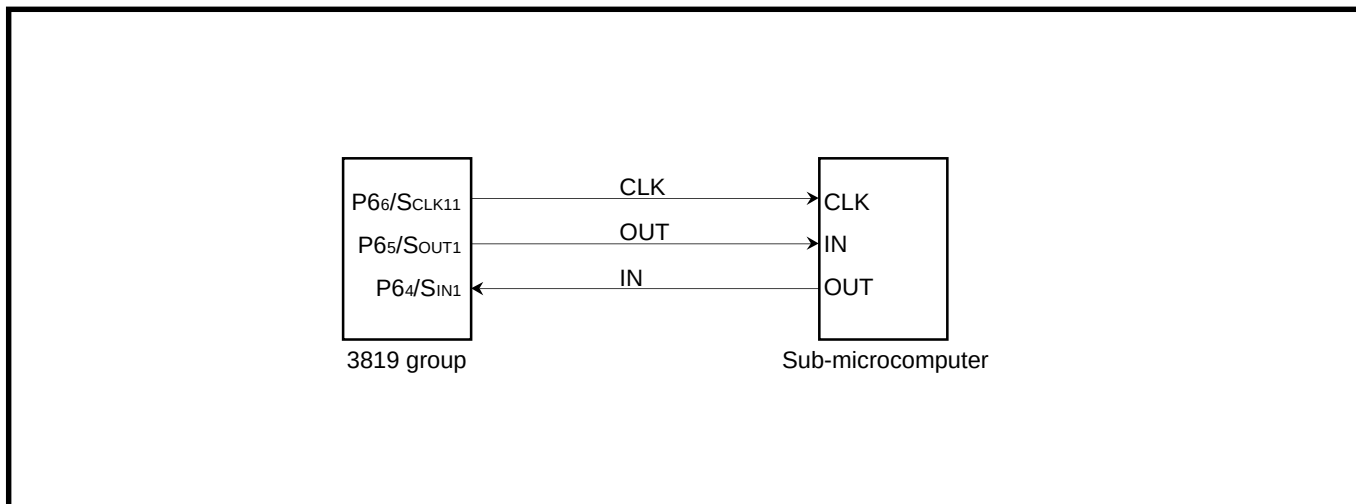


Fig. 2.3.18 Connection diagram [Data transmission or reception using automatic transfer]

- Specifications :**
- The Serial I/O 1 is used (the automatic transfer function is used).
 - Transmission clock frequency: 131 kHz ($f(X_{IN}) = 4.19 \text{ MHz}$ is divided by 32)
 - Transmission direction : LSB first
 - Number of bytes for transmission or reception : each 8 bytes/block
 - Transmission interval: 244 μs (corresponding to a transmission clock of 32 bits)
 - The Serial I/O automatic transfer interrupt is not used.

Figure 2.3.19 shows a transmission or reception timing chart using an automatic transfer.

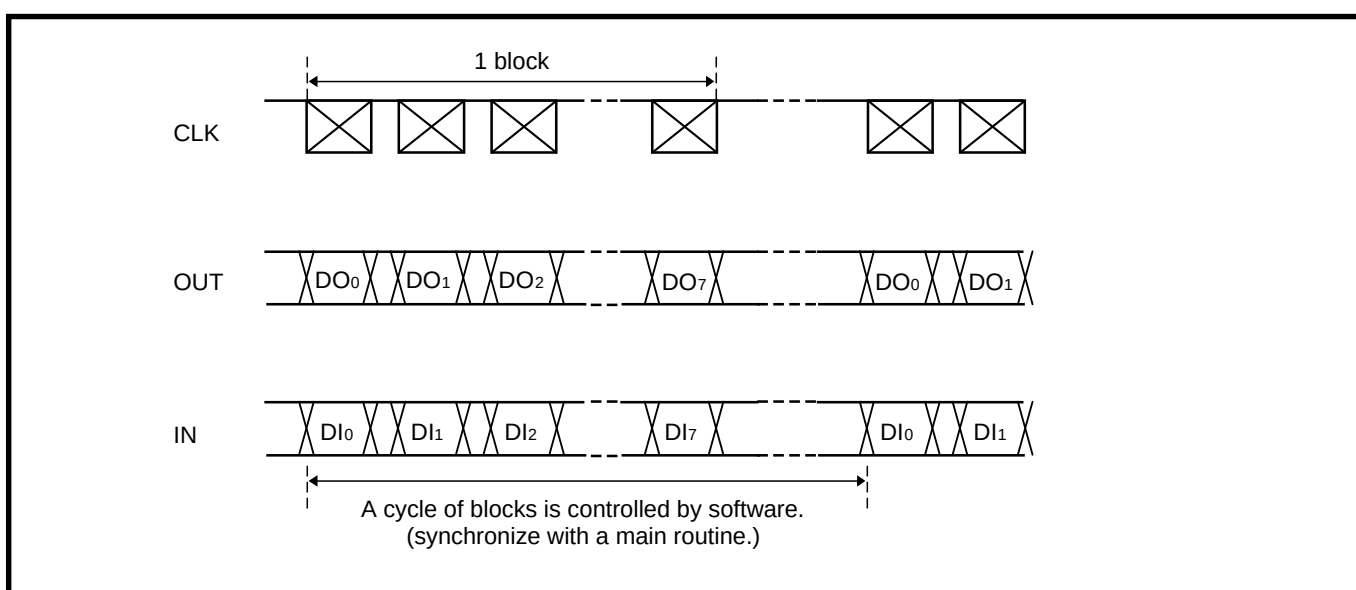


Fig. 2.3.19 Timing chart [Data transmission or reception using automatic transfer]

2. APPLICATION

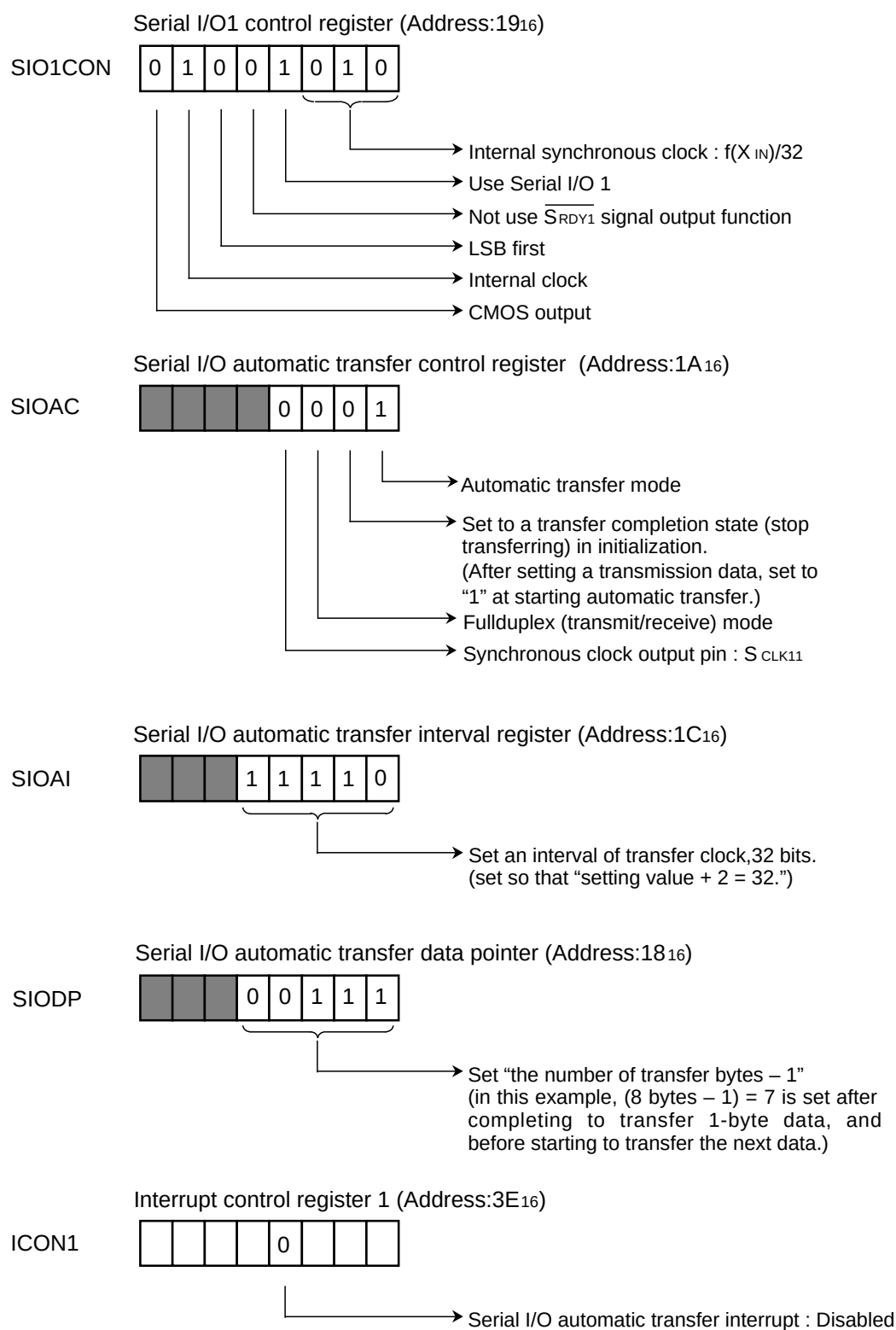


Fig. 2.3.20 Setting of related registers [Data transmission or reception using automatic transfer]

2. APPLICATION

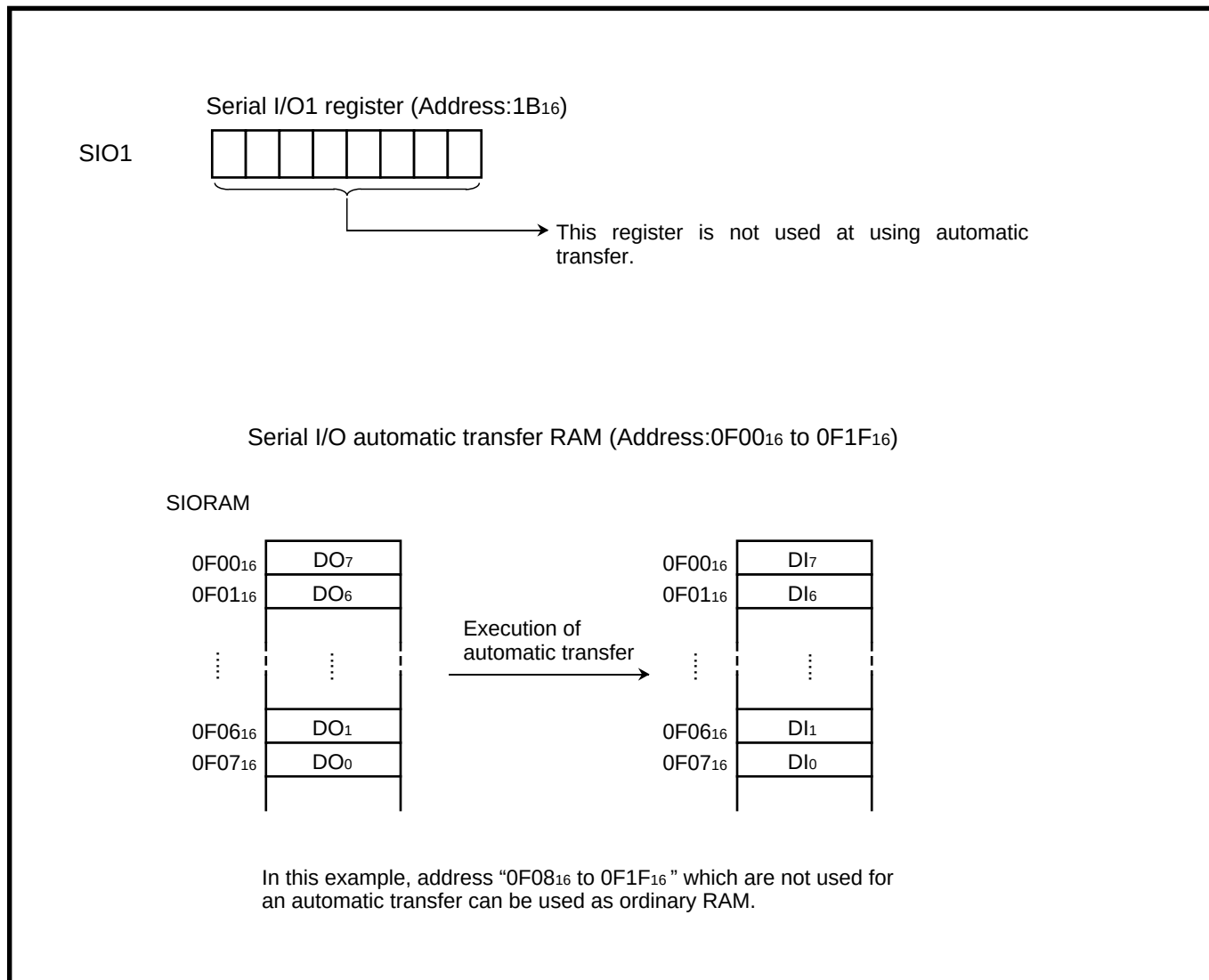


Fig. 2.3.21 Setting of transmission data [Data transmission or reception using automatic transfer]

2. APPLICATION

Control procedure : In this example, a serial communication is performed at the beginning of the main routine which loops in a certain cycle.

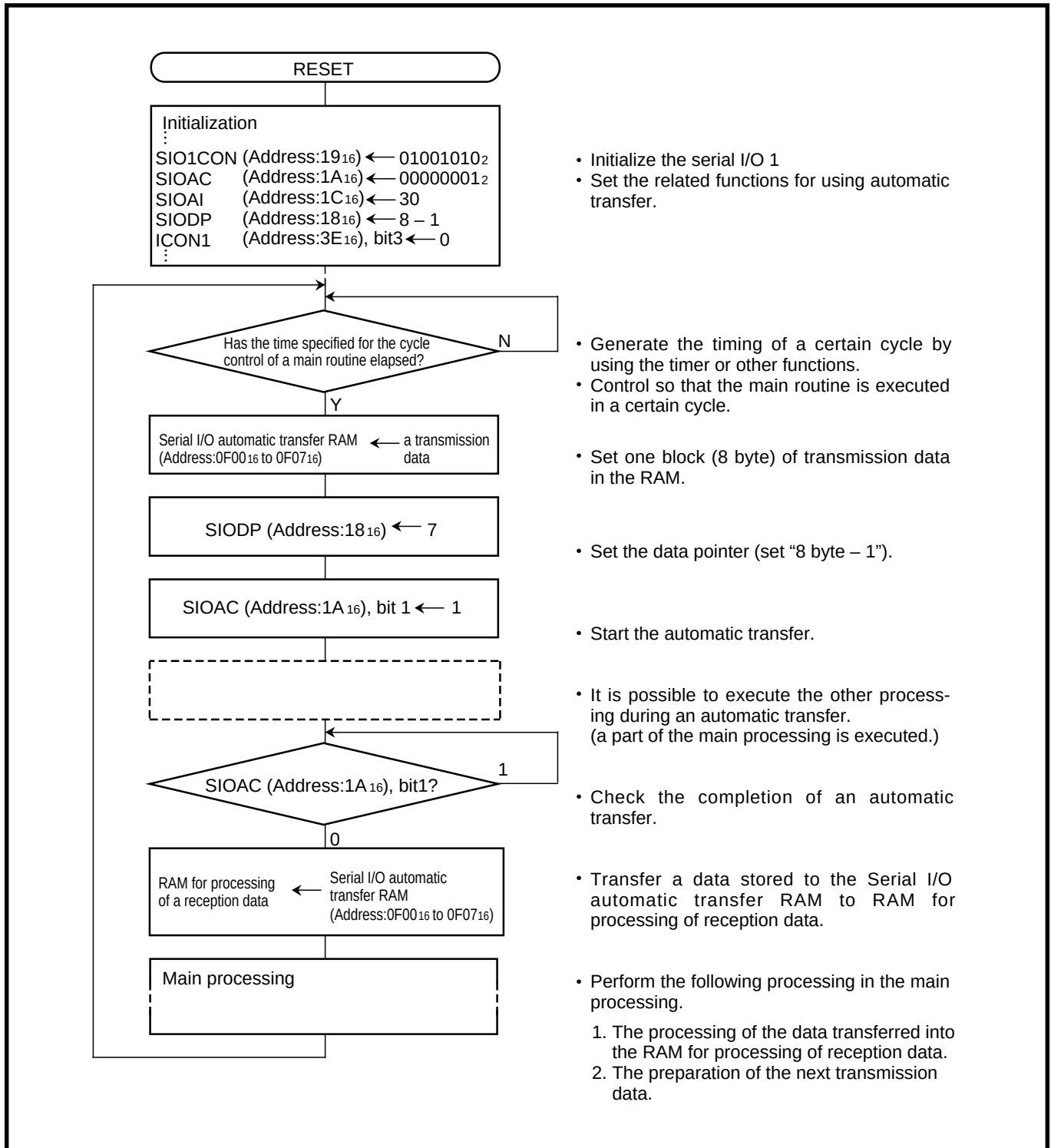


Fig. 2.3.22 Control procedure [Data transmission or reception using automatic transfer]

2. APPLICATION

(3) Cyclic transmission or reception of block data (data of a specified number of bytes) between microcomputers [without using an automatic transfer]

Outline : When a clock synchronous serial I/O is used for communication, synchronization of the clock and the data between the transmitter and receiver sides may be lost because of noise included in the synchronizing clock. Thus, it is necessary to be corrected constantly. This “heading adjustment” is carried out by using the interval between blocks in this example.

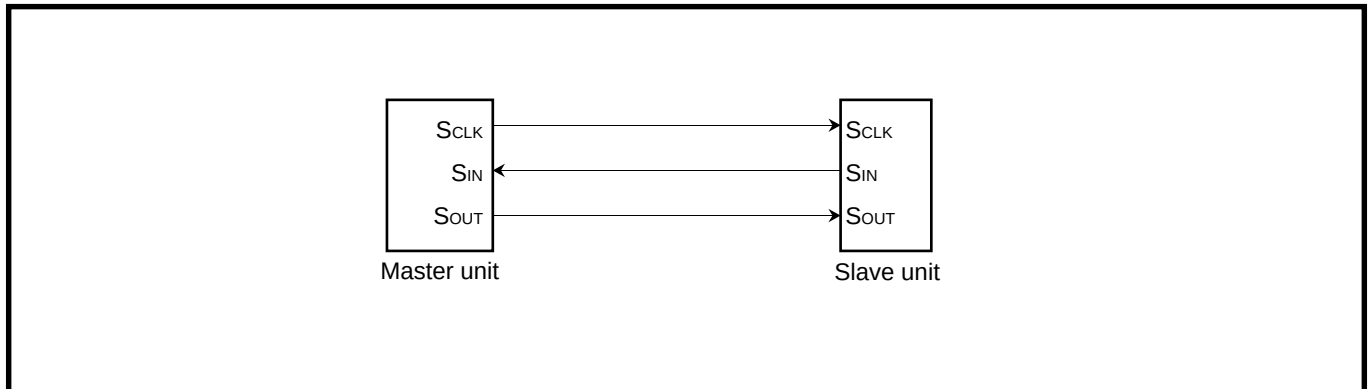


Fig. 2.3.23 Connection diagram [Cyclic transmission or reception of block data between microcomputers]

- Specifications :**
- Synchronous clock frequency : 131 kHz ($f(X_{IN}) = 4.19 \text{ MHz}$ is divided by 32)
 - Byte cycle : 488 μs
 - Number of bytes for transmission or reception : each 8 byte/block
 - Block transmission cycle : 16 ms
 - Block transmission period : 3.5 ms
 - Interval between blocks : 12.5 ms
 - Heading adjustive time : 8 ms
 - Transmission direction : LSB first

Limitations of the specifications

1. Reading of the reception data and setting of the next transmission data must be completed within the time obtained from “byte cycle – time for transmitting 1-byte data” (in this example, the time taken from generating of the Serial I/O 1 interrupt request to generating of the next synchronizing clock is 431 μs).
2. “Heading adjustive time < interval between blocks” must be satisfied.
3. Although the transmission direction can be switched for the Serial I/O of 3819 group, it cannot be switched for some serial I/Os of 740 family including 38000 series (only LSB first). Be sure to check when deciding specifications.

2. APPLICATION

The communication is performed according to the timing shown below. In the slave unit, when a synchronizing clock is not input within a certain time (heading adjustive time), the next clock input is processed as the beginning (heading) of a block.

When a clock is input again after one block (8 byte) is received, the clock is ignored.

Figure 2.3.25 shows a setting of related registers.

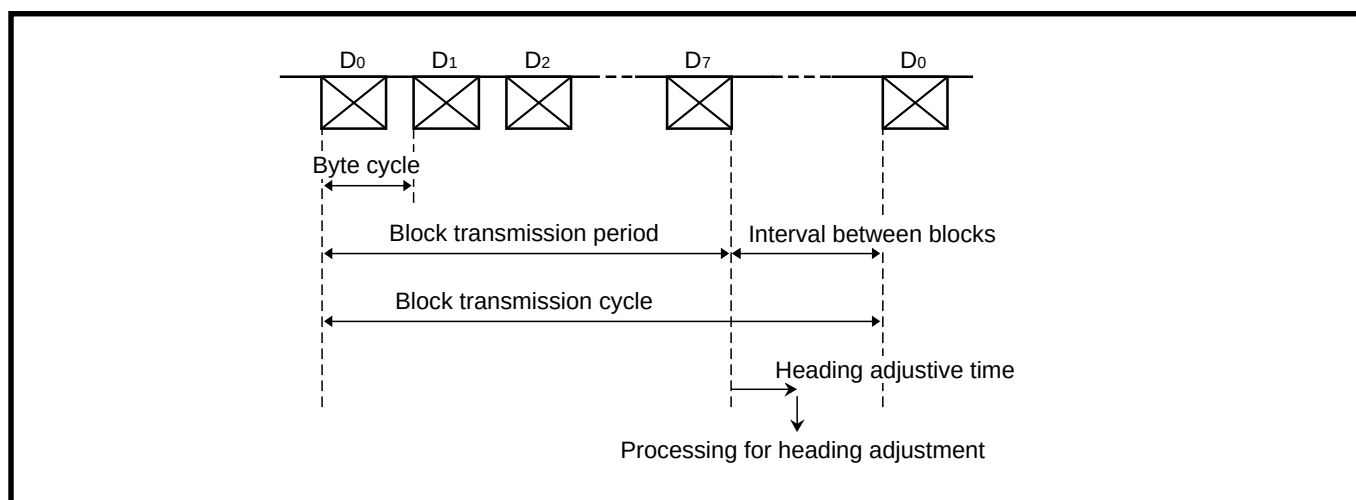


Fig. 2.3.24 Timing chart [Cyclic transmission or reception of block data between microcomputers]

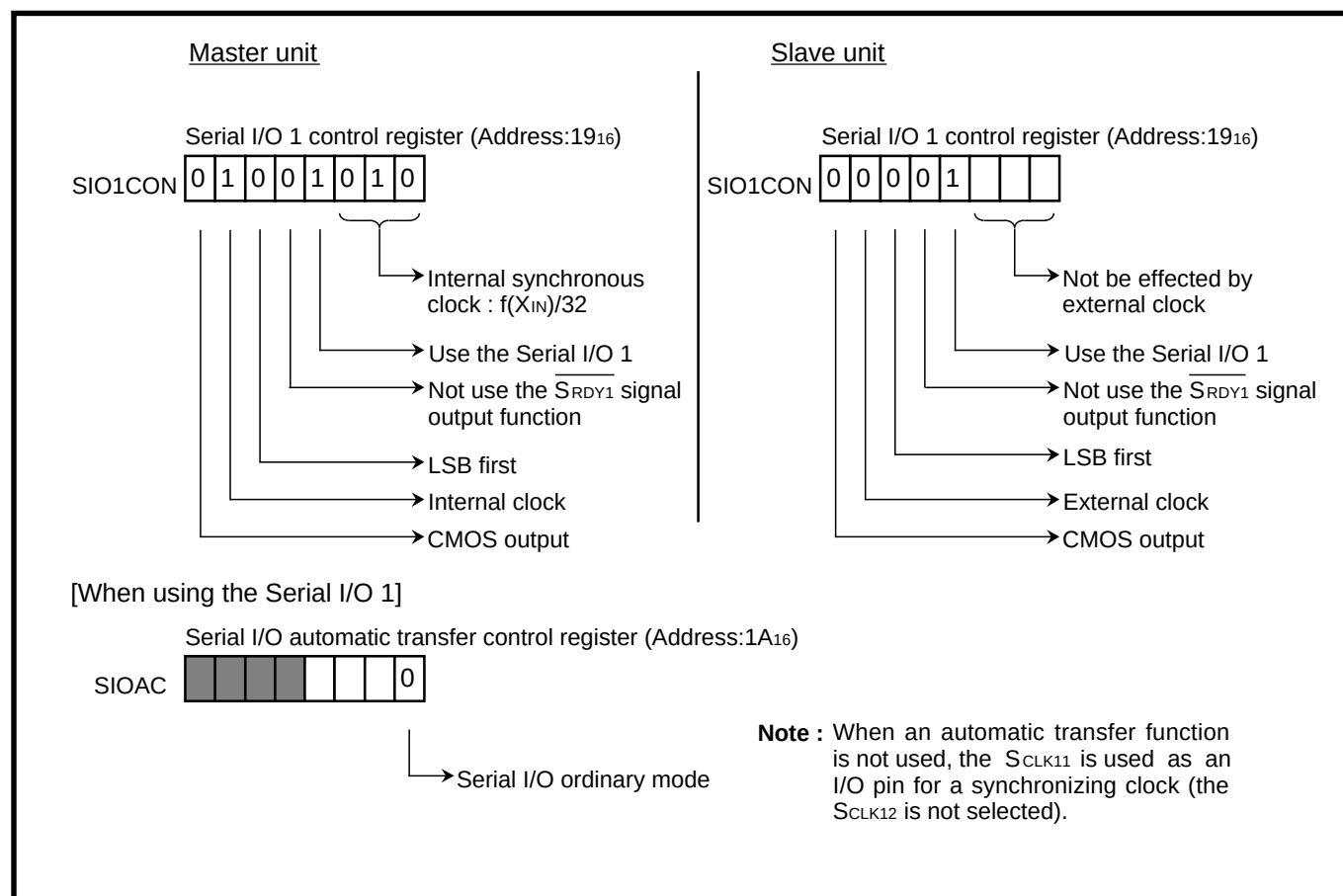


Fig. 2.3.25 Setting of related registers [Cyclic transmission or reception of block data between microcomputers]

2. APPLICATION

Control procedure :

(1) Control in the master unit

After a setting of the related registers is completed as shown in Figure 2.3.25, in the master unit transmission or reception of one-byte data is started simply by writing transmission data to the Serial I/O 1 register.

To perform the communication in the timing shown in the specifications, therefore, take the timing into account and write transmission data. Read out the reception data when the Serial I/O 1 interrupt request bit is set to "1", or before the next transmission data is written to the Serial I/O 1 register.

A processing example in the master unit using timer interrupts is shown below.

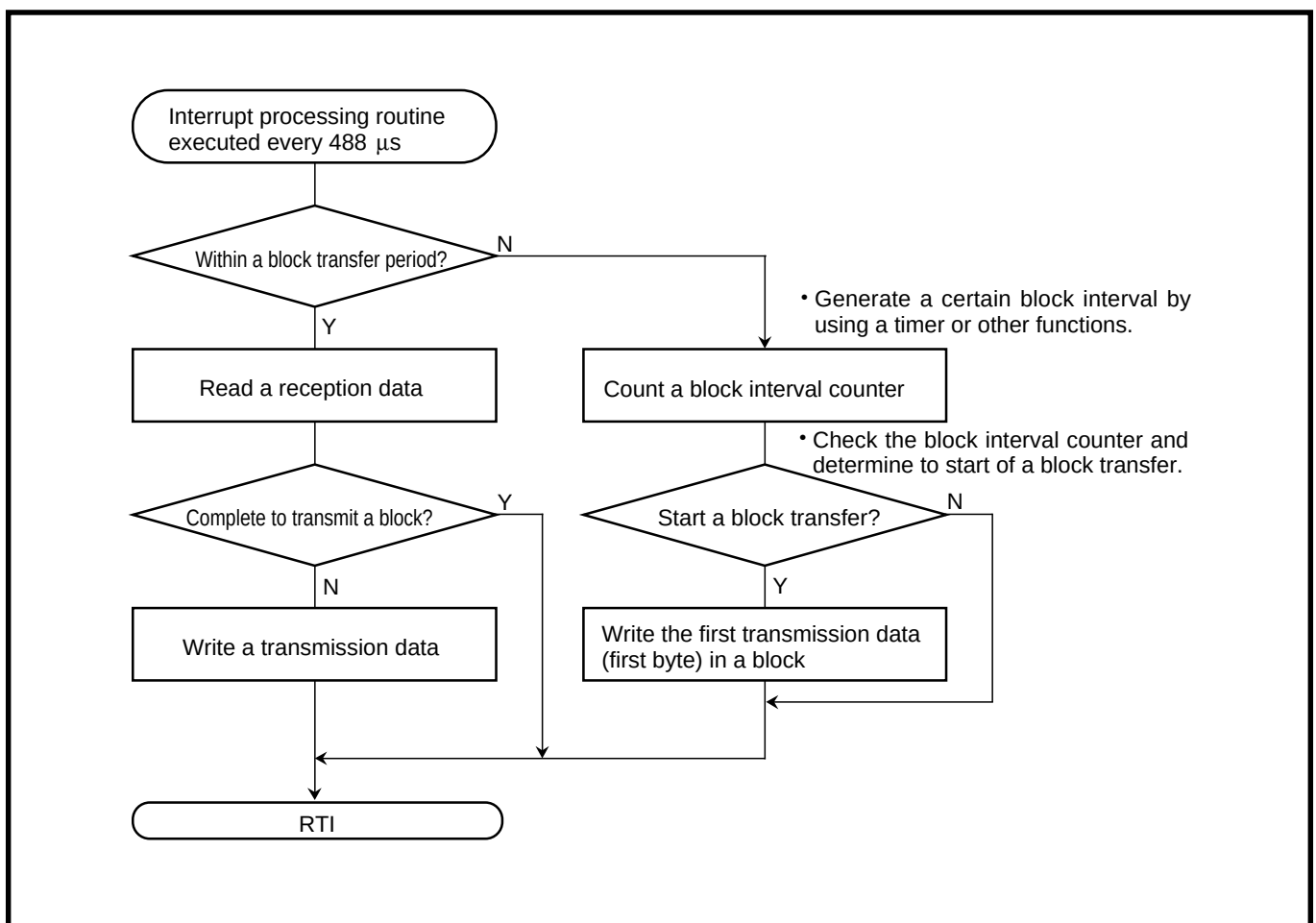


Fig. 2.3.26 Control in the master unit

2. APPLICATION

(2) Control in the slave unit

After a setting of the related registers is completed as shown in Figure 2.3.25, the slave unit becomes the state which is received a synchronizing clock at all times, and the Serial I/O 1 interrupt request bit is set to "1" every time an 8-bit synchronous clock is received.

For transmitting or receiving data according to the synchronizing clock input in the timing shown in the specifications, read out the reception data and write the next transmission data to the Serial I/O 1 register in the following conditions.

- When the Serial I/O 1 interrupt occurs.
- When the Serial I/O 1 interrupt request bit is set to "1" as the result of checking.

When the Serial I/O 1 interrupt request bit is not set to "1" within a certain time (heading adjustive time), the first byte of the transmission data in a block is written to the Serial I/O 1 register, then the next reception data is processed as the first byte of the reception data in a block. A processing example in the slave unit using serial I/O interrupts and timer interrupts (for a heading adjustment) is shown below.

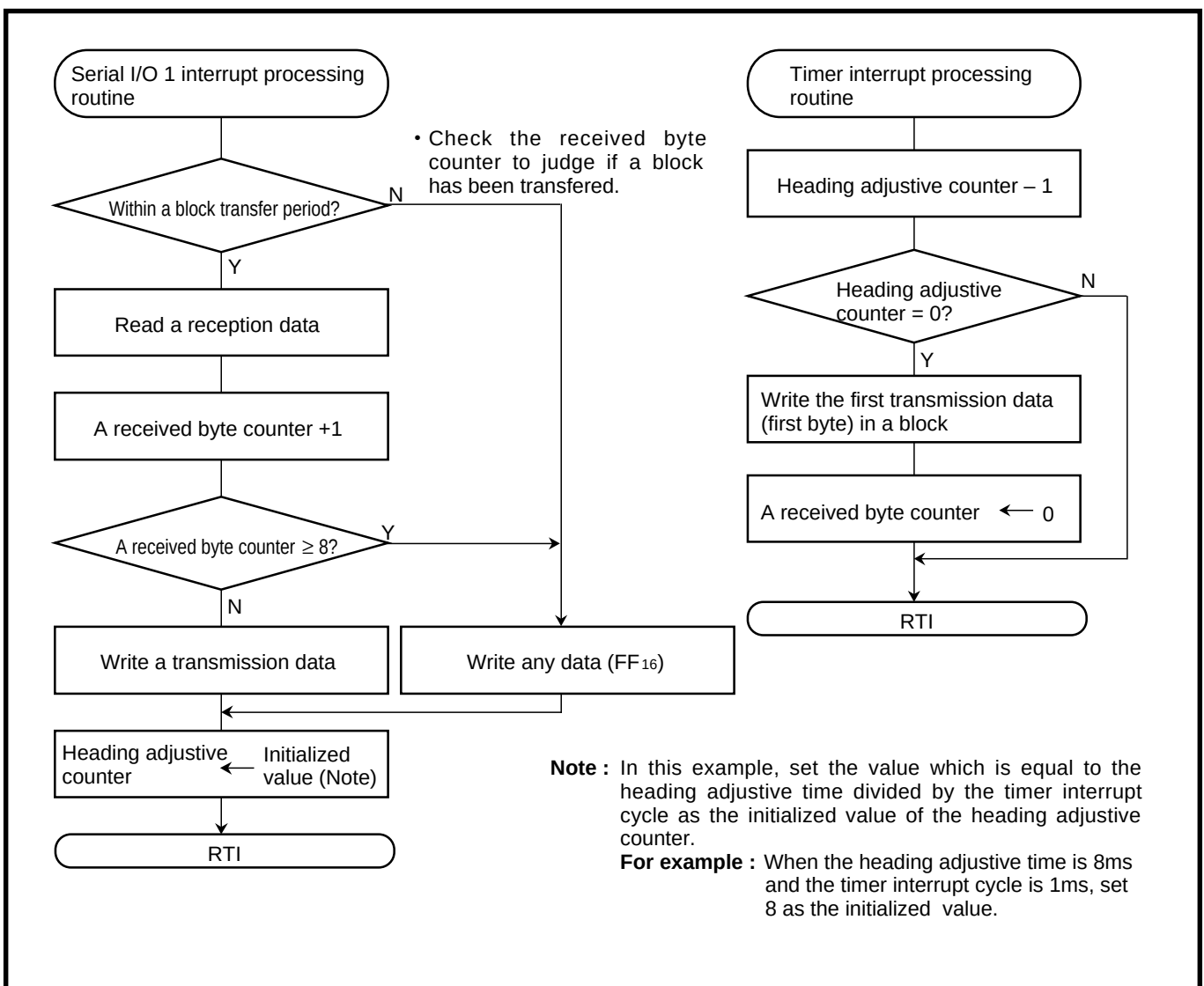


Fig. 2.3.27 Control in the slave unit

2. APPLICATION

2.4 A-D conversion

2.4.1 Related registers

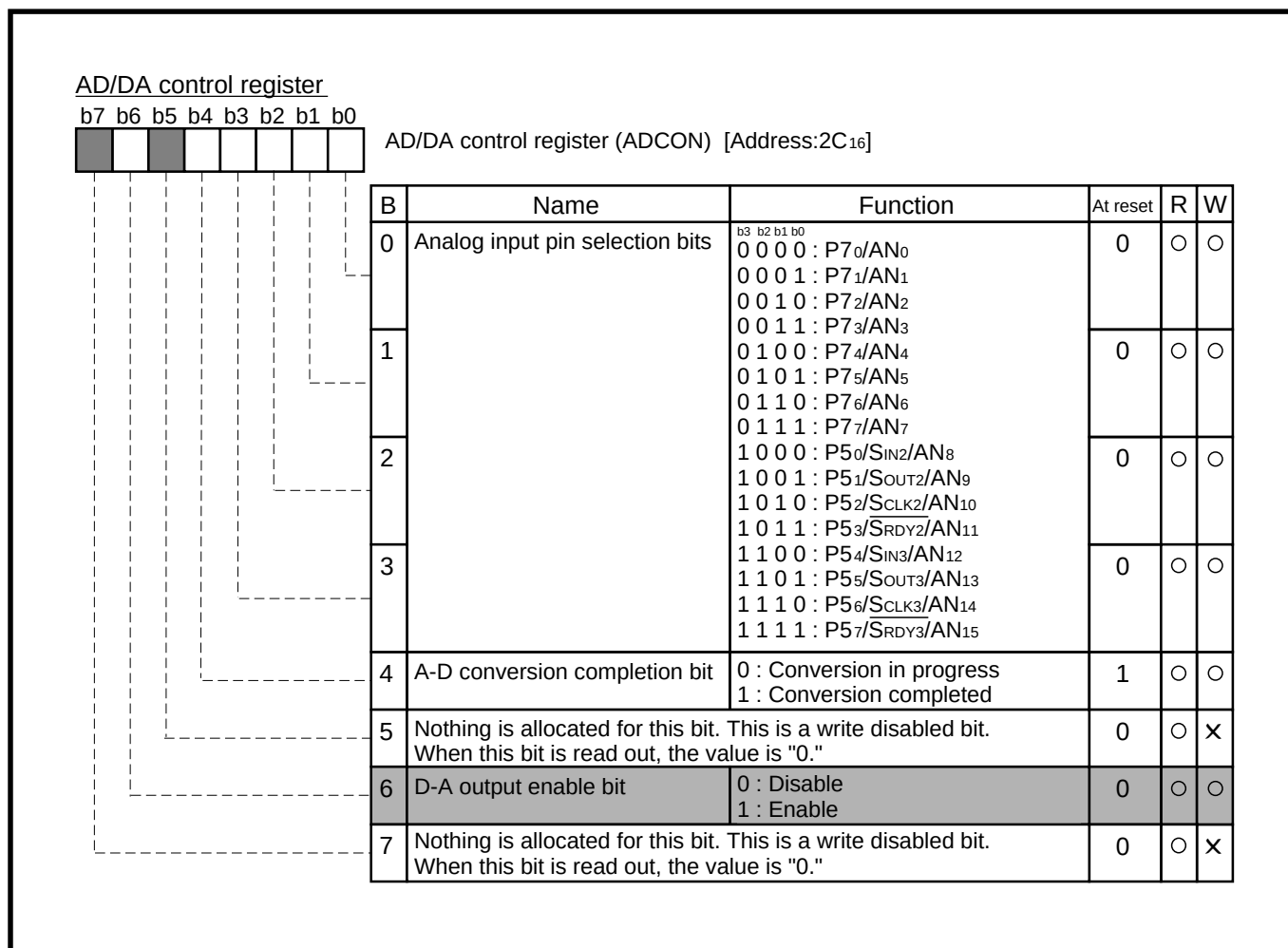


Fig. 2.4.1 Structure of AD/DA control register

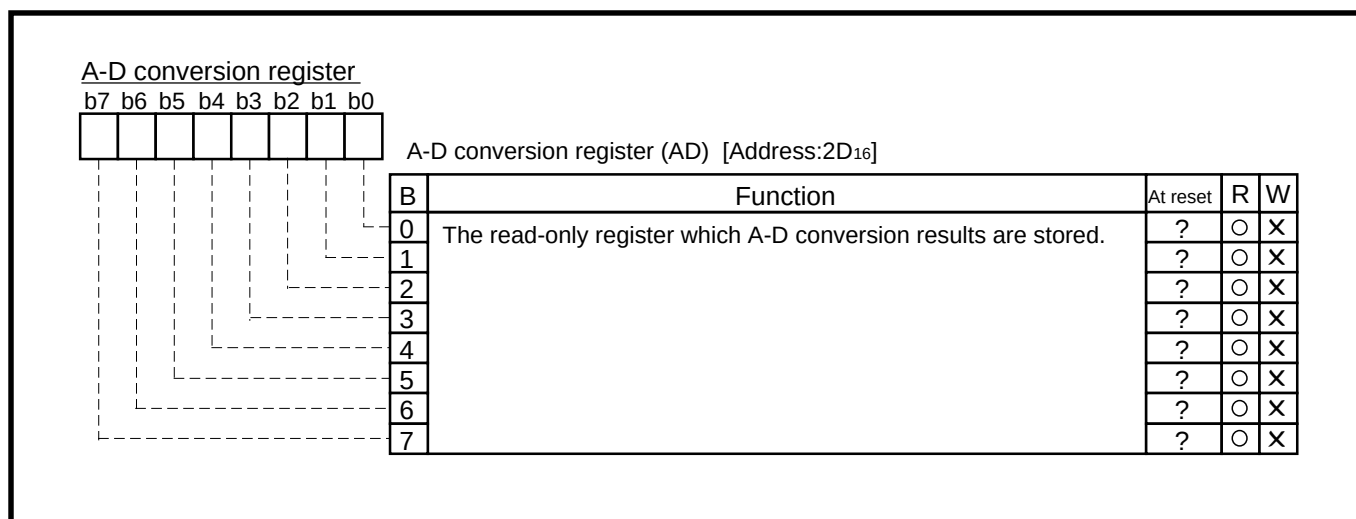


Fig. 2.4.2 Structure of A-D conversion register

2. APPLICATION

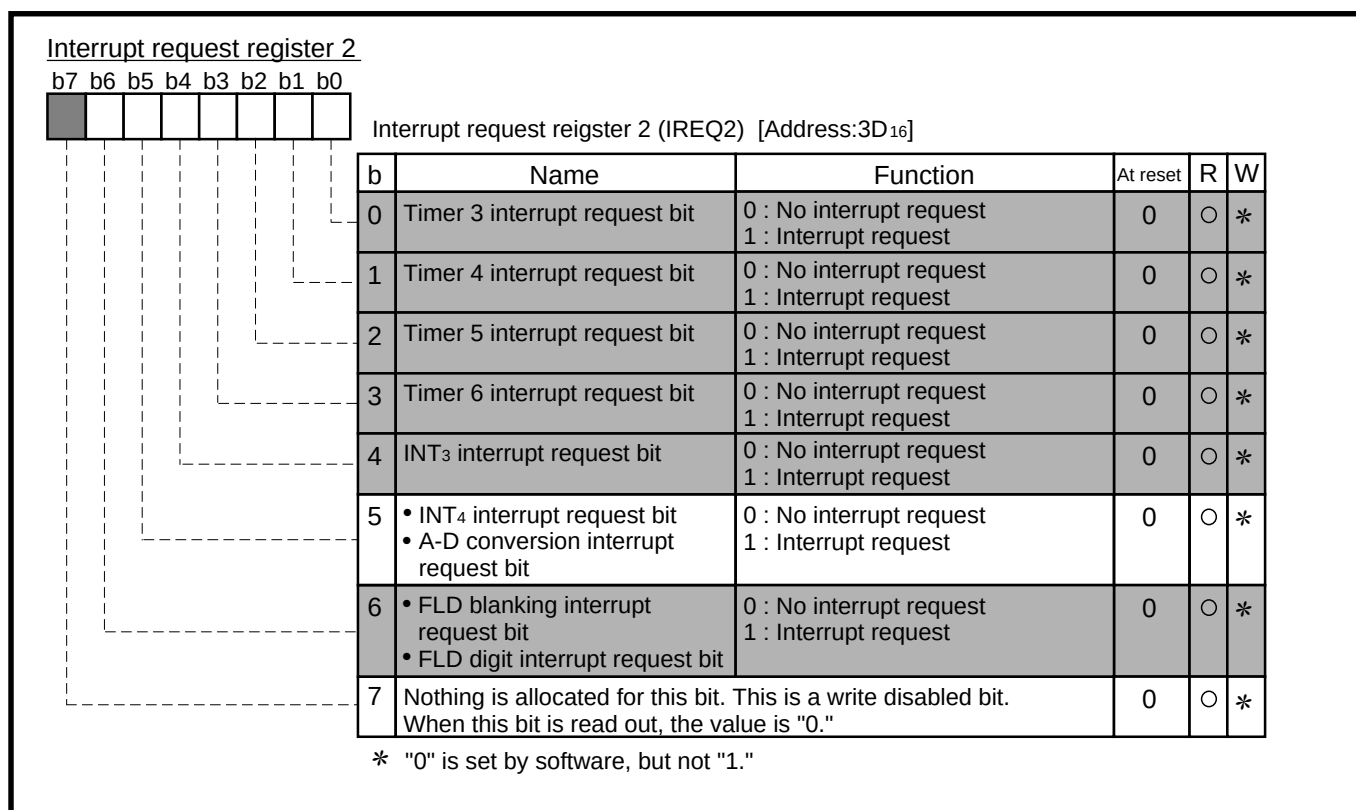


Fig. 2.4.3 Structure of Interrupt request register 2

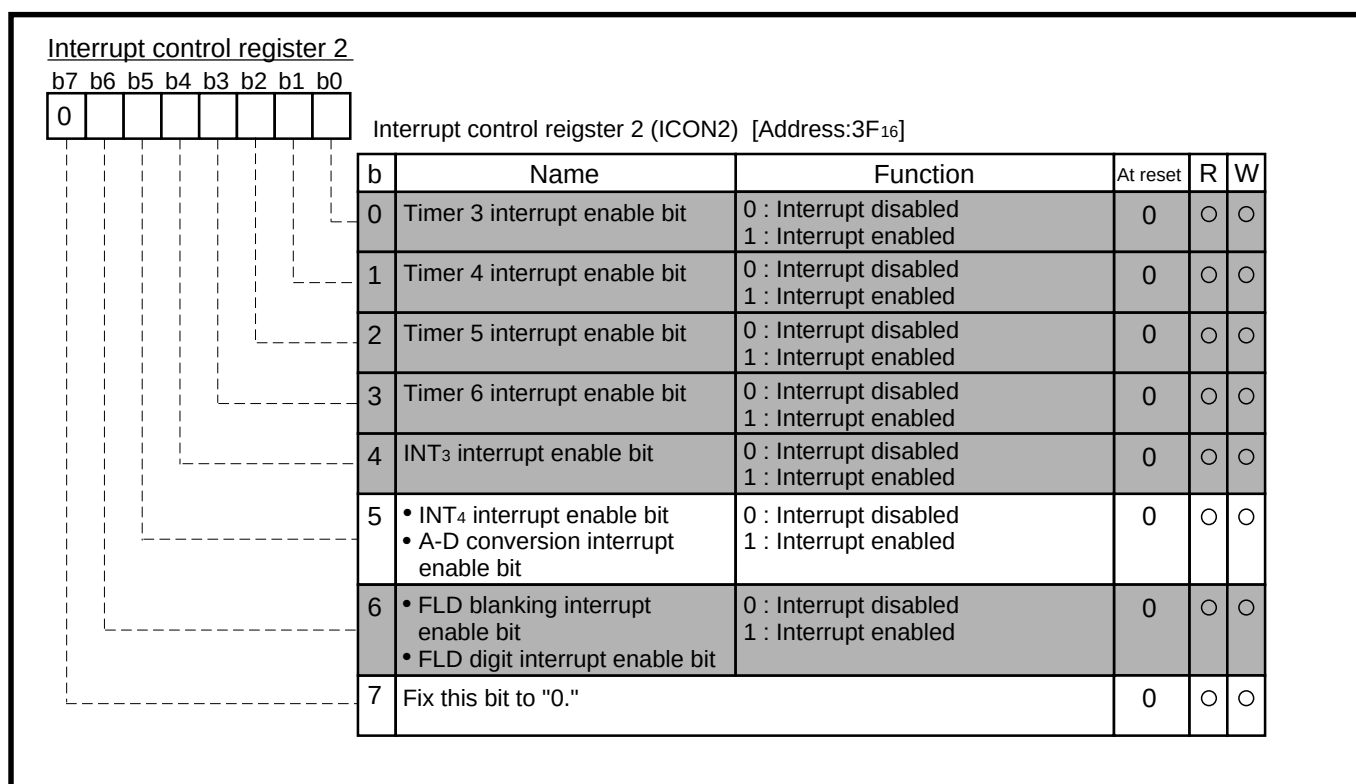


Fig. 2.4.4 Structure of Interrupt control register 2

2. APPLICATION

2.4.2 A-D conversion application example

Conversion of Analog input voltage

Outline : The analog input voltage input from the sensor is converted into digital values.

Figure 2.4.5 shows a connection diagram, and Figure 2.4.6 shows a setting of related registers.

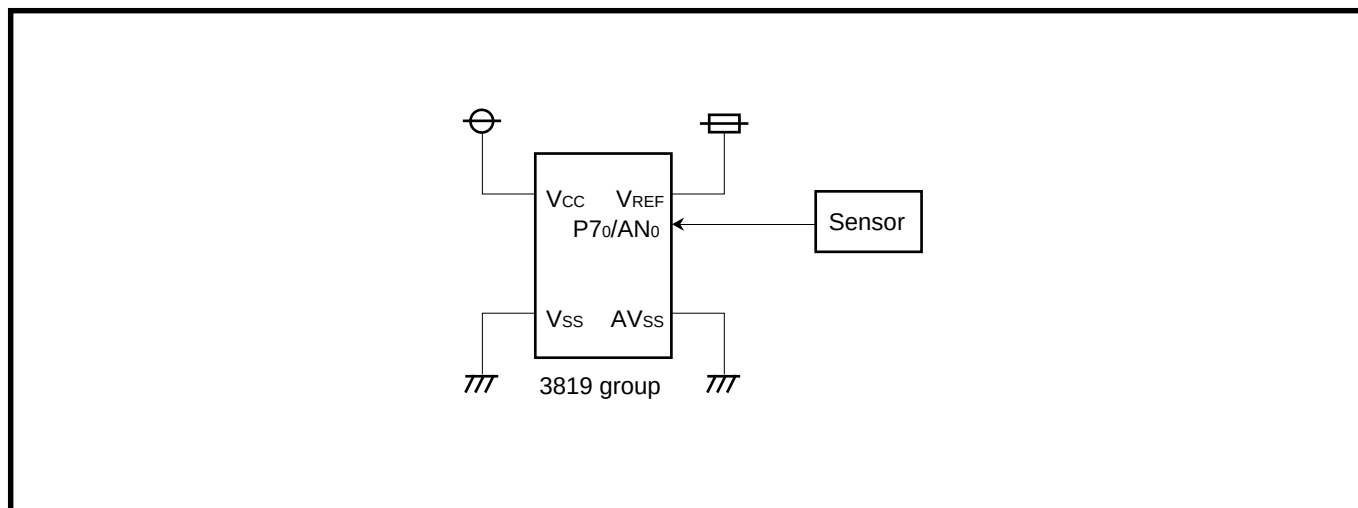


Fig. 2.4.5 Connection diagram [Conversion of Analog input voltage]

- Specifications :**
- The AN0 pin is used as an analog input pin.
 - The analog input voltage input from the sensor is converted into digital values.

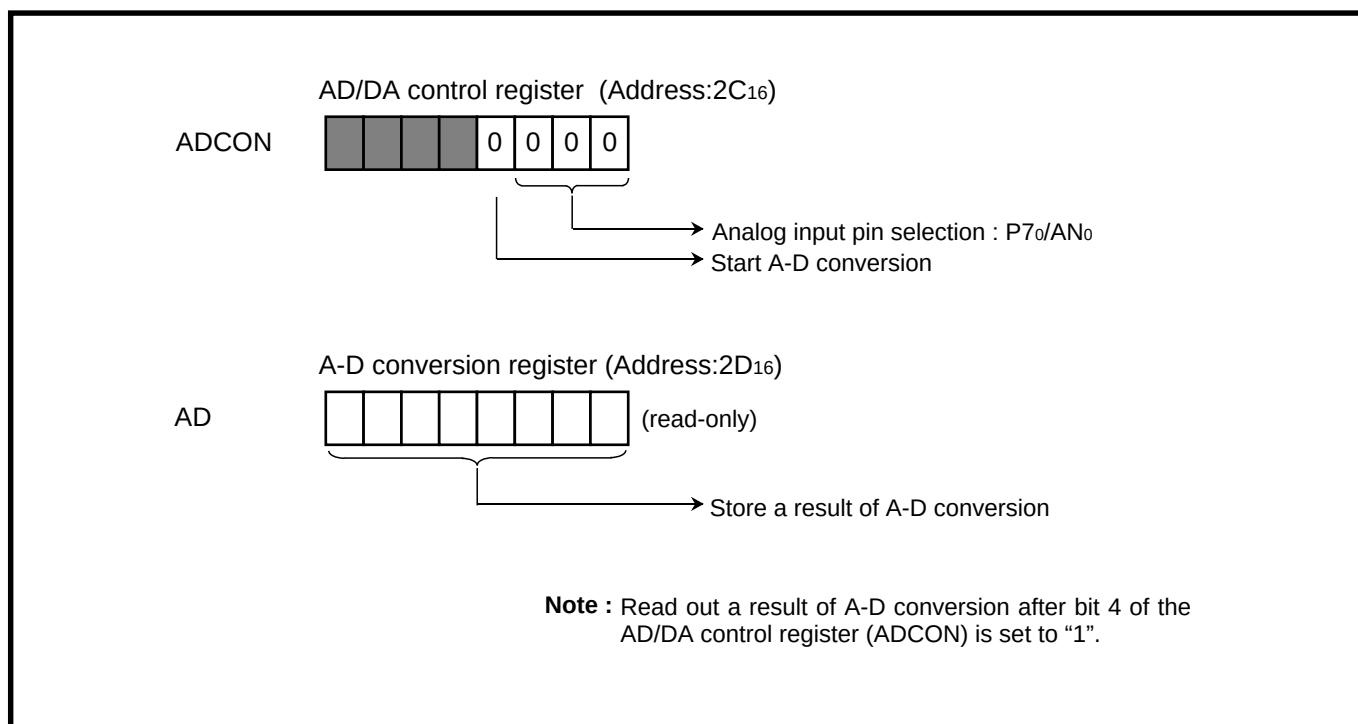


Fig. 2.4.6 Setting of related registers [Conversion of Analog input voltage]

2. APPLICATION

Control procedure : By setting the related registers as shown in Figure 2.4.6, the analog input voltage input from the sensor are converted into digital values.

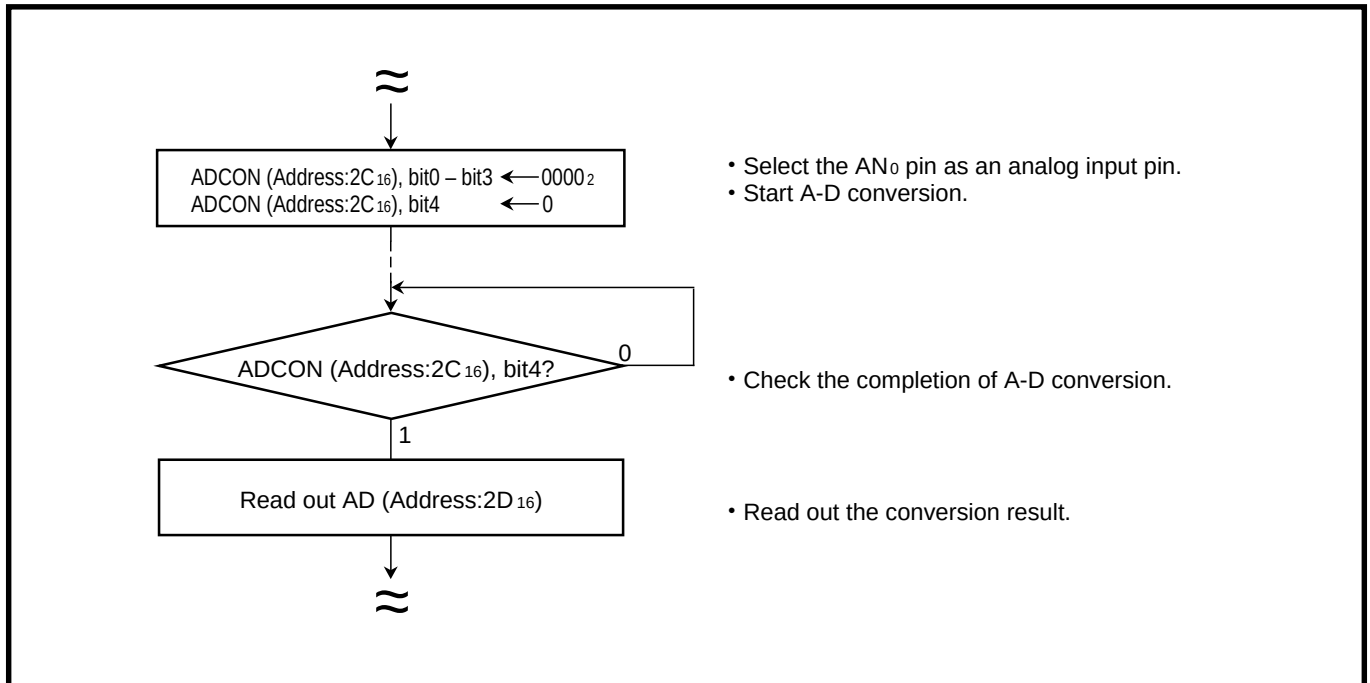


Fig. 2.4.7 Control procedure [Conversion of Analog input voltage]

3819 Group

2.5 FLD controller

2. APPLICATION

2.5 FLD controller

2.5.1 Related registers

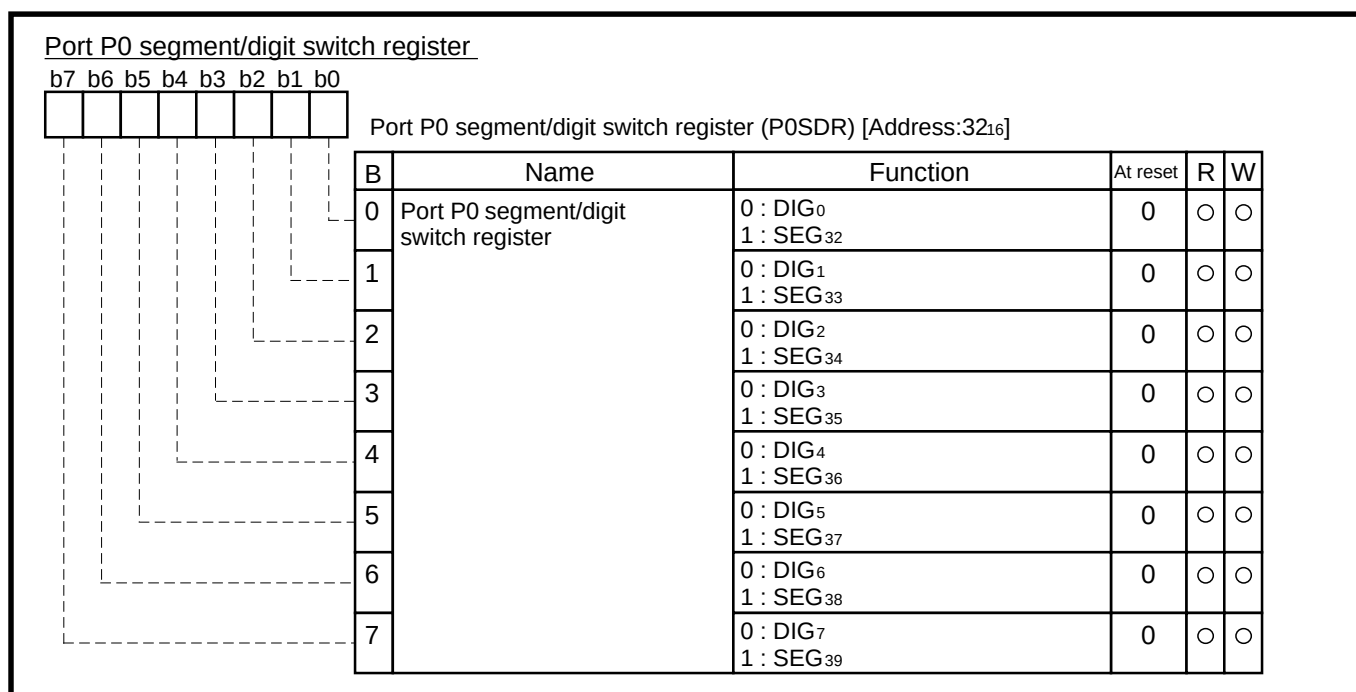


Fig. 2.5.1 Structure of Port P0 segment/digit switch register

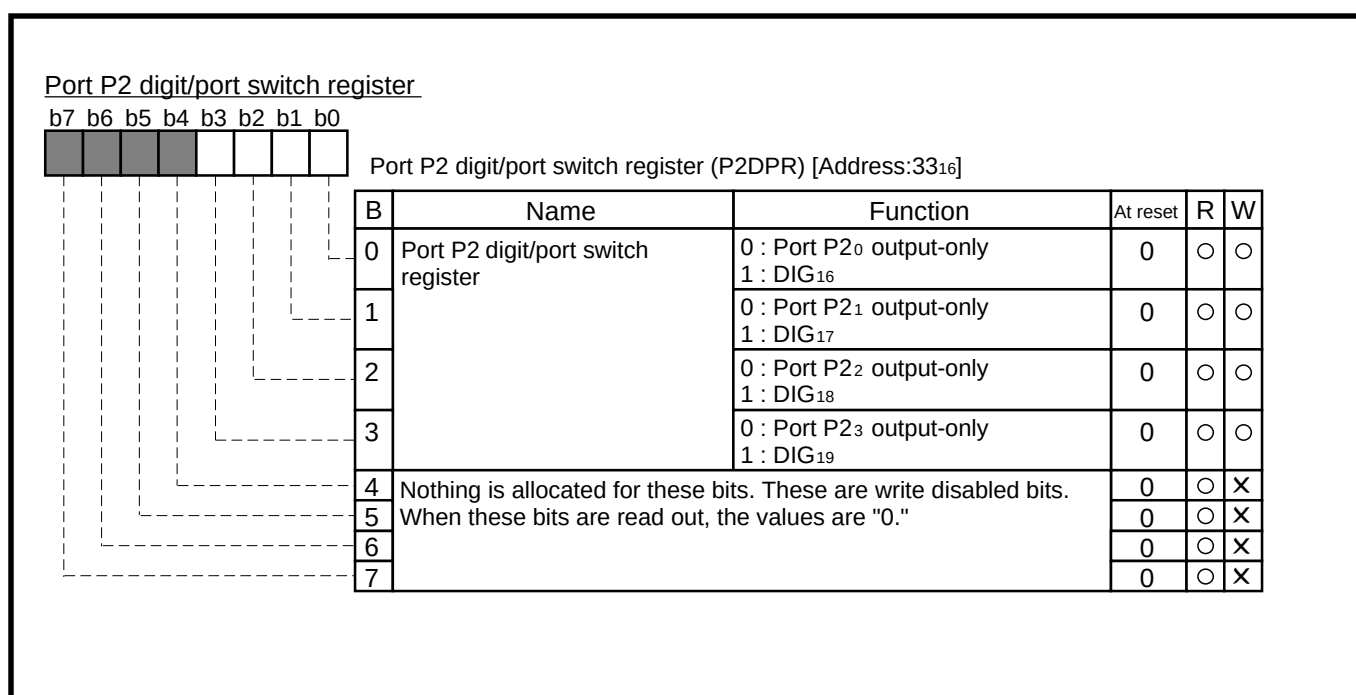


Fig. 2.5.2 Structure of Port P2 digit/port switch register

3819 Group 2.5 FLD controller

2. APPLICATION

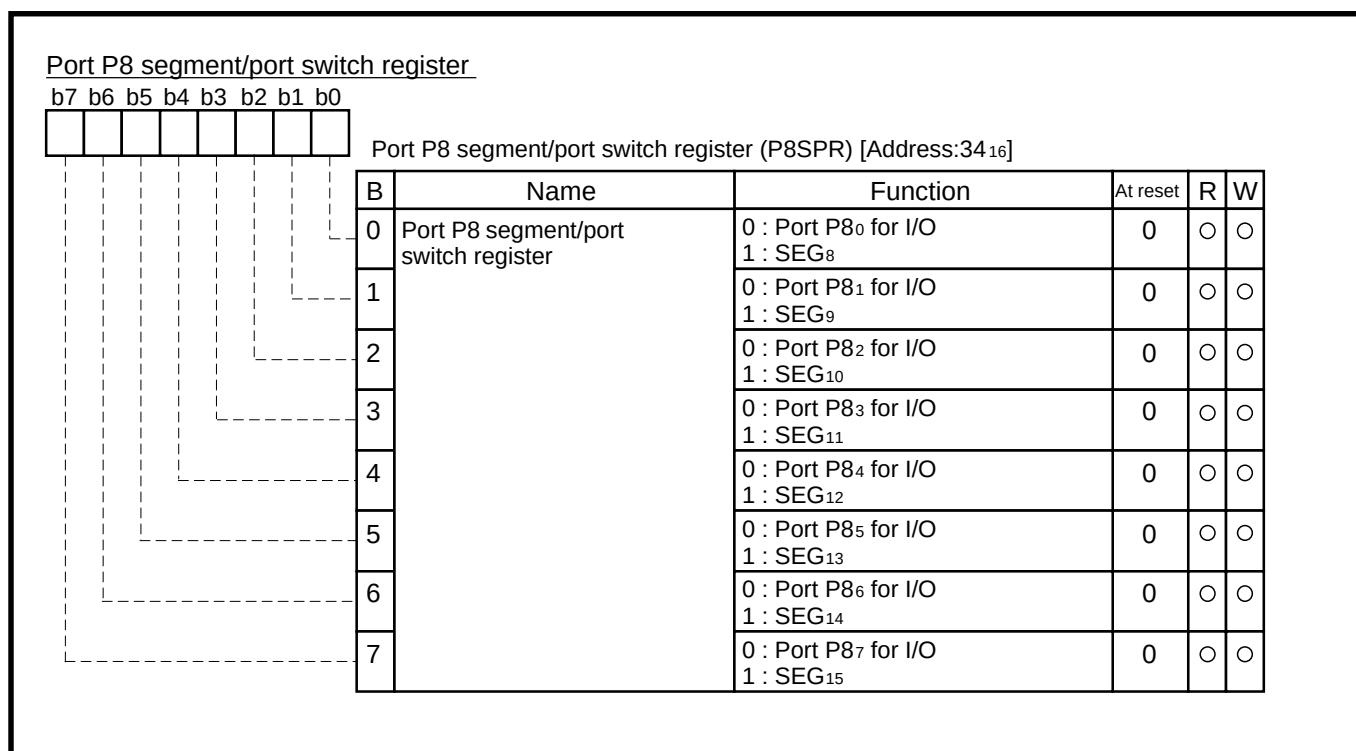


Fig. 2.5.3 Structure of Port P8 segment/port switch register

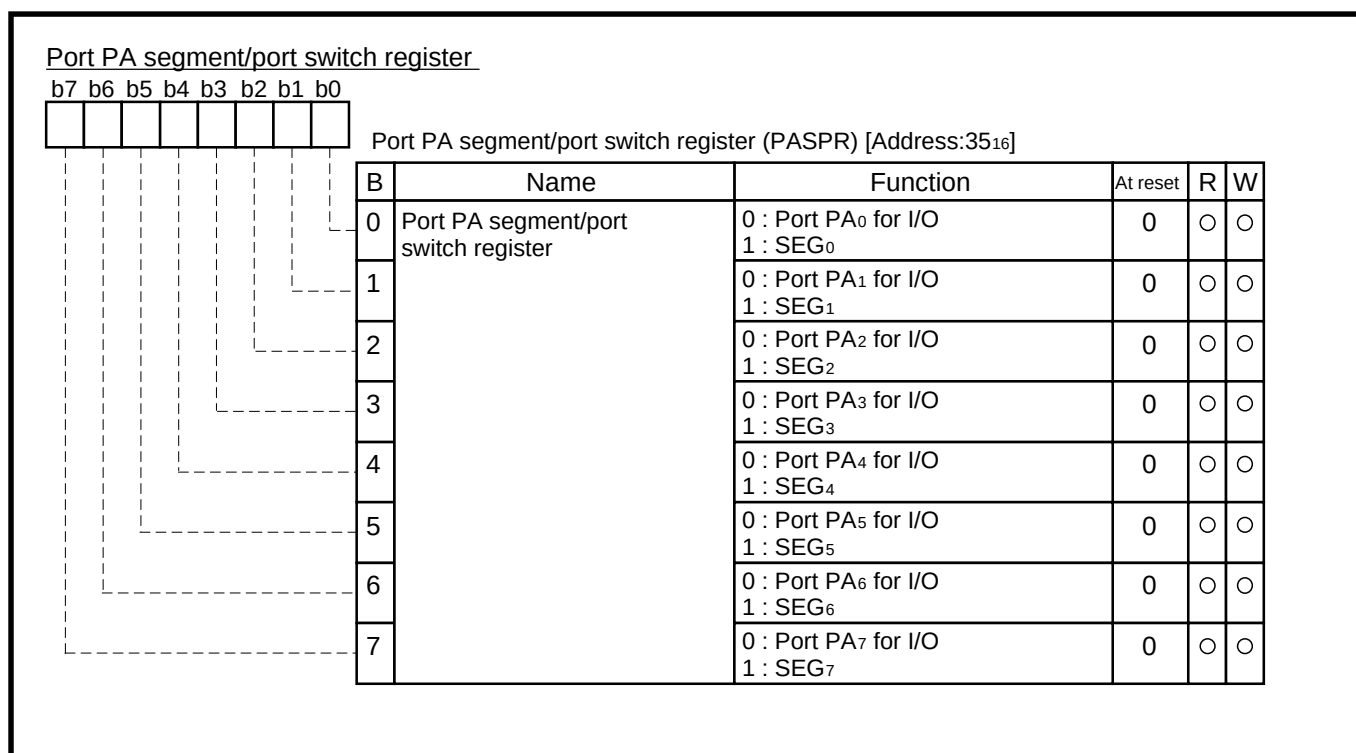


Fig. 2.5.4 Structure of Port PA segment/port switch register

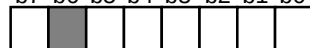
3819 Group

2.5 FLD controller

2. APPLICATION

FLDC mode register 1

b7 b6 b5 b4 b3 b2 b1 b0



FLDC mode register 1 (FLDM1) [Address:36₁₆]

B	Name	Function	At reset	R	W
0	Tscan control bits	b1b0 0 0 : FLD digit interrupt (at rising edge of each digit)	0	○	○
1		0 1 : 1 × Tdisp 1 0 : 2 × Tdisp 1 1 : 3 × Tdisp } FLD blanking interrupt (at falling edge of the last digit)	0	○	○
2	Toff control bit (Setting of digit/segment OFF time)	b5 b4 b3 b2 0 0 0 0 : 1/16 × Tdisp 0 0 0 1 : 2/16 × Tdisp 0 0 1 0 : 3/16 × Tdisp 0 0 1 1 : 4/16 × Tdisp 0 1 0 0 : 5/16 × Tdisp 0 1 0 1 : 6/16 × Tdisp 0 1 1 0 : 7/16 × Tdisp 0 1 1 1 : 8/16 × Tdisp 1 0 0 0 : 9/16 × Tdisp 1 0 0 1 : 10/16 × Tdisp 1 0 1 0 : 11/16 × Tdisp 1 0 1 1 : 12/16 × Tdisp 1 1 0 0 : 13/16 × Tdisp 1 1 0 1 : 14/16 × Tdisp 1 1 1 0 : 15/16 × Tdisp 1 1 1 1 : 16/16 × Tdisp	0	○	○
3			0	○	○
4			0	○	○
5			0	○	○
6	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
7	High-breakdown-voltage drivability selection bit	0 : Strong drivability 1 : Weak drivability	0	○	○

Fig. 2.5.5 Structure of FLDC mode register 1

3819 Group

2.5 FLD controller

2. APPLICATION

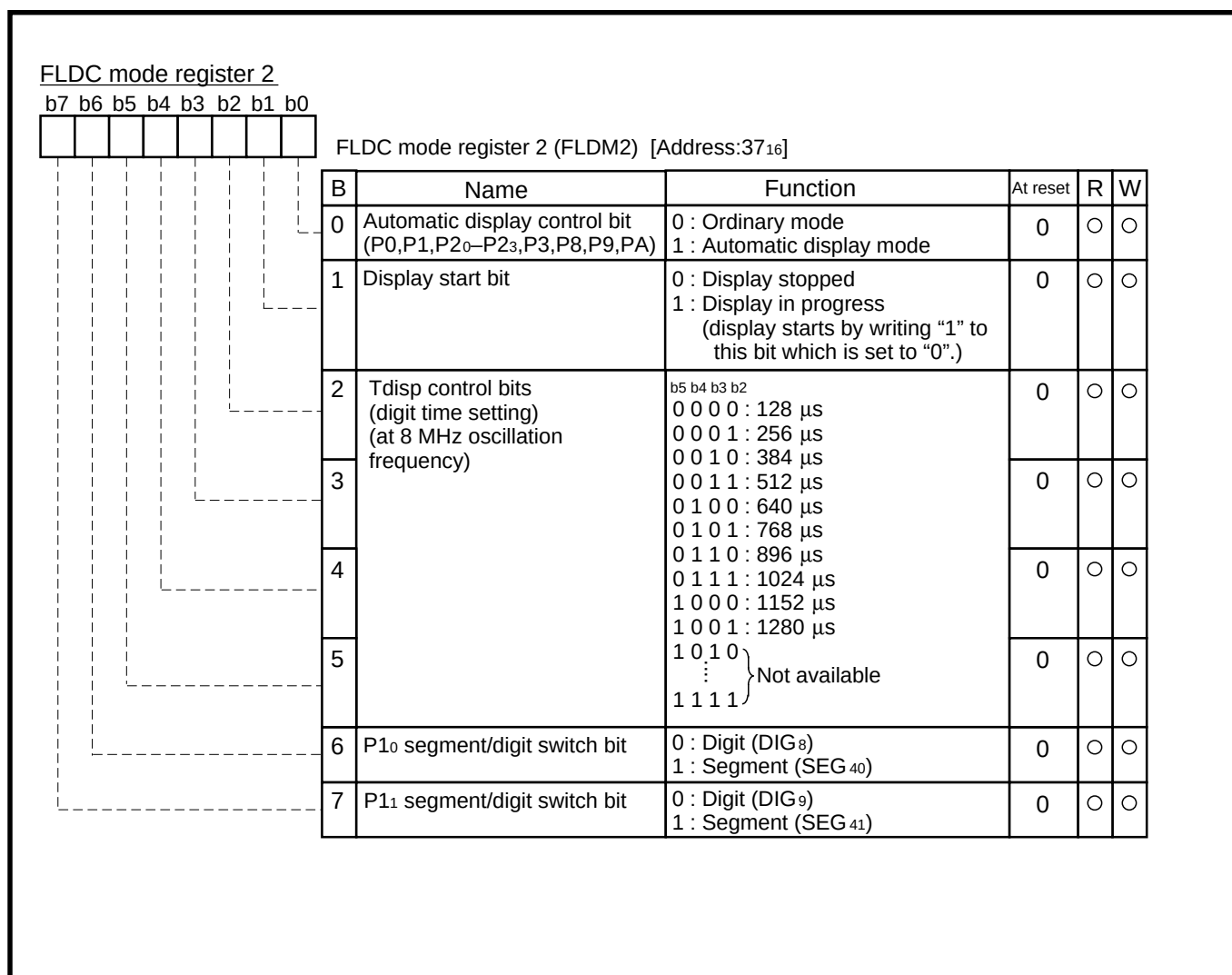


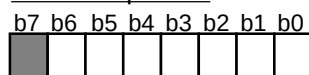
Fig. 2.5.6 Structure of FLDC mode register 2

3819 Group

2.5 FLD controller

2. APPLICATION

FLD data pointer

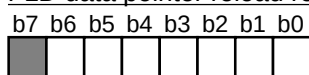


FLD data pointer (FLDDP) [Address:38₁₆]

B	Function	At reset	R	W
0	Indicate the address of data which is transferred to the segment of the FLD automatic display RAM.	?	○	×
1		?	○	×
2		?	○	×
3		?	○	×
4		?	○	×
5		?	○	×
6		?	○	×
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."	0	○	×

Fig. 2.5.7 Structure of FLD data pointer

FLD data pointer reload register



FLD data pointer reload register (FLDDP) [Address:38₁₆]

B	Function	At reset	R	W
0	Indicate the first digit address of the high-order segment.	?	×	○
1		?	×	○
2		?	×	○
3		?	×	○
4		?	×	○
5		?	×	○
6		?	×	○
7	Nothing is allocated for this bit. This is a write disabled bit.	?	×	×

Fig. 2.5.8 Structure of FLD data pointer reload register

3819 Group

2.5 FLD controller

2. APPLICATION

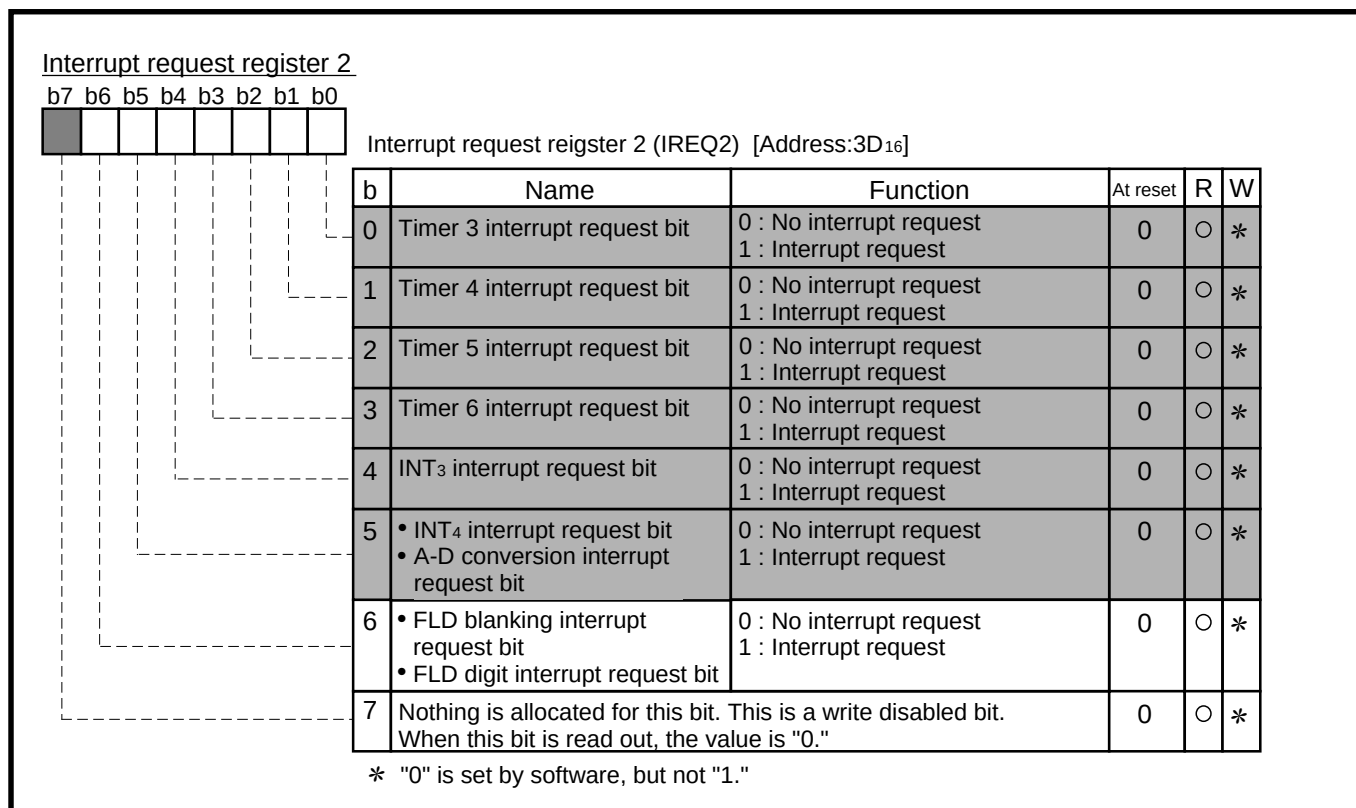


Fig. 2.5.9 Structure of Interrupt request register 2

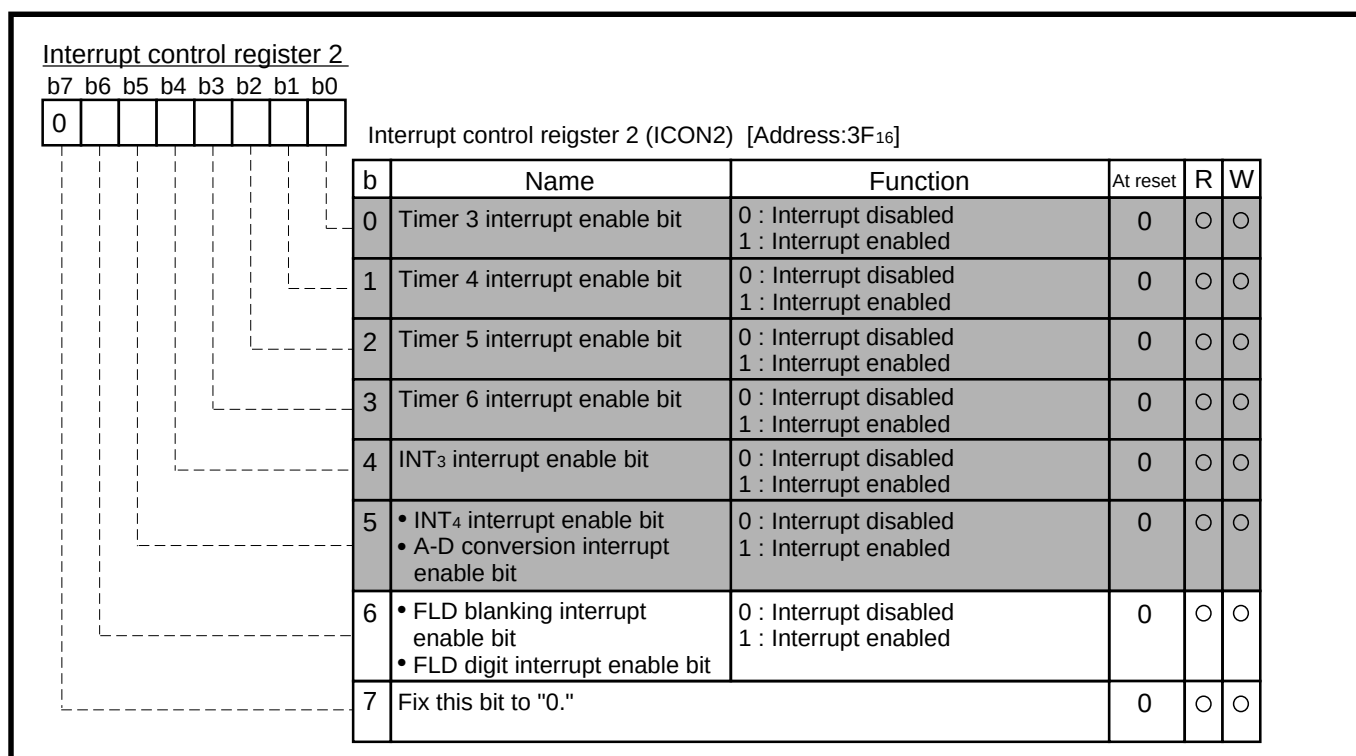


Fig. 2.5.10 Structure of Interrupt control register 2

2. APPLICATION

2.5.2 FLD controller application examples

(1) FLD automatic display and Key-scan using segment pin

Outline : The panel with fluorescent display (FLD) is displayed by using FLD automatic display function. Then the key is read in with using segment pin by software.

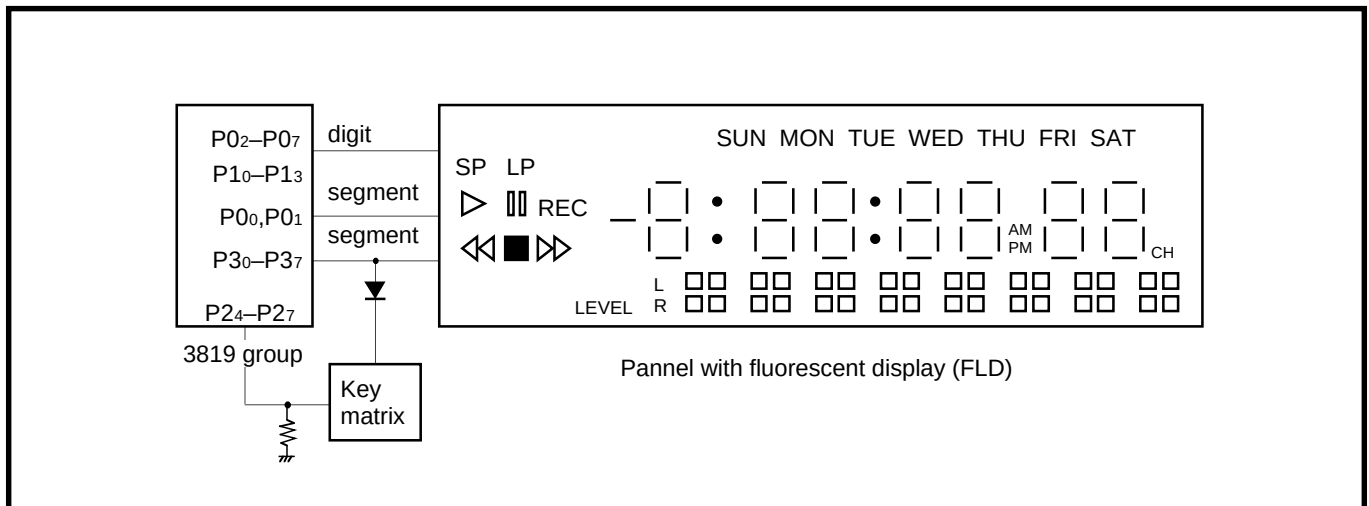


Fig. 2.5.11 Connection diagram [FLD automatic display and Key-scan using segment pin]

- Specifications :**
- The automatic display function is used.
 - 10 digits and 10 segments are used.
 - $T_{off} = 15.27 \mu s$, $T_{disp} = 244.39 \mu s$, $T_{scan} = 733.17 \mu s$ (at $f(X_{IN}) = 4.19 \text{ MHz}$)
 - The FLD blanking interrupt is used.
 - The segment pin is used for the Key-scan.

Figure 2.5.12 shows a timing chart of the Key-scan using an FLD automatic display and segments, and Figure 2.5.13 shows an enlarged view of SEG24 to SEG31 during T_{scan} .

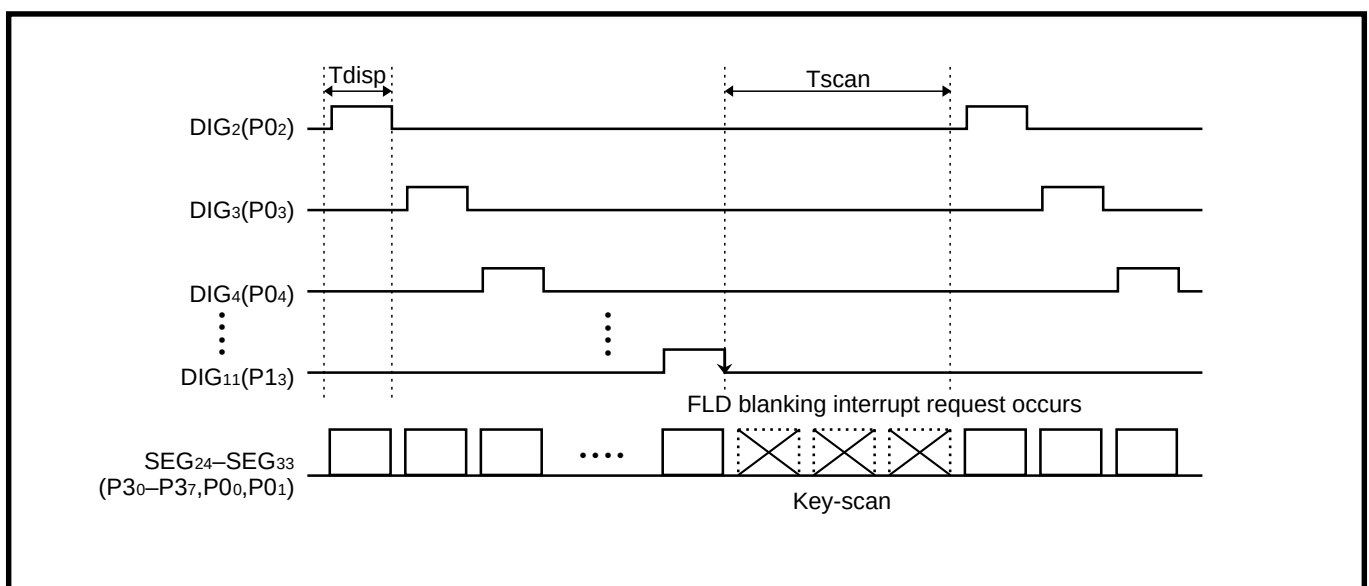


Fig. 2.5.12 Timing chart [FLD automatic display and Key-scan using segment pin]

2. APPLICATION

After switching a segment pin to an output port, the waveform shown below is created by software, and the Key-scan is performed.

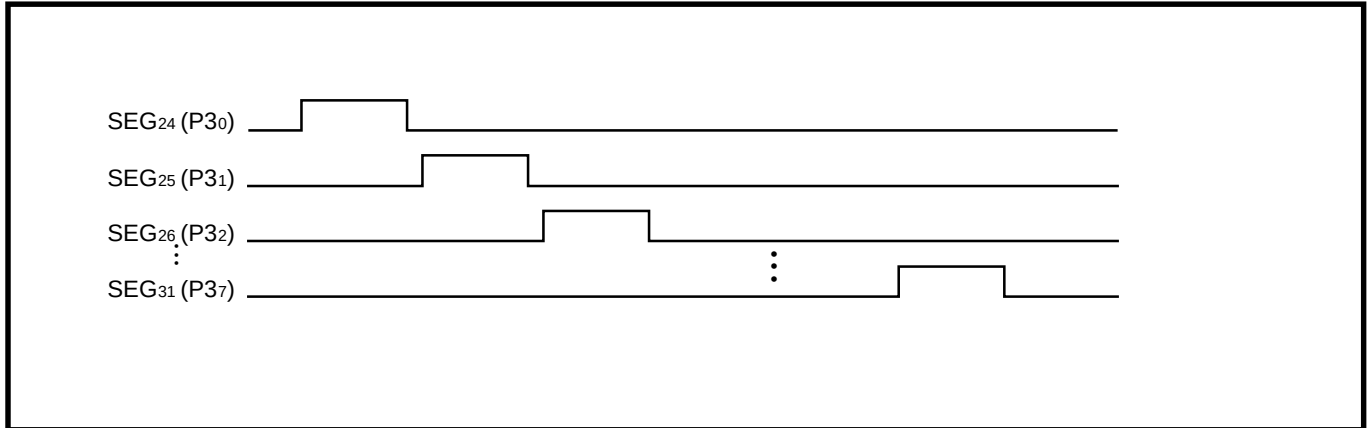


Fig. 2.5.13 Enlarged view of SEG₂₄ to SEG₃₁ during Tscan

Figures 2.5.14 and 2.5.15 show a setting of related registers.

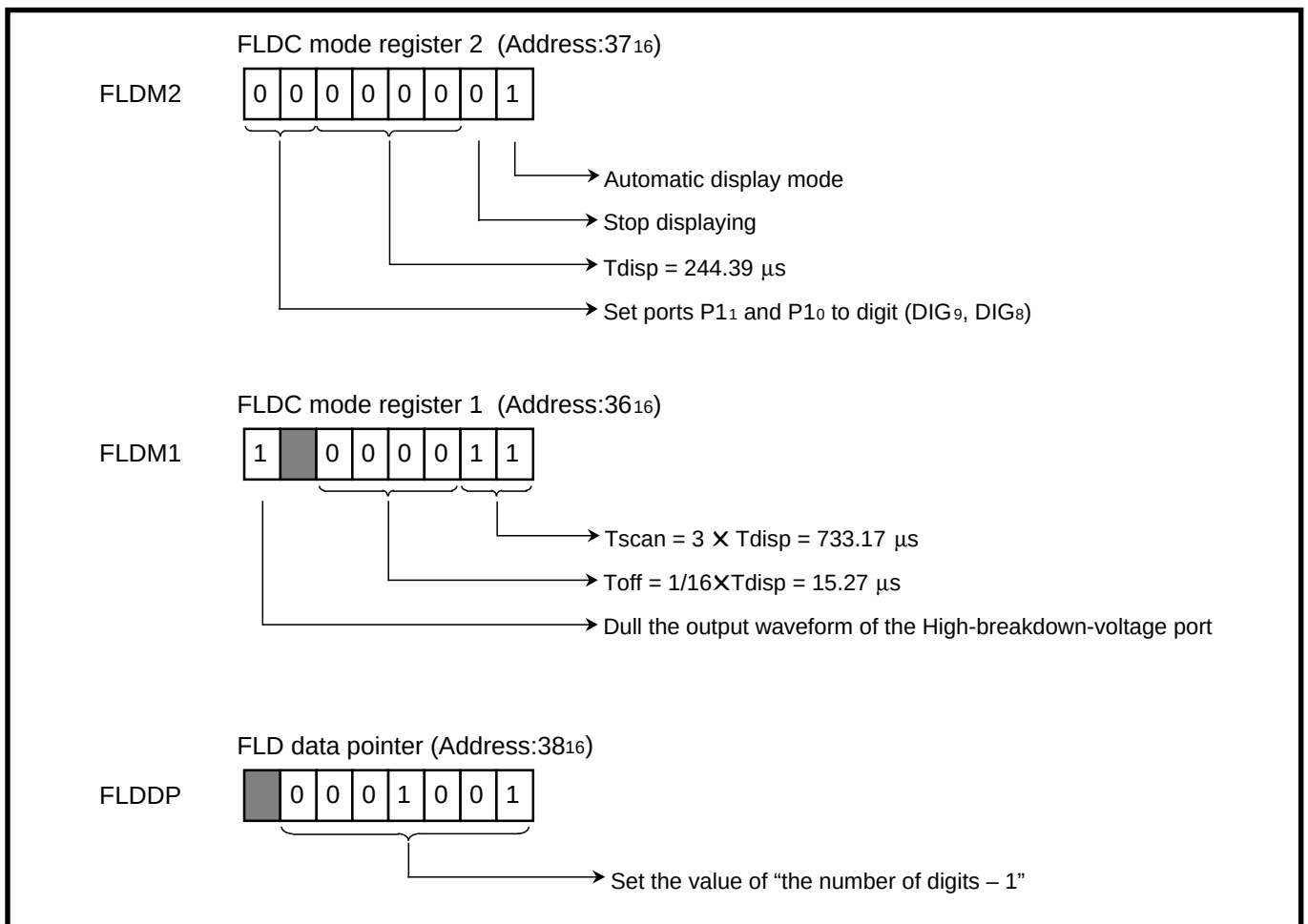


Fig. 2.5.14 Setting of related registers (1) [FLD automatic display and Key-scan using segment pin]

2. APPLICATION

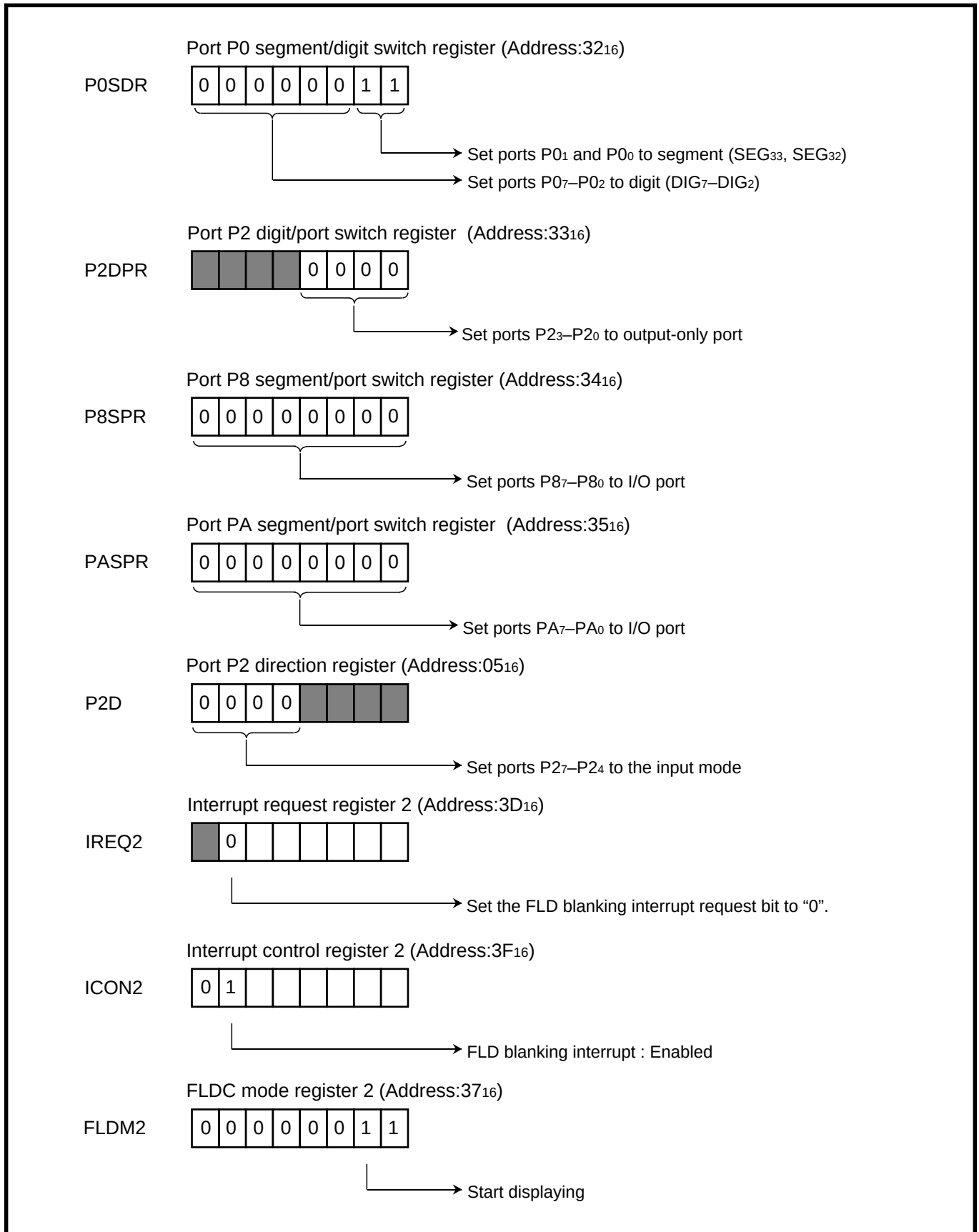


Fig. 2.5.15 Setting of related registers (2) [FLD automatic display and Key-scan using segment pin]

2. APPLICATION

Setting of FLD automatic display RAM :

Table 2.5.1 FLD automatic display RAM map [FLD automatic display and Key-scan using segment pin]

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0FB0 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₁₁ (P ₁₃)
0FB1 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₁₀ (P ₁₂)
0FB2 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₉ (P ₁₁)
0FB3 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₈ (P ₁₀)
0FB4 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₇ (P ₀₇)
0FB5 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₆ (P ₀₆)
0FB6 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₅ (P ₀₅)
0FB7 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₄ (P ₀₄)
0FB8 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₃ (P ₀₃)
0FB9 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₂ (P ₀₂)
0FBA ₁₆									
0FBB ₁₆									
0FBC ₁₆									
0FBD ₁₆									
0FBE ₁₆									
0FBF ₁₆									
0FC0 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₁₁ (P ₁₃)
0FC1 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₁₀ (P ₁₂)
0FC2 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₉ (P ₁₁)
0FC3 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₈ (P ₁₀)
0FC4 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₇ (P ₀₇)
0FC5 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₆ (P ₀₆)
0FC6 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₅ (P ₀₅)
0FC7 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₄ (P ₀₄)
0FC8 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₃ (P ₀₃)
0FC9 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₂ (P ₀₂)

 : Area which is used to set a display value

 : Area which is available as ordinary RAM

3819 Group

2.5 FLD controller

2. APPLICATION

FLD digit allocation :

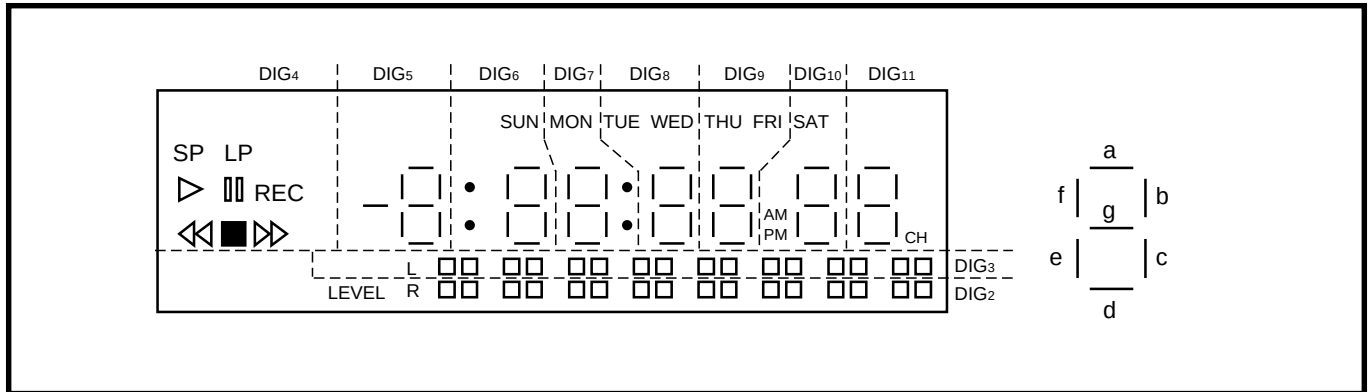


Fig. 2.5.16 Example of FLD digit allocation [FLD automatic display and Key-scan using segment pin]

Table 2.5.2 FLD automatic display RAM map example [FLD automatic display and Key-scan using segment pin]

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0FB0 ₁₆	CH	g	f	e	d	c	b	a	→ DIG ₁₁ (P ₁₃)
0FB1 ₁₆	SAT	g	f	e	d	c	b	a	→ DIG ₁₀ (P ₁₂)
0FB2 ₁₆	FRI	g	f	e	d	c	b	a	→ DIG ₉ (P ₁₁)
0FB3 ₁₆	WED	g	f	e	d	c	b	a	→ DIG ₈ (P ₁₀)
0FB4 ₁₆	MON	g	f	e	d	c	b	a	→ DIG ₇ (P ₀₇)
0FB5 ₁₆	SUN	g	f	e	d	c	b	a	→ DIG ₆ (P ₀₆)
0FB6 ₁₆	—	g	f	e	d	c	b	a	→ DIG ₅ (P ₀₅)
0FB7 ₁₆	■	◀◀	▶▶	▯▯	▷	REC	SP	LP	→ DIG ₄ (P ₀₄)
0FB8 ₁₆	□□	□□	□□	□□	□□	□□	□□	□□	→ DIG ₃ (P ₀₃)
0FB9 ₁₆	□□	□□	□□	□□	□□	□□	□□	□□	→ DIG ₂ (P ₀₂)
0FBA ₁₆									
0FBB ₁₆									
0FBC ₁₆									
0FBD ₁₆									
0FBE ₁₆									
0FBF ₁₆									
0FC0 ₁₆									→ DIG ₁₁ (P ₁₃)
0FC1 ₁₆							PM	AM	→ DIG ₁₀ (P ₁₂)
0FC2 ₁₆								THU	→ DIG ₉ (P ₁₁)
0FC3 ₁₆								TUE	→ DIG ₈ (P ₁₀)
0FC4 ₁₆								⋮	→ DIG ₇ (P ₀₇)
0FC5 ₁₆								⋮	→ DIG ₆ (P ₀₆)
0FC6 ₁₆									→ DIG ₅ (P ₀₅)
0FC7 ₁₆									→ DIG ₄ (P ₀₄)
0FC8 ₁₆							L		→ DIG ₃ (P ₀₃)
0FC9 ₁₆							R	LEVEL	→ DIG ₂ (P ₀₂)

◻ : Unused

2. APPLICATION

Control procedure :

Figure 2.5.17 shows a control procedure.

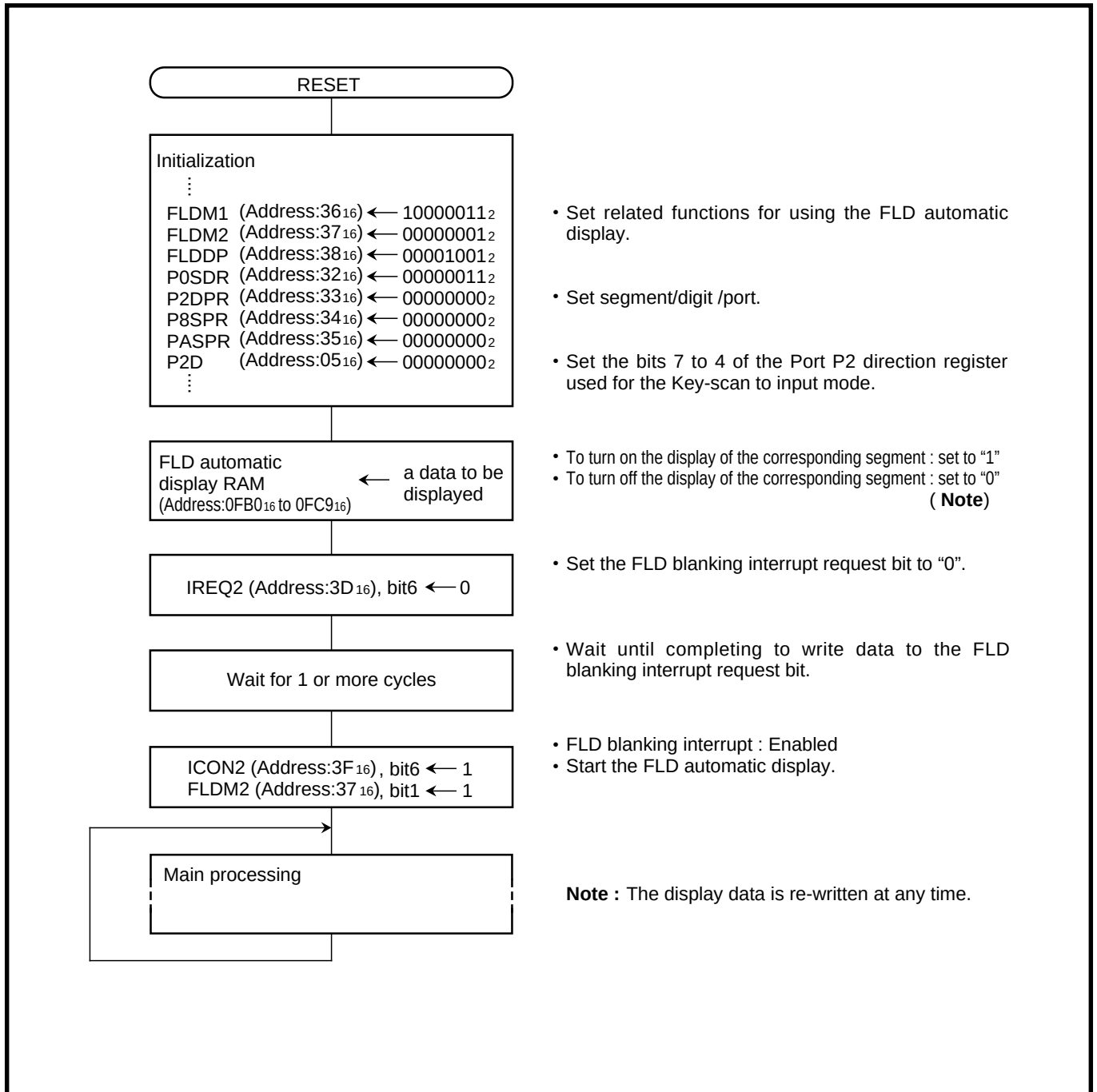


Fig. 2.5.17 Control procedure [FLD automatic display and Key-scan using segment pin]

2. APPLICATION

Segment key-scan (FLD blanking interrupt) :

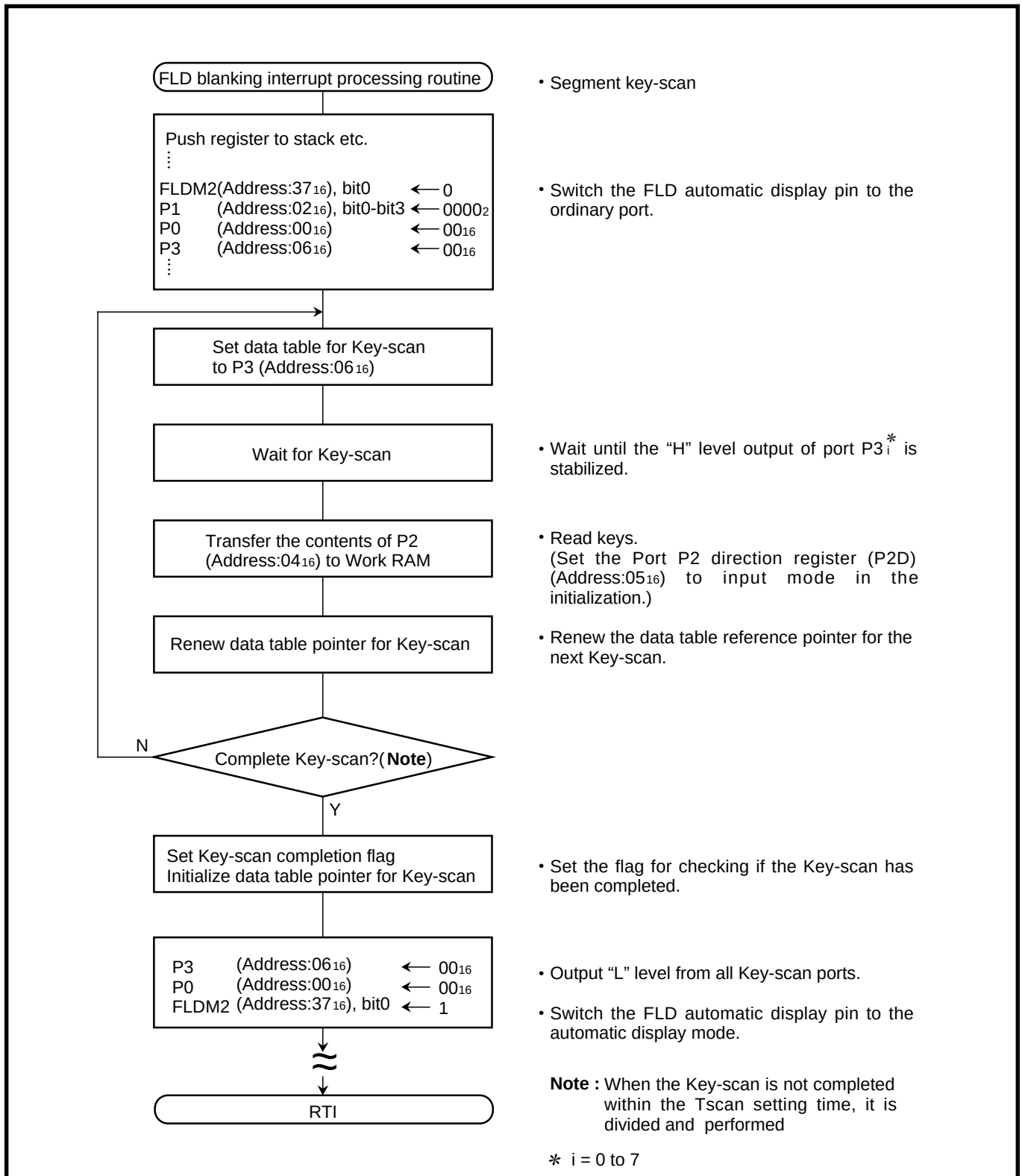


Fig. 2.5.18 Control procedure of Segment key-scan

3819 Group 2.5 FLD controller

2. APPLICATION

(2) FLD automatic display and Key-scan using digit pin

Outline : The pannel with fluorescent display (FLD) is displayed by using FLD automatic display function. Then the key is read in with using digit output waveforms.

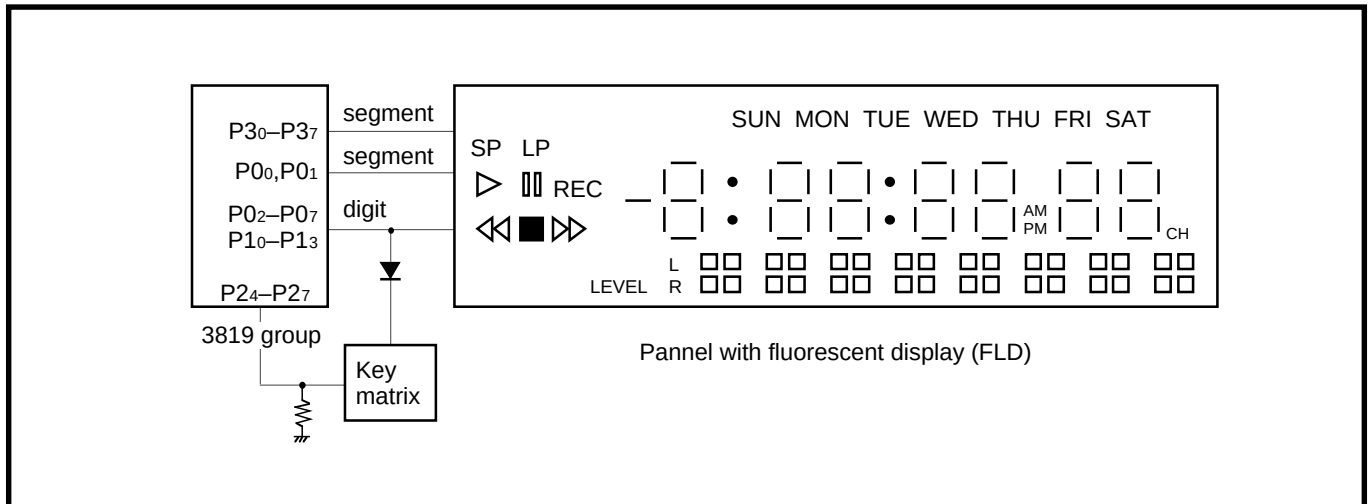


Fig. 2.5.19 Connection diagram [FLD automatic display and Key-scan using digit pin]

- Specifications :**
- The automatic display function is used.
 - 10 digits and 10 segments are used.
 - $T_{off} = 15.27 \mu s$, $T_{disp} = 244.39 \mu s$, $T_{scan} = 0 \mu s$ (at $f(XIN) = 4.19 \text{ MHz}$)
 - The FLD digit interrupt is used.
 - The digit pin is used for the Key-scan.

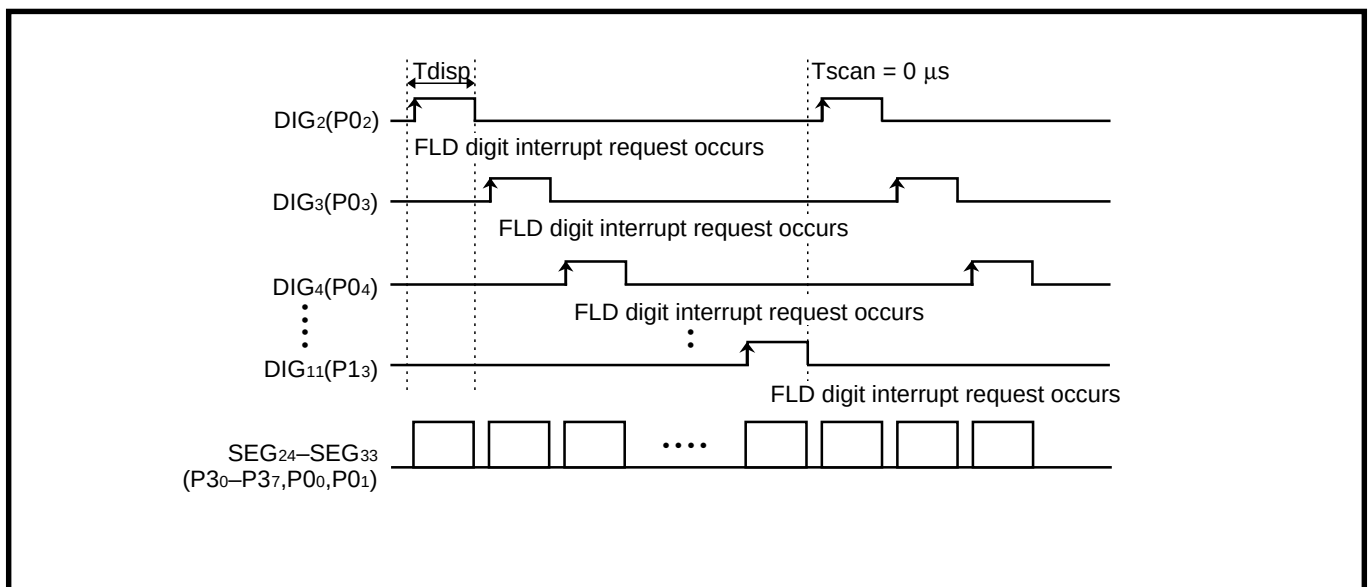


Fig. 2.5.20 Timing chart [FLD automatic display and Key-scan using digit pin]

2. APPLICATION

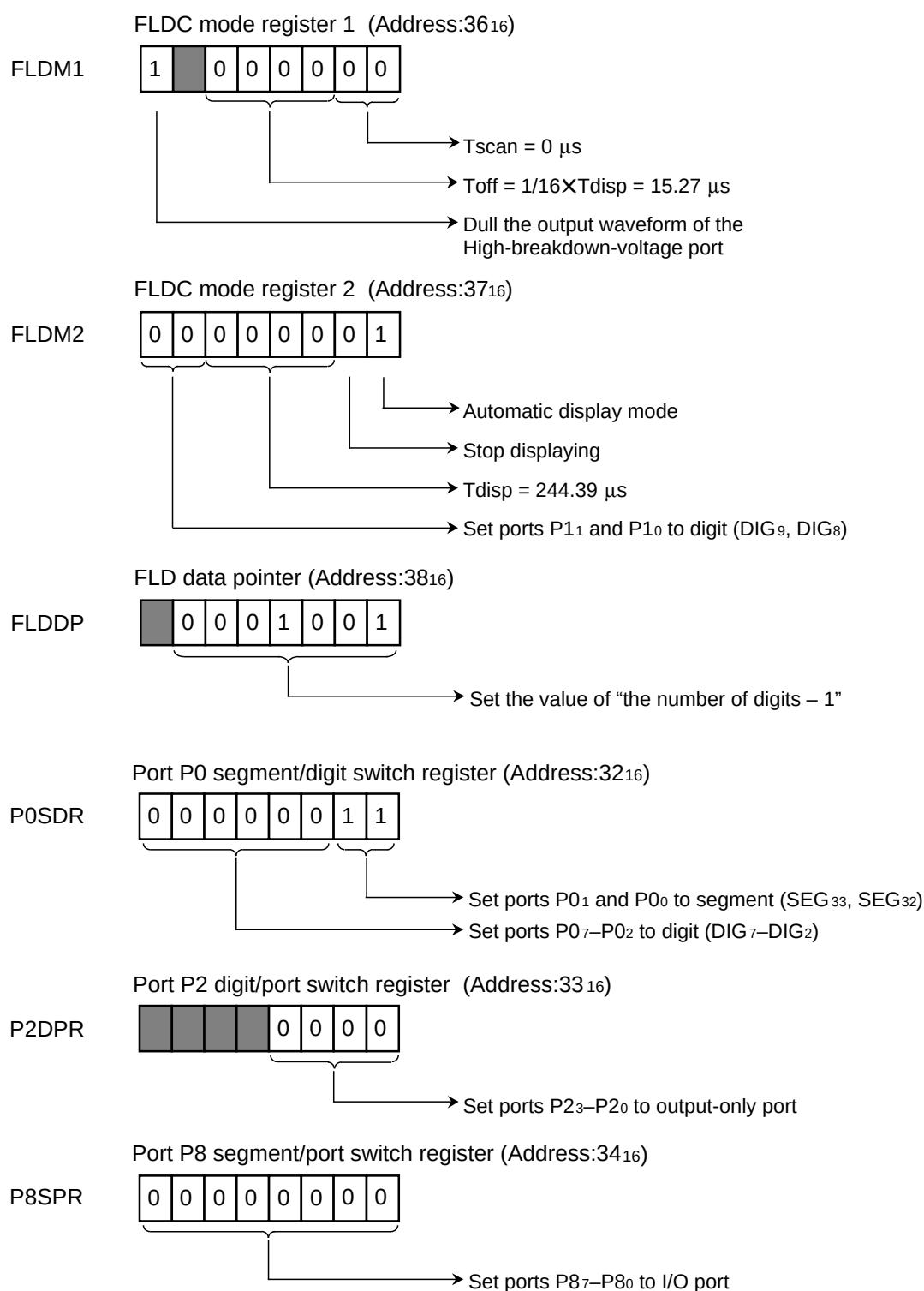


Fig. 2.5.21 Setting of related registers (1) [FLD automatic display and Key-scan using digit pin]

2. APPLICATION

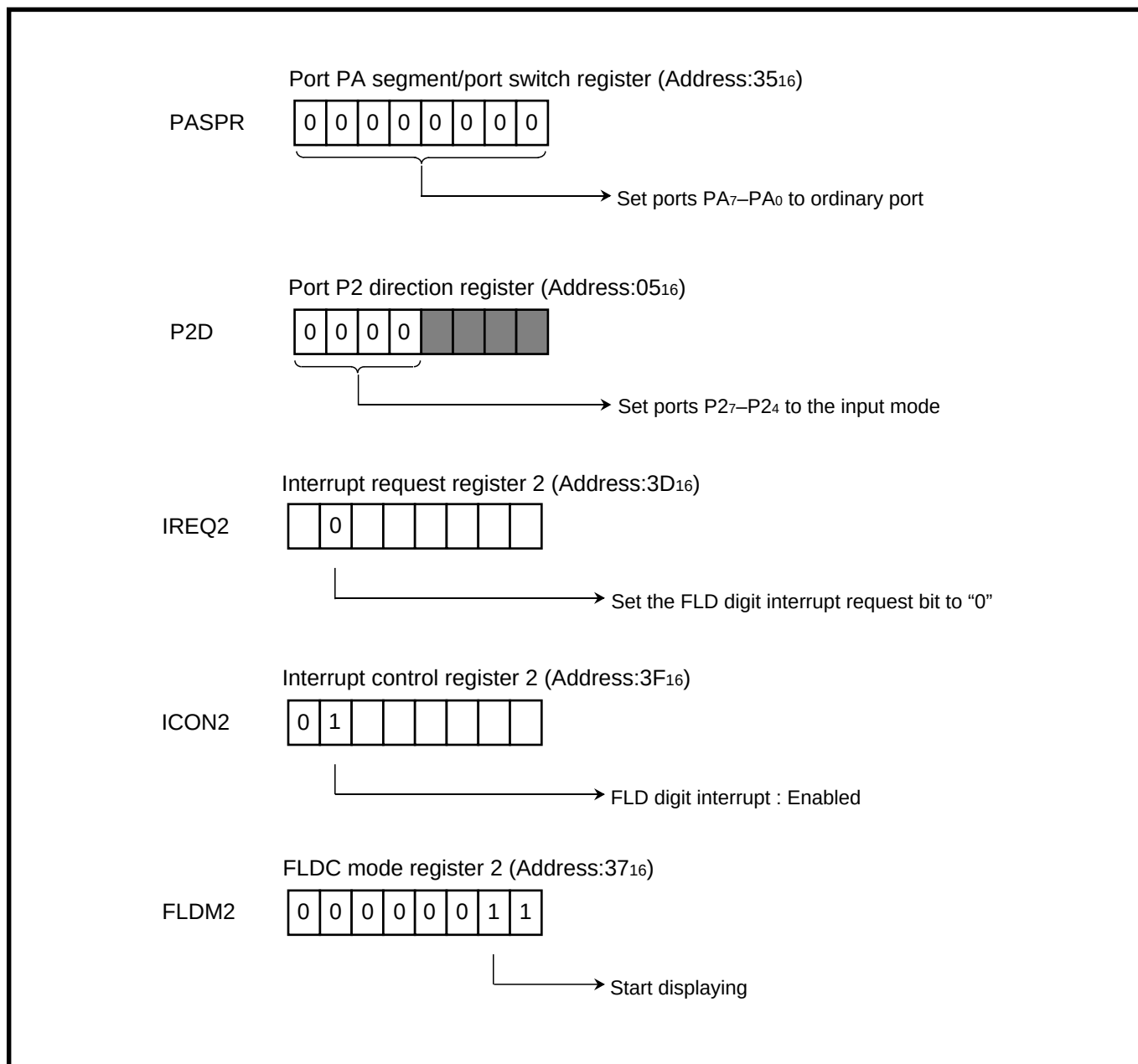


Fig. 2.5.22 Setting of related registers (2) [FLD automatic display and Key-scan using digit pin]

2. APPLICATION

3819 Group 2.5 FLD controller

Setting of FLD automatic display RAM :

Table 2.5.3 FLD automatic display RAM map [FLD automatic display and Key-scan using digit pin]

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0FB0 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₁₁ (P ₁₃)
0FB1 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₁₀ (P ₁₂)
0FB2 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₉ (P ₁₁)
0FB3 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₈ (P ₁₀)
0FB4 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₇ (P ₀₇)
0FB5 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₆ (P ₀₆)
0FB6 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₅ (P ₀₅)
0FB7 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₄ (P ₀₄)
0FB8 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₃ (P ₀₃)
0FB9 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₂ (P ₀₂)
0FBA ₁₆									
0FBB ₁₆									
0FBC ₁₆									
0FBD ₁₆									
0FBE ₁₆									
0FBF ₁₆									
0FC0 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₁₁ (P ₁₃)
0FC1 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₁₀ (P ₁₂)
0FC2 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₉ (P ₁₁)
0FC3 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₈ (P ₁₀)
0FC4 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₇ (P ₀₇)
0FC5 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₆ (P ₀₆)
0FC6 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₅ (P ₀₅)
0FC7 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₄ (P ₀₄)
0FC8 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₃ (P ₀₃)
0FC9 ₁₆							SEG ₃₃	SEG ₃₂	→ DIG ₂ (P ₀₂)

 : Area which is used to set a display value

 : Area which is available as ordinary RAM

2. APPLICATION

3819 Group 2.5 FLD controller

FLD digit allocation :

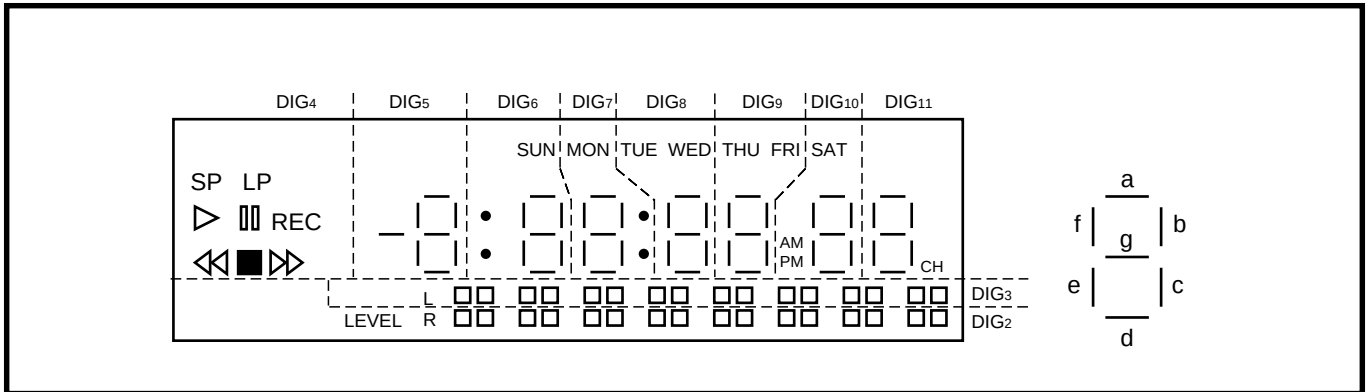


Fig. 2.5.23 Example of FLD digit allocation [FLD automatic display and Key-scan using digit pin]

Table 2.5.4 FLD automatic display RAM map example [FLD automatic display and Key-scan using digit pin]

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0FB0 ₁₆	CH	g	f	e	d	c	b	a	→ DIG ₁₁ (P ₁₃)
0FB1 ₁₆	SAT	g	f	e	d	c	b	a	→ DIG ₁₀ (P ₁₂)
0FB2 ₁₆	FRI	g	f	e	d	c	b	a	→ DIG ₉ (P ₁₁)
0FB3 ₁₆	WED	g	f	e	d	c	b	a	→ DIG ₈ (P ₁₀)
0FB4 ₁₆	MON	g	f	e	d	c	b	a	→ DIG ₇ (P ₀₇)
0FB5 ₁₆	SUN	g	f	e	d	c	b	a	→ DIG ₆ (P ₀₆)
0FB6 ₁₆	—	g	f	e	d	c	b	a	→ DIG ₅ (P ₀₅)
0FB7 ₁₆	■	◀◀	▶▶	□□	▶	REC	SP	LP	→ DIG ₄ (P ₀₄)
0FB8 ₁₆	□□	□□	□□	□□	□□	□□	□□	□□	→ DIG ₃ (P ₀₃)
0FB9 ₁₆	□□	□□	□□	□□	□□	□□	□□	□□	→ DIG ₂ (P ₀₂)
0FBA ₁₆									
0FBB ₁₆									
0FBC ₁₆									
0FBD ₁₆									
0FBE ₁₆									
0FBF ₁₆									
0FC0 ₁₆									→ DIG ₁₁ (P ₁₃)
0FC1 ₁₆							PM	AM	→ DIG ₁₀ (P ₁₂)
0FC2 ₁₆								THU	→ DIG ₉ (P ₁₁)
0FC3 ₁₆								TUE	→ DIG ₈ (P ₁₀)
0FC4 ₁₆								⋮	→ DIG ₇ (P ₀₇)
0FC5 ₁₆								⋮	→ DIG ₆ (P ₀₆)
0FC6 ₁₆									→ DIG ₅ (P ₀₅)
0FC7 ₁₆									→ DIG ₄ (P ₀₄)
0FC8 ₁₆							L		→ DIG ₃ (P ₀₃)
0FC9 ₁₆							R	LEVEL	→ DIG ₂ (P ₀₂)

◻ : Unused

3819 Group 2.5 FLD controller

2. APPLICATION

Control procedure :

Figure 2.5.24 shows a control procedure.

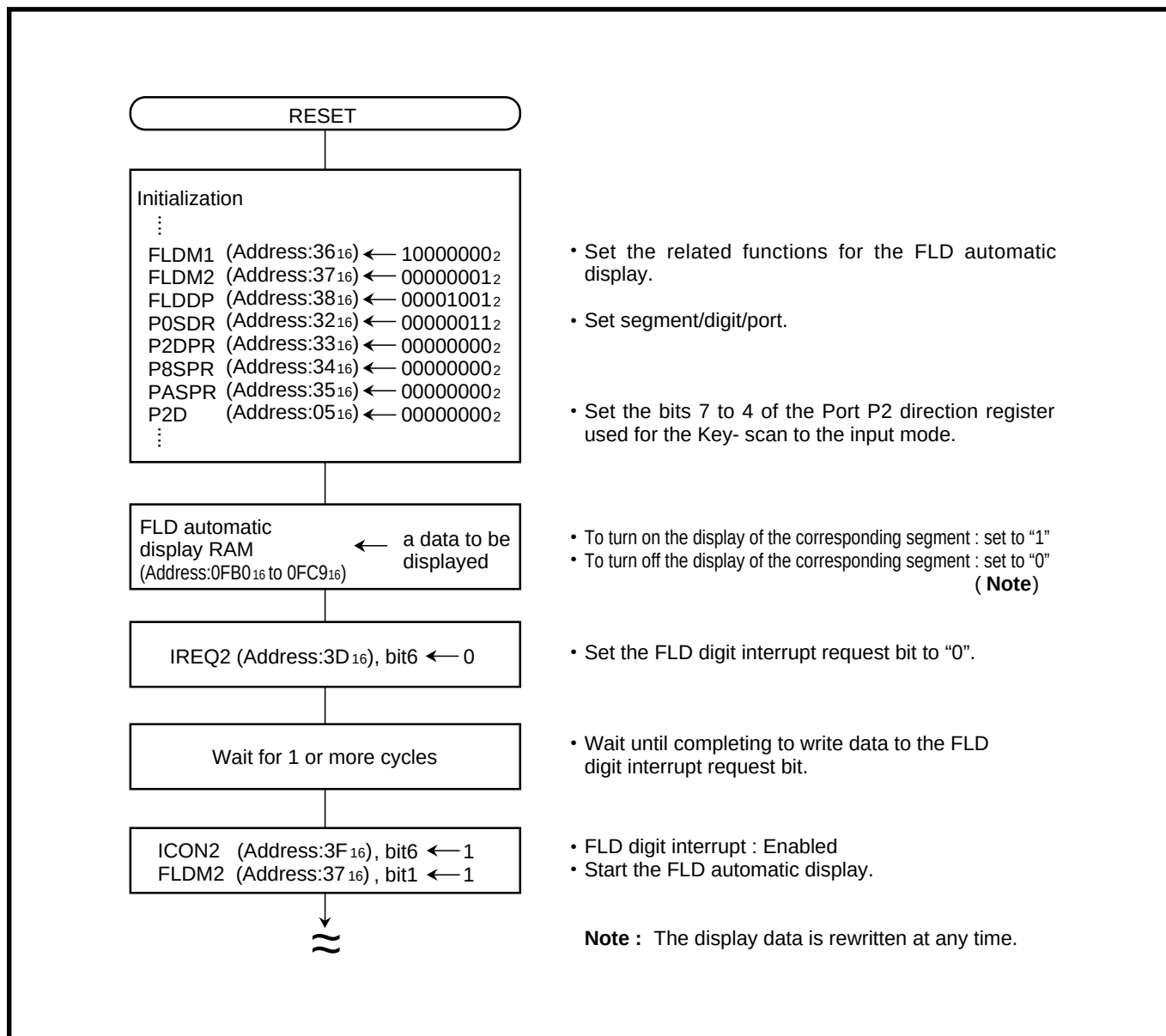


Fig. 2.5.24 Control procedure [FLD automatic display and Key-scan using digit pin]

2. APPLICATION

Digit key-scan (FLD digit interrupt) :

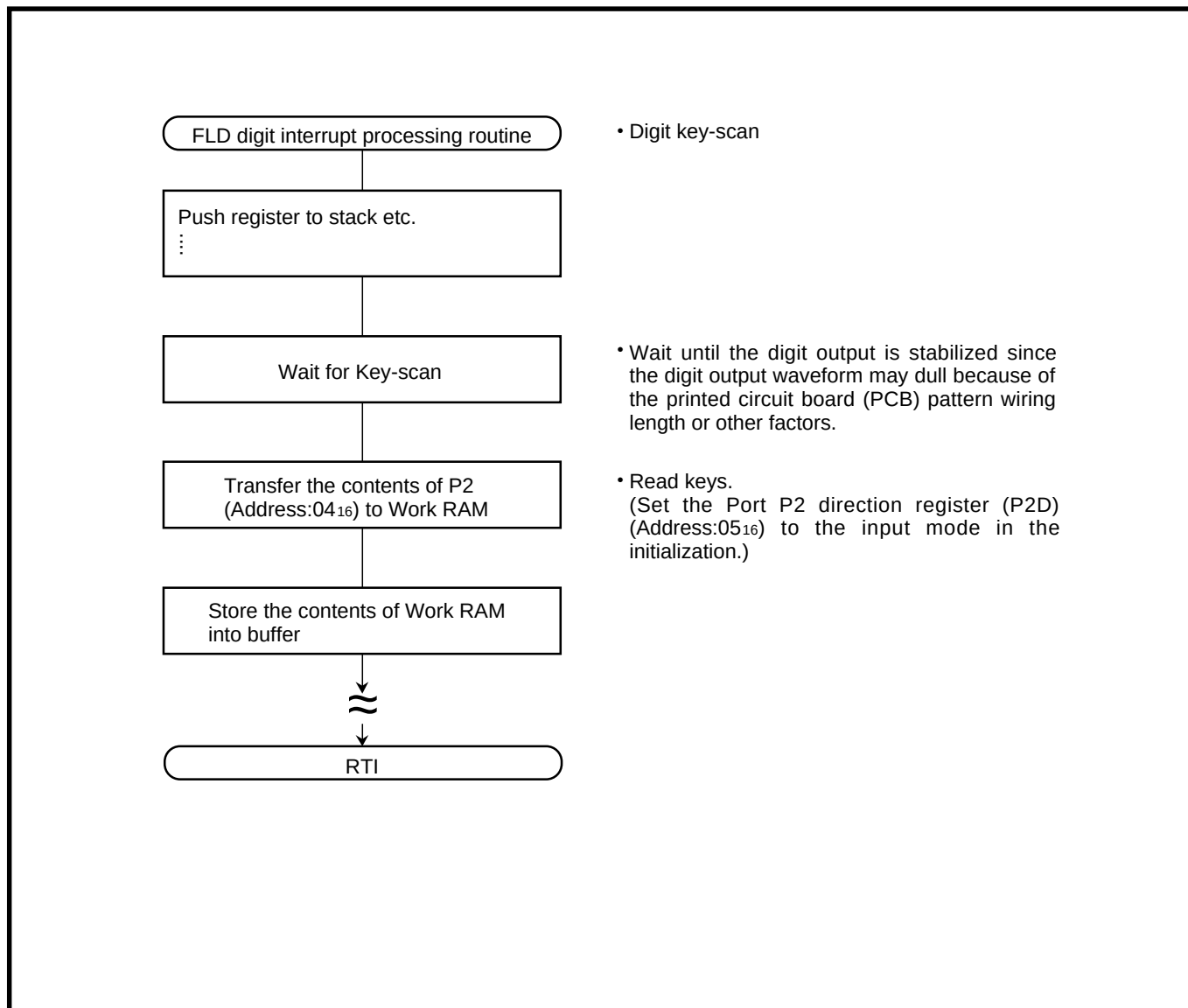


Fig. 2.5.25 Control procedure of Digit key-scan

3819 Group 2.5 FLD controller

2. APPLICATION

(3) FLD display by software (example of without using FLD controller)

Outline : The FLD display and the key read-in are performed by using timer interrupts.

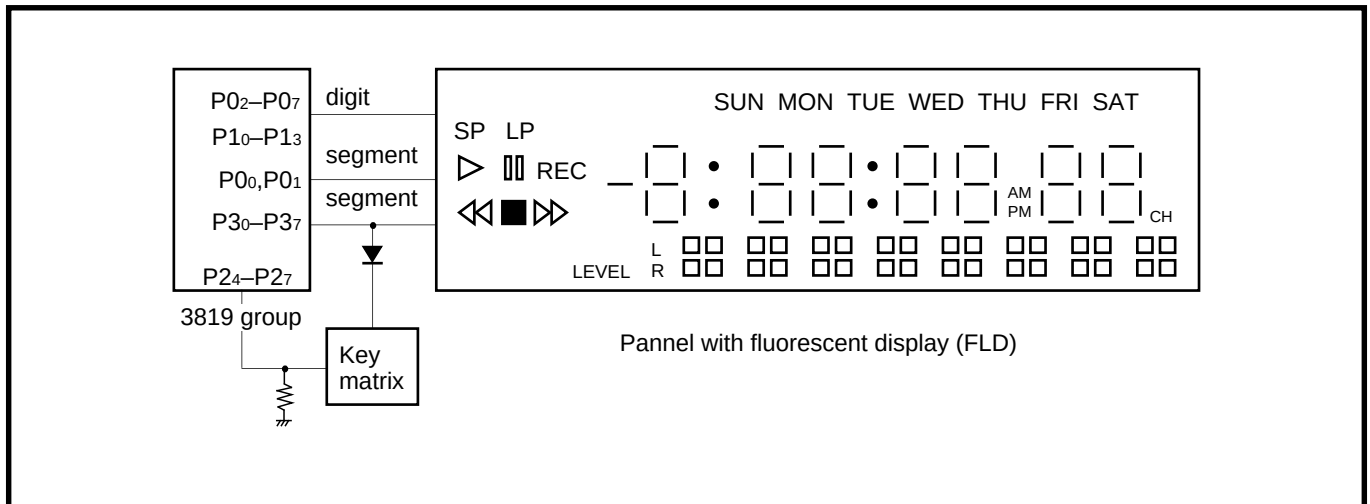


Fig. 2.5.26 Connection diagram [FLD display by software]

- Specifications :**
- The display is controlled by software.
 - 10 digits and 10 segments are used.
 - The Timer 1 interrupts are used.
 - The segment pin is used for Key-scan.

Fig. 2.5.27 shows a timing chart of FLD display by software, and Fig. 2.5.28 shows an enlarged view of Key-scan of ports P30 to P37.

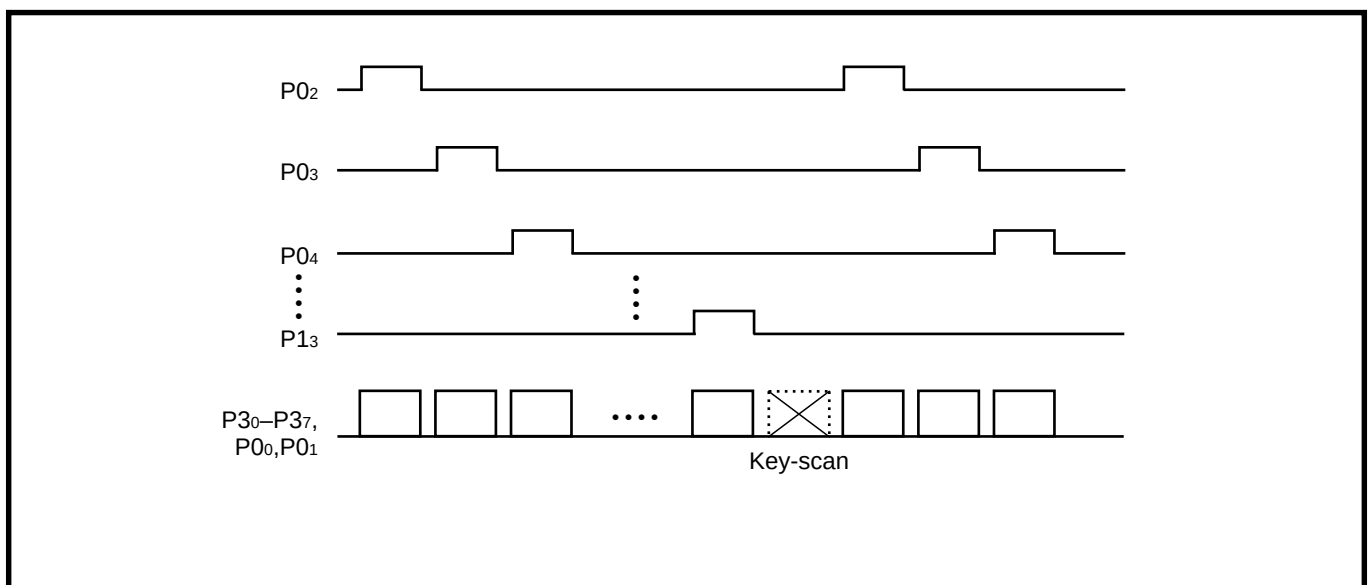


Fig. 2.5.27 Timing chart [FLD display by software]

2. APPLICATION

The waveform shown below is created by software, and the Key-scan is performed.

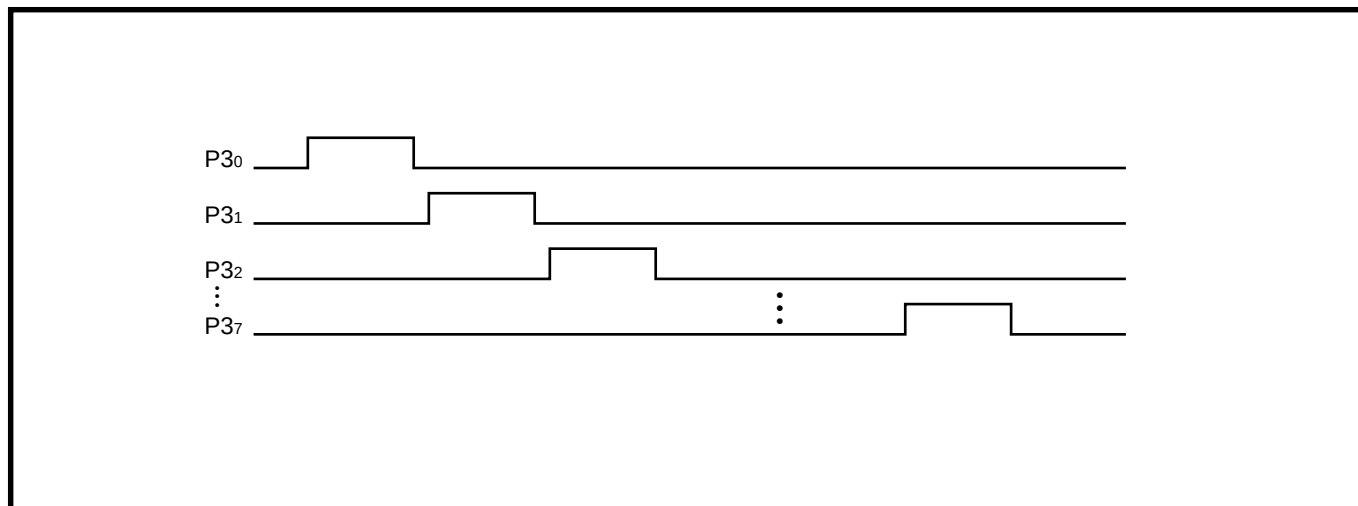


Fig. 2.5.28 Enlarged view of Key-scan of ports P30 to P37

Figure 2.5.29 shows a setting of related registers.

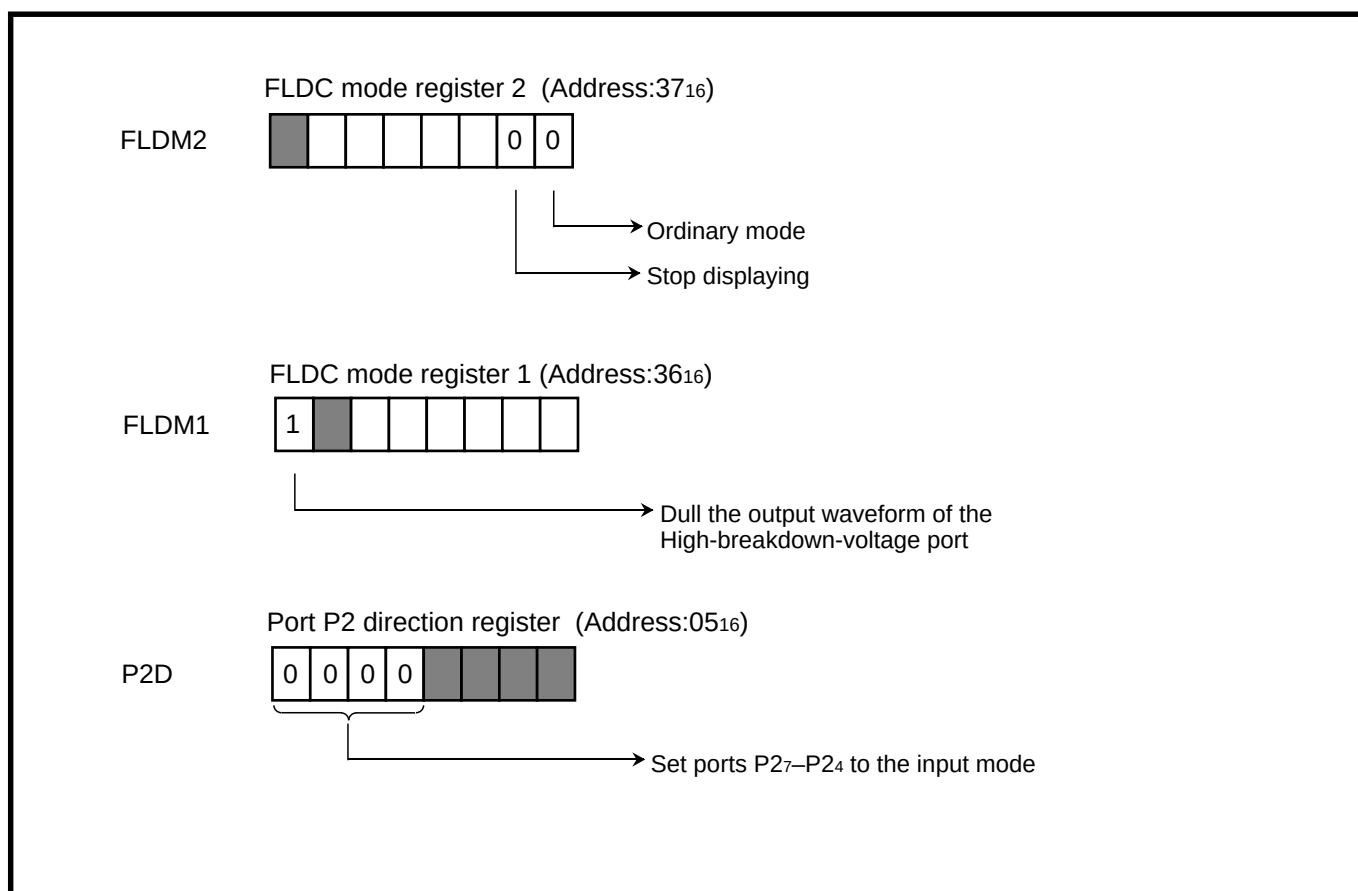


Fig. 2.5.29 Setting of related registers [FLD display by software]

3819 Group

2.5 FLD controller

2. APPLICATION

FLD digit allocation :

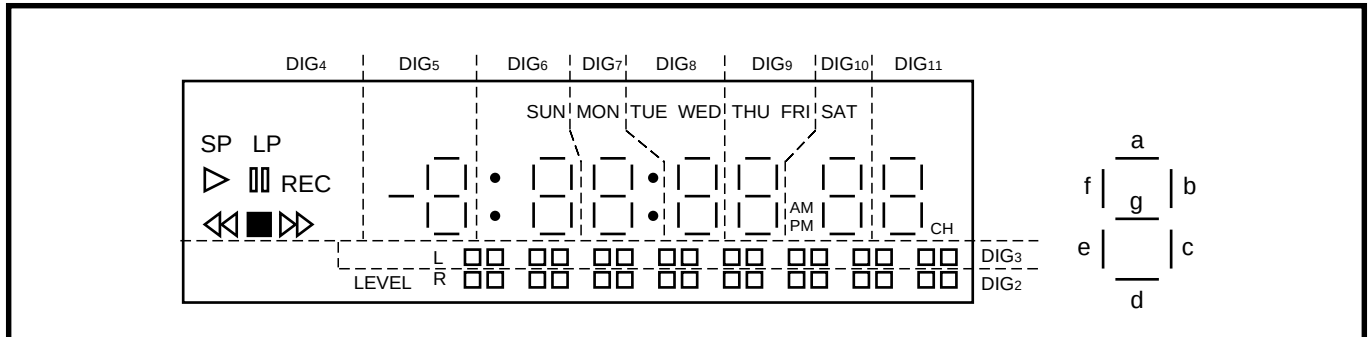


Fig. 2.5.30 Example of FLD digit allocation [FLD display by software]

Table 2.5.5 FLD automatic display RAM map example [FLD display by software]
(Automatic display is not performed because of not using FLD controller)

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0FB0 ₁₆	CH	g	f	e	d	c	b	a	→ DIG11 (P13)
0FB1 ₁₆	SAT	g	f	e	d	c	b	a	→ DIG10 (P12)
0FB2 ₁₆	FRI	g	f	e	d	c	b	a	→ DIG9 (P11)
0FB3 ₁₆	WED	g	f	e	d	c	b	a	→ DIG8 (P10)
0FB4 ₁₆	MON	g	f	e	d	c	b	a	→ DIG7 (P07)
0FB5 ₁₆	SUN	g	f	e	d	c	b	a	→ DIG6 (P06)
0FB6 ₁₆	—	g	f	e	d	c	b	a	→ DIG5 (P05)
0FB7 ₁₆	■	◀◀	▶▶	▢▢	▷	REC	SP	LP	→ DIG4 (P04)
0FB8 ₁₆	□□	□□	□□	□□	□□	□□	□□	□□	→ DIG3 (P03)
0FB9 ₁₆	□□	□□	□□	□□	□□	□□	□□	□□	→ DIG2 (P02)
0FBA ₁₆									
0FBB ₁₆									
0FBC ₁₆									
0FBD ₁₆									
0FBE ₁₆									
0FBF ₁₆									
0FC0 ₁₆									→ DIG11 (P13)
0FC1 ₁₆							PM	AM	→ DIG10 (P12)
0FC2 ₁₆								THU	→ DIG9 (P11)
0FC3 ₁₆								TUE	→ DIG8 (P10)
0FC4 ₁₆								•	→ DIG7 (P07)
0FC5 ₁₆								•	→ DIG6 (P06)
0FC6 ₁₆									→ DIG5 (P05)
0FC7 ₁₆									→ DIG4 (P04)
0FC8 ₁₆							L		→ DIG3 (P03)
0FC9 ₁₆							R	LEVEL	→ DIG2 (P02)

◻ : Unused

3819 Group 2.5 FLD controller

2. APPLICATION

Control procedure :

Figure 2.5.31 shows a control procedure.

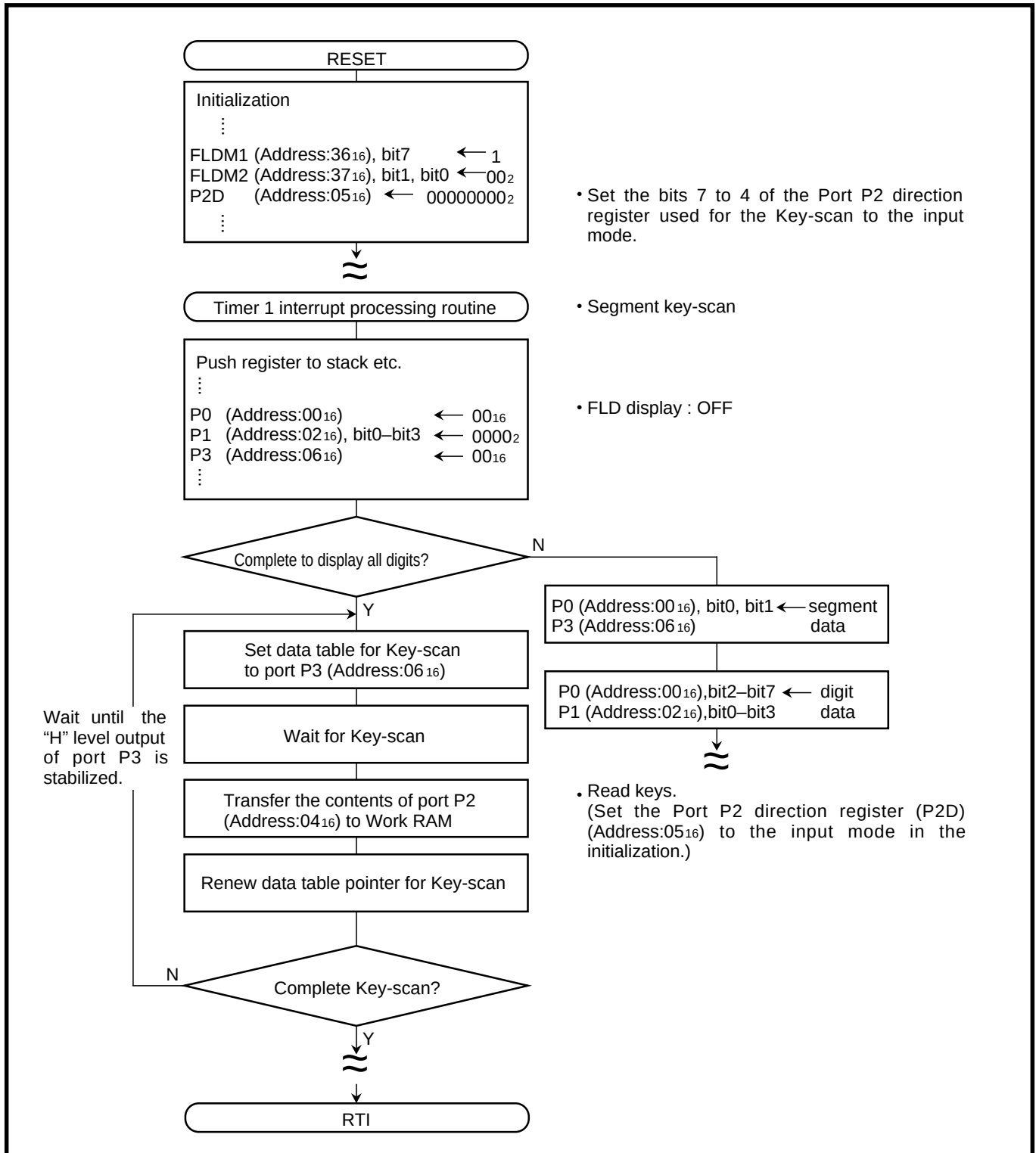


Fig. 2.5.31 Control procedure [FLD display by software]

2. APPLICATION

(4) 5 × 7 dot display

Outline : The 5 × 7 dot display is performed by using the FLD automatic display function.

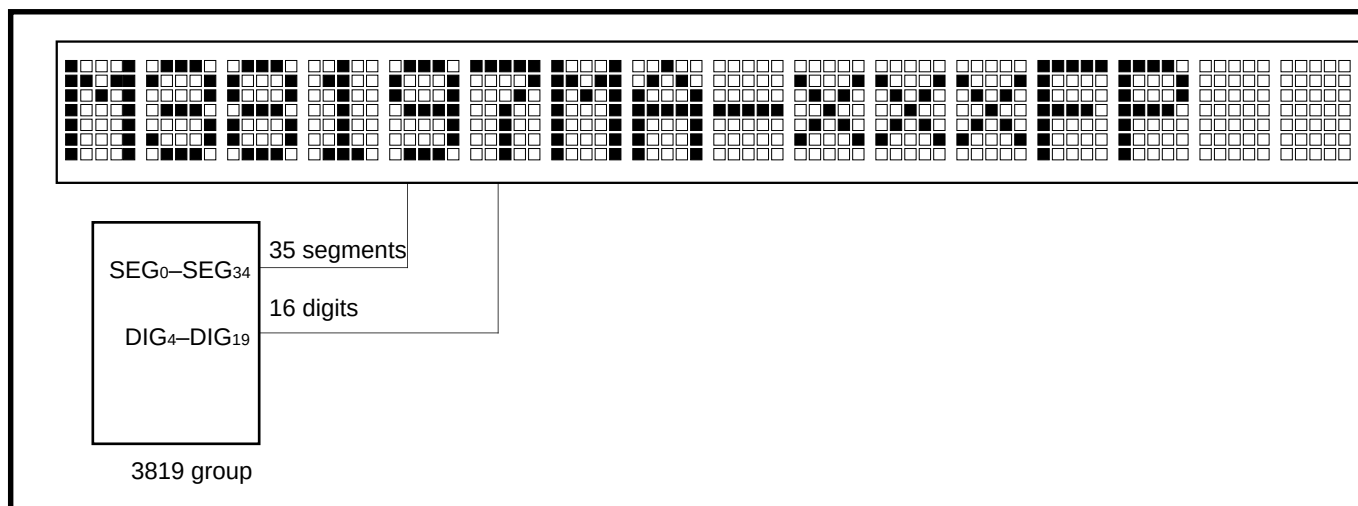


Fig. 2.5.32 Connection diagram [5 × 7 dot display]

- Specifications :**
- The automatic display function is used.
 - 16 digits and 35 segments are used.
 - $T_{off} = 288 \mu s$, $T_{disp} = 512 \mu s$, $T_{scan} = 512 \mu s$ (at $f(XIN) = 8 \text{ MHz}$)

Figure 2.5.33 shows a timing chart of FLD automatic display.

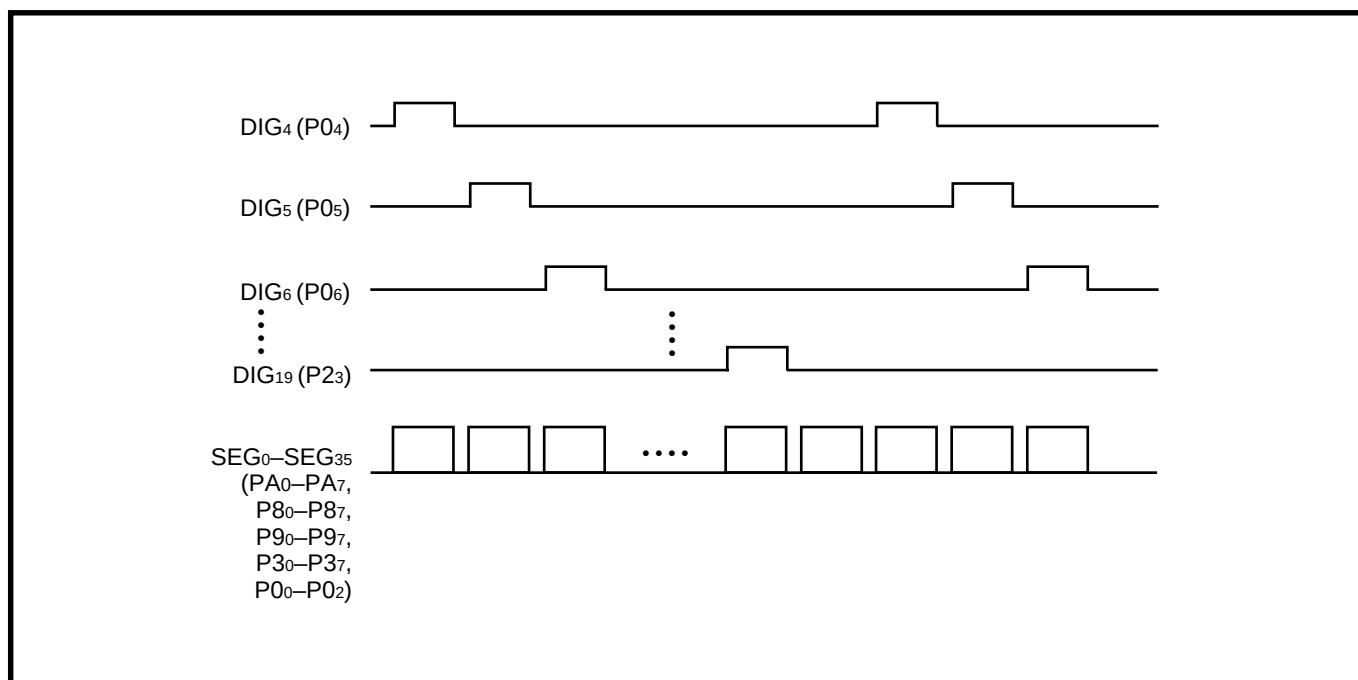


Fig. 2.5.33 Timing chart [5 × 7 dot display]

2. APPLICATION

Figures 2.5.34 and 2.5.35 show a setting of related registers.

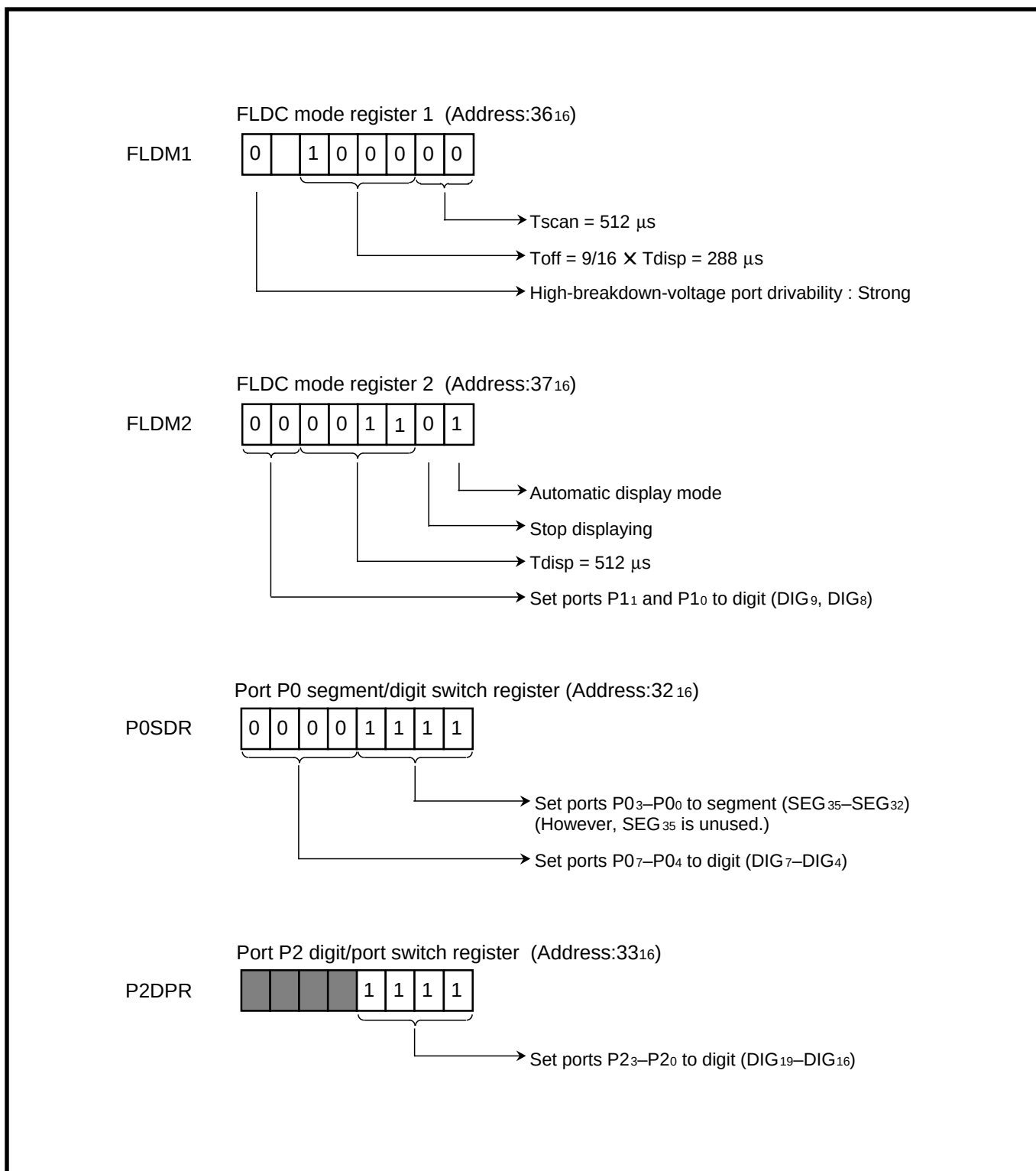


Fig. 2.5.34 Setting of related registers (1) [5 × 7 dot display]

2. APPLICATION



Fig. 2.5.35 Setting of related registers (2) [5 × 7 dot display]

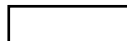
3819 Group 2.5 FLD controller

2. APPLICATION

Setting of FLD automatic display RAM :

Table 2.5.6 FLD automatic display RAM map [5 × 7 dot display]

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0F80 ₁₆	SEG ₇	SEG ₆	SEG ₅	SEG ₄	SEG ₃	SEG ₂	SEG ₁	SEG ₀	→ DIG ₁₉ (P ₂₃)
0F81 ₁₆									→ DIG ₁₈ (P ₂₂)
0F82 ₁₆									→ DIG ₁₇ (P ₂₁)
0F83 ₁₆									→ DIG ₁₆ (P ₂₀)
0F84 ₁₆									→ DIG ₁₅ (P ₁₇)
0F85 ₁₆									→ DIG ₁₄ (P ₁₆)
0F86 ₁₆									→ DIG ₁₃ (P ₁₅)
0F87 ₁₆									→ DIG ₁₂ (P ₁₄)
0F88 ₁₆									→ DIG ₁₁ (P ₁₃)
0F89 ₁₆									→ DIG ₁₀ (P ₁₂)
0F8A ₁₆									→ DIG ₉ (P ₁₁)
0F8B ₁₆									→ DIG ₈ (P ₁₀)
0F8C ₁₆									→ DIG ₇ (P ₀₇)
0F8D ₁₆									→ DIG ₆ (P ₀₆)
0F8E ₁₆									→ DIG ₅ (P ₀₅)
0F8F ₁₆									→ DIG ₄ (P ₀₄)
0F90 ₁₆	SEG ₁₅	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	SEG ₈	→ DIG ₁₉ (P ₂₃)
0F91 ₁₆									→ DIG ₁₈ (P ₂₂)
0F92 ₁₆									→ DIG ₁₇ (P ₂₁)
0F93 ₁₆									→ DIG ₁₆ (P ₂₀)
0F94 ₁₆									→ DIG ₁₅ (P ₁₇)
0F95 ₁₆									→ DIG ₁₄ (P ₁₆)
0F96 ₁₆									→ DIG ₁₃ (P ₁₅)
0F97 ₁₆									→ DIG ₁₂ (P ₁₄)
0F98 ₁₆									→ DIG ₁₁ (P ₁₃)
0F99 ₁₆									→ DIG ₁₀ (P ₁₂)
0F9A ₁₆									→ DIG ₉ (P ₁₁)
0F9B ₁₆									→ DIG ₈ (P ₁₀)
0F9C ₁₆									→ DIG ₇ (P ₀₇)
0F9D ₁₆									→ DIG ₆ (P ₀₆)
0F9E ₁₆									→ DIG ₅ (P ₀₅)
0F9F ₁₆									→ DIG ₄ (P ₀₄)
0FA0 ₁₆	SEG ₂₃	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	SEG ₁₆	→ DIG ₁₉ (P ₂₃)
0FA1 ₁₆									→ DIG ₁₈ (P ₂₂)
0FA2 ₁₆									→ DIG ₁₇ (P ₂₁)
0FA3 ₁₆									→ DIG ₁₆ (P ₂₀)
0FA4 ₁₆									→ DIG ₁₅ (P ₁₇)
0FA5 ₁₆									→ DIG ₁₄ (P ₁₆)
0FA6 ₁₆									→ DIG ₁₃ (P ₁₅)
0FA7 ₁₆									→ DIG ₁₂ (P ₁₄)
0FA8 ₁₆									→ DIG ₁₁ (P ₁₃)
0FA9 ₁₆									→ DIG ₁₀ (P ₁₂)
0FAA ₁₆									→ DIG ₉ (P ₁₁)
0FAB ₁₆									→ DIG ₈ (P ₁₀)
0FAC ₁₆									→ DIG ₇ (P ₀₇)
0FAD ₁₆									→ DIG ₆ (P ₀₆)
0FAE ₁₆									→ DIG ₅ (P ₀₅)
0FAF ₁₆									→ DIG ₄ (P ₀₄)
0FB0 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	→ DIG ₁₉ (P ₂₃)
0FB1 ₁₆									→ DIG ₁₈ (P ₂₂)
0FB2 ₁₆									→ DIG ₁₇ (P ₂₁)
0FB3 ₁₆									→ DIG ₁₆ (P ₂₀)
0FB4 ₁₆									→ DIG ₁₅ (P ₁₇)
0FB5 ₁₆									→ DIG ₁₄ (P ₁₆)
0FB6 ₁₆									→ DIG ₁₃ (P ₁₅)
0FB7 ₁₆									→ DIG ₁₂ (P ₁₄)
0FB8 ₁₆									→ DIG ₁₁ (P ₁₃)
0FB9 ₁₆									→ DIG ₁₀ (P ₁₂)
0FBA ₁₆									→ DIG ₉ (P ₁₁)
0FBB ₁₆									→ DIG ₈ (P ₁₀)
0FBC ₁₆									→ DIG ₇ (P ₀₇)
0FBD ₁₆									→ DIG ₆ (P ₀₆)
0FBE ₁₆									→ DIG ₅ (P ₀₅)
0FBF ₁₆									→ DIG ₄ (P ₀₄)
0FC0 ₁₆						SEG ₃₄	SEG ₃₃	SEG ₃₂	→ DIG ₁₉ (P ₂₃)
0FC1 ₁₆									→ DIG ₁₈ (P ₂₂)
0FC2 ₁₆									→ DIG ₁₇ (P ₂₁)
0FC3 ₁₆									→ DIG ₁₆ (P ₂₀)
0FC4 ₁₆									→ DIG ₁₅ (P ₁₇)
0FC5 ₁₆									→ DIG ₁₄ (P ₁₆)
0FC6 ₁₆									→ DIG ₁₃ (P ₁₅)
0FC7 ₁₆									→ DIG ₁₂ (P ₁₄)
0FC8 ₁₆									→ DIG ₁₁ (P ₁₃)
0FC9 ₁₆									→ DIG ₁₀ (P ₁₂)
0FCA ₁₆									→ DIG ₉ (P ₁₁)
0FCB ₁₆									→ DIG ₈ (P ₁₀)
0FCC ₁₆									→ DIG ₇ (P ₀₇)
0FCD ₁₆									→ DIG ₆ (P ₀₆)
0FCE ₁₆									→ DIG ₅ (P ₀₅)
0FCF ₁₆									→ DIG ₄ (P ₀₄)

 : Area which is used to set a display value
 : Area which is available as ordinary RAM

2. APPLICATION

Control procedure :

Figure 2.5.38 shows a control procedure.

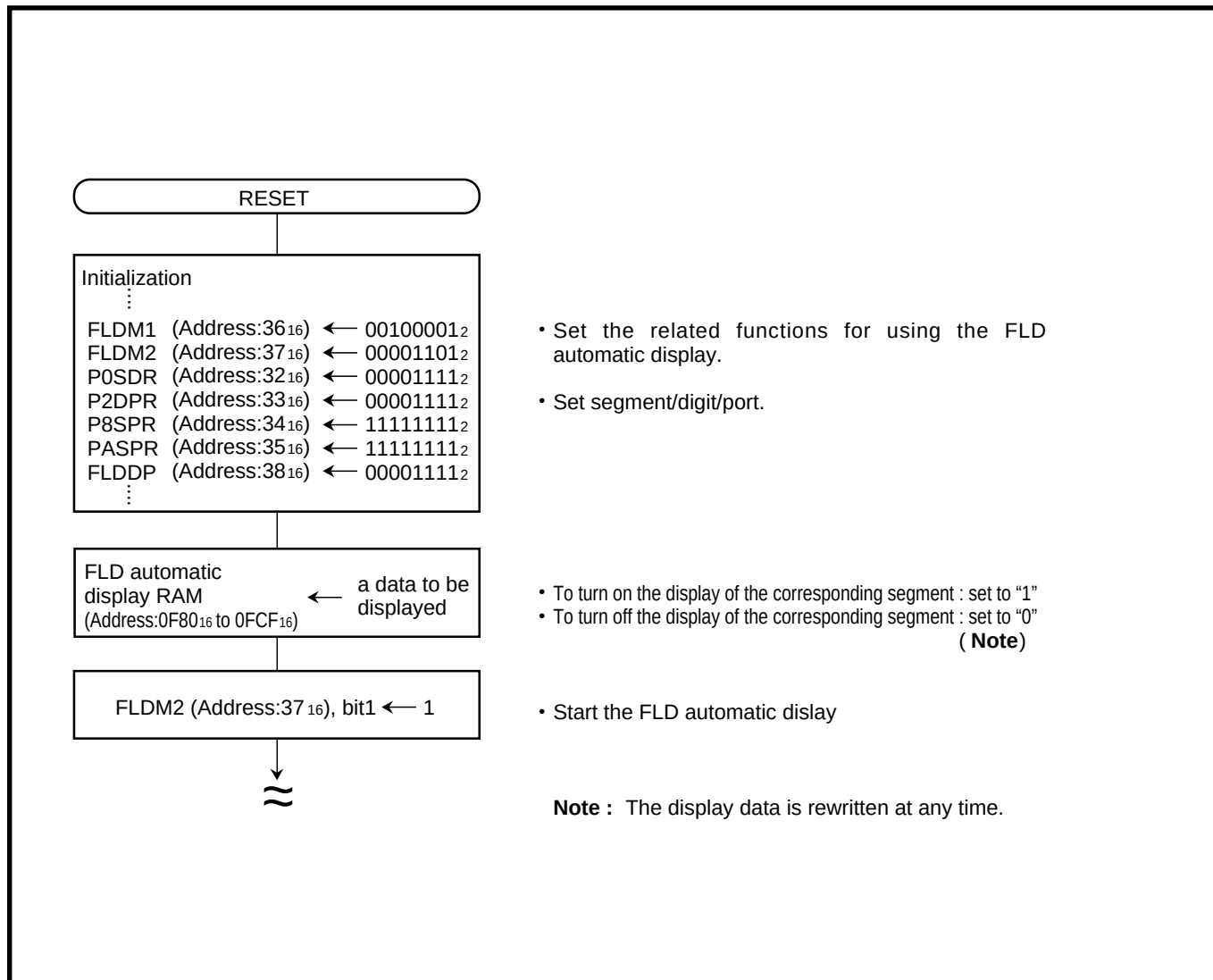


Fig. 2.5.38 Control procedure [5 × 7 dot display]

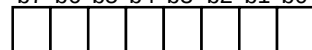
2. APPLICATION 2.6 Interrupt interval determination function

2.6 Interrupt interval determination function

2.6.1 Related registers

Interrupt interval determination register

b7 b6 b5 b4 b3 b2 b1 b0


Interrupt interval determination register (IID) [Address:30₁₆]

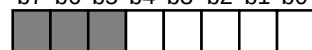
B	Function	At reset	R	W
0	This register stores the values obtained by counting the following interval with a counter sampling clock.	?	○	×
1		?	○	×
2	- Falling edge interval - Rising edge interval - Both-sided edge interval (selected by the interrupt edge selection register)	?	○	×
3		?	○	×
4		?	○	×
5	This register is read-only.	?	○	×
6		?	○	×
7		?	○	×

Note : When the noise filter sampling clock selection bits (bits 2 and 3) of the Interrupt interval determination control register (IIDCON) (Address: 31₁₆) is set to "00" (when no noise filter is used), the both-sided edge detection function is not available.

Fig. 2.6.1 Structure of Interrupt interval determination register

Interrupt interval determination control register

b7 b6 b5 b4 b3 b2 b1 b0


Interrupt interval determination control register (IIDCON) [Address:31₁₆]

B	Name	Function	At reset	R	W
0	Interrupt interval determination circuit operating selection bit	0 : Stopped 1 : Operating	0	○	○
1	Counter sampling clock selection bit	0 : $f(X_{IN})/256$ 1 : $f(X_{IN})/512$	0	○	○
2	Noise filter sampling clock selection bits (INT ₂)	00 : Filter stop	0	○	○
3		01 : $f(X_{IN})/64$ 10 : $f(X_{IN})/128$ 11 : $f(X_{IN})/256$			
4	One-sided/both-sided edge detection selection bit	0 : One-sided edge detection 1 : Both-sided edge detection (Note)	0	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."		0	○	×
6			0	○	×
7			0	○	×

Note : When the noise filter sampling clock selection bits (bits 2 and 3) of the Interrupt interval determination control register (IIDCON) (Address: 31₁₆) is set to "00" (when no noise filter is used), the both-sided edge detection function is not available.

Fig. 2.6.2 Structure of Interrupt interval determination control register

2. APPLICATION 2.6 Interrupt interval determination function

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0

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Interrupt edge selection register (INTEDGE) [Address:3A₁₆]

b	Name	Function	At reset	R	W
0	INT ₀ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
1	INT ₁ /ZCR interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
2	INT ₂ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
3	INT ₃ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
4	INT ₄ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
5	INT ₄ /A-D conversion interrupt switch bit	0 : INT ₄ interrupt 1 : A-D conversion interrupt	0	○	○
6	CNTR ₀ pin active edge switch bit	0 : Falling edge active 1 : Rising edge active	0	○	○
7	CNTR ₁ pin active edge switch bit	0 : Falling edge active 1 : Rising edge active	0	○	○

Fig. 2.6.3 Structure of Interrupt edge selection register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

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Interrupt request register 1 (IREQ1) [Address:3C₁₆]

B	Name	Function	At reset	R	W
0	INT ₀ interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	INT ₁ /ZCR interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	• INT ₂ interrupt request bit • Remote control/counter overflow interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	• Serial I/O 1 interrupt request bit • Serial I/O automatic transfer interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	Serial I/O 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	Serial I/O 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	Timer 1 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Timer 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*

* "0" is set by software, but not "1."

Fig. 2.6.4 Structure of Interrupt request register 1

2. APPLICATION

2.6 Interrupt interval determination function

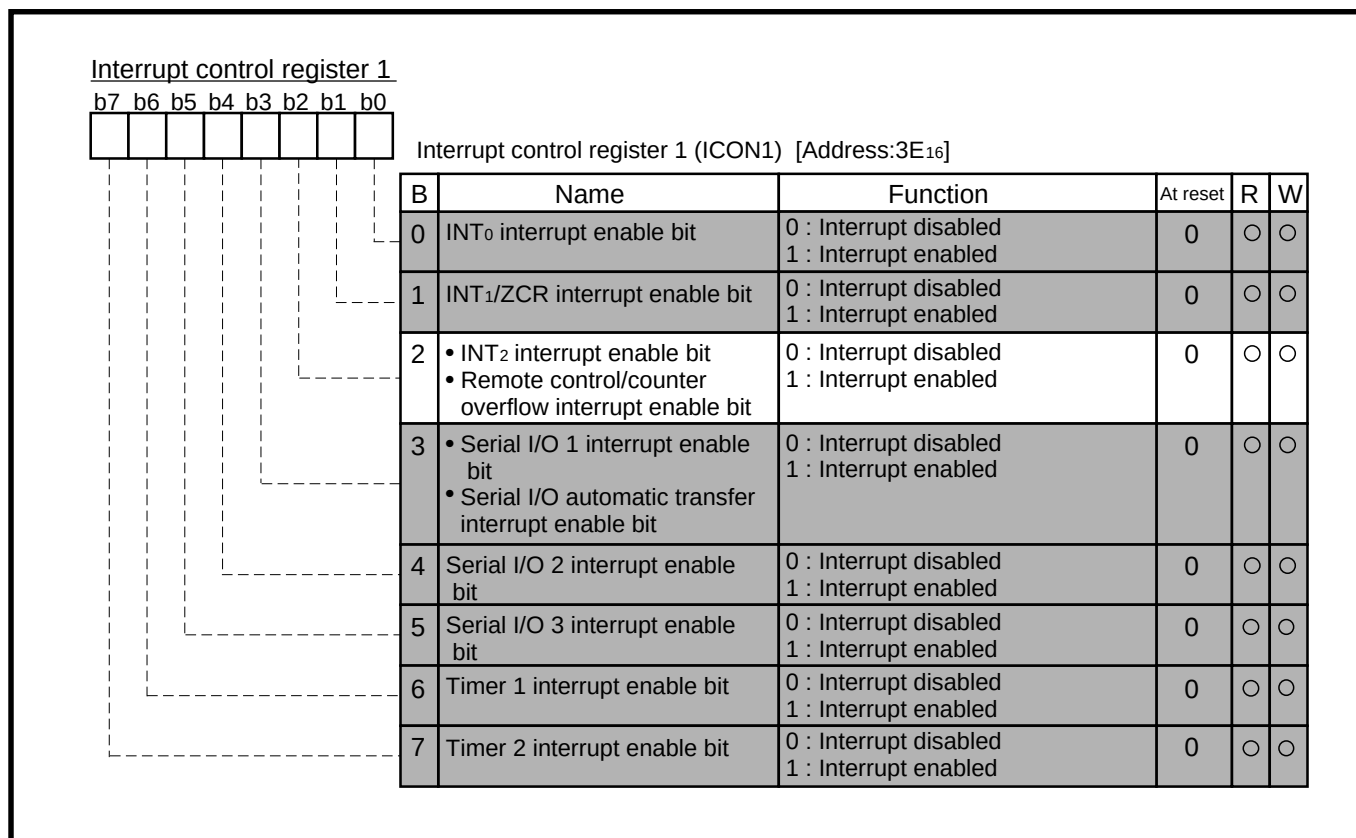


Fig. 2.6.5 Structure of Interrupt control register 1

2. APPLICATION

2.6 Interrupt interval determination function

2.6.2 Interrupt interval determination function

Reception of remote-control signal

Outline : Remote-control signal is read in by both of the interrupt interval determination function using a noise filter and a timer interrupt.

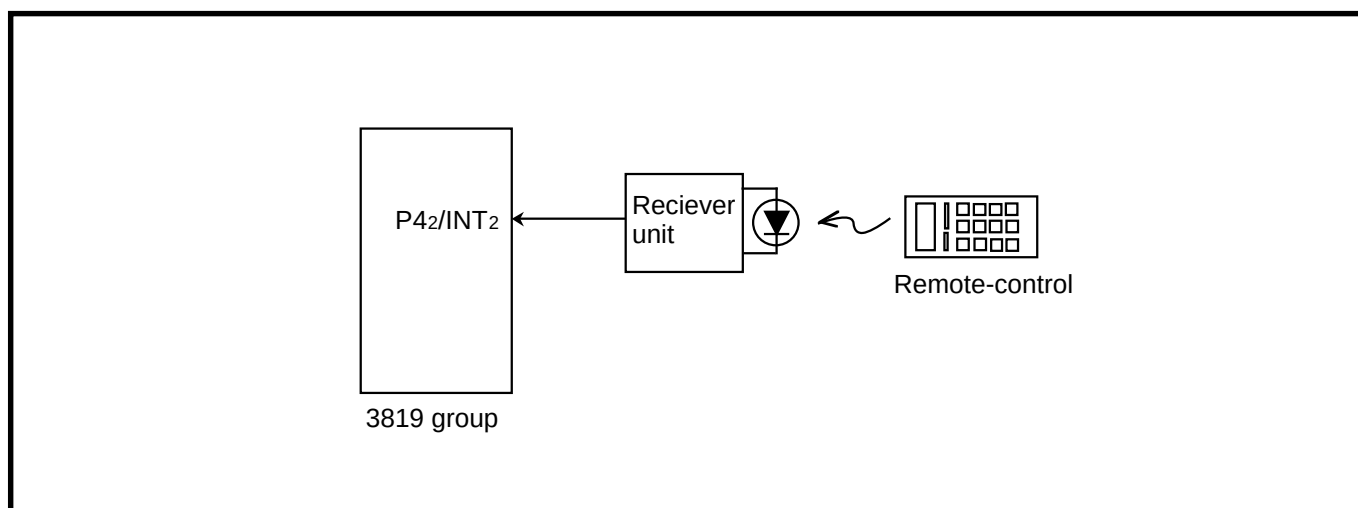


Fig. 2.6.6 Connection diagram [Reception of remote-control signal]

- Specifications :**
- Operation at $f(XIN) = 8 \text{ MHz}$ in the high-speed mode.
 - The one-sided edge interval is measured.
 - The noise filter is used.
 - The remote control interrupt request is checked within the timer 2 interrupt (488 μs cycle) processing routine.

Figure 2.6.7 shows a function block diagram, and Figure 2.6.8 shows a timing chart of data determination.

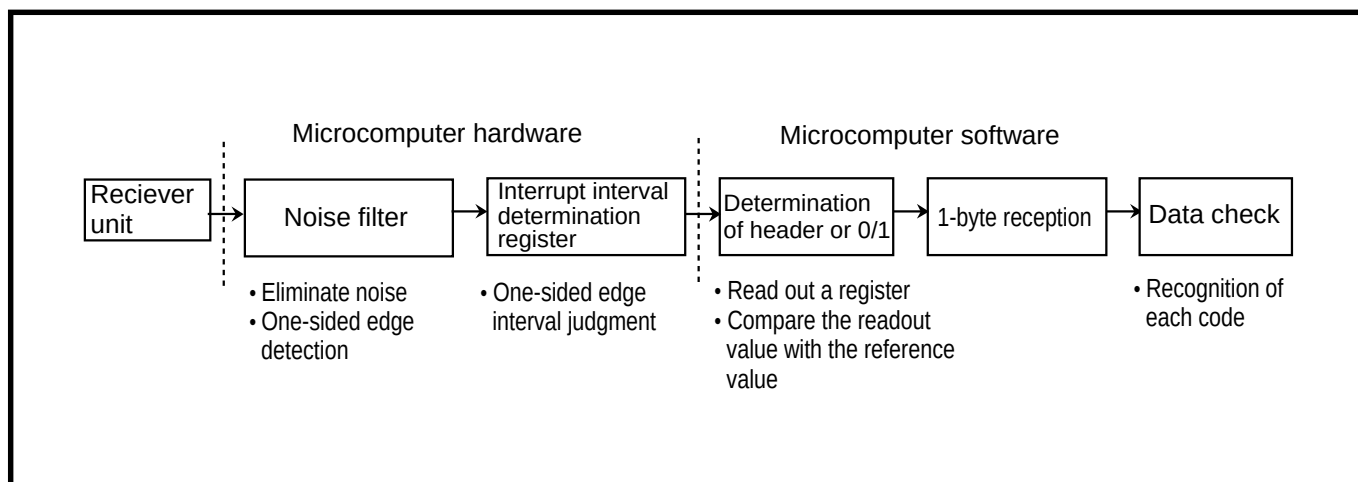


Fig. 2.6.7 Function block diagram [Reception of remote-control signal]

2. APPLICATION

2.6 Interrupt interval determination function

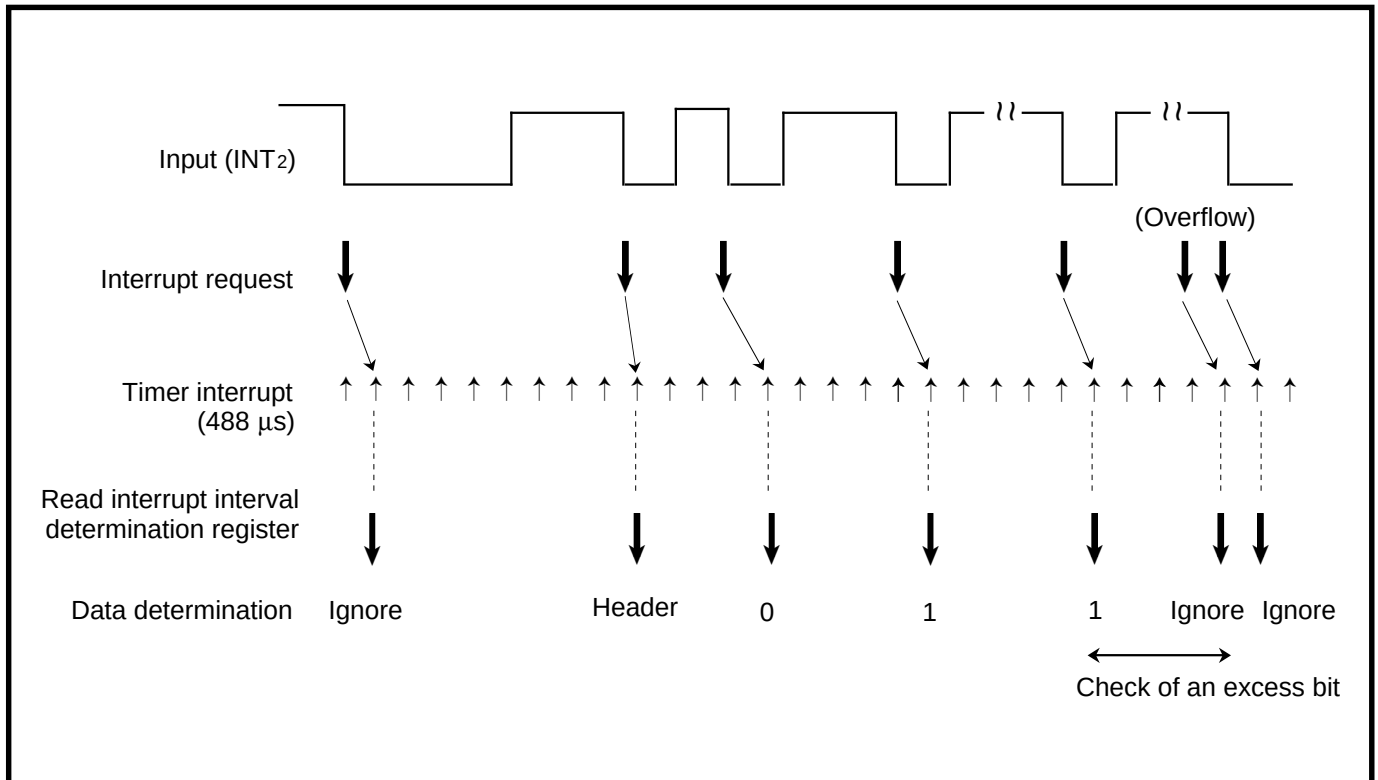


Fig. 2.6.8 Timing chart of data determination

2. APPLICATION

2.6 Interrupt interval determination function

Figure 2.6.9 shows a setting of related registers.

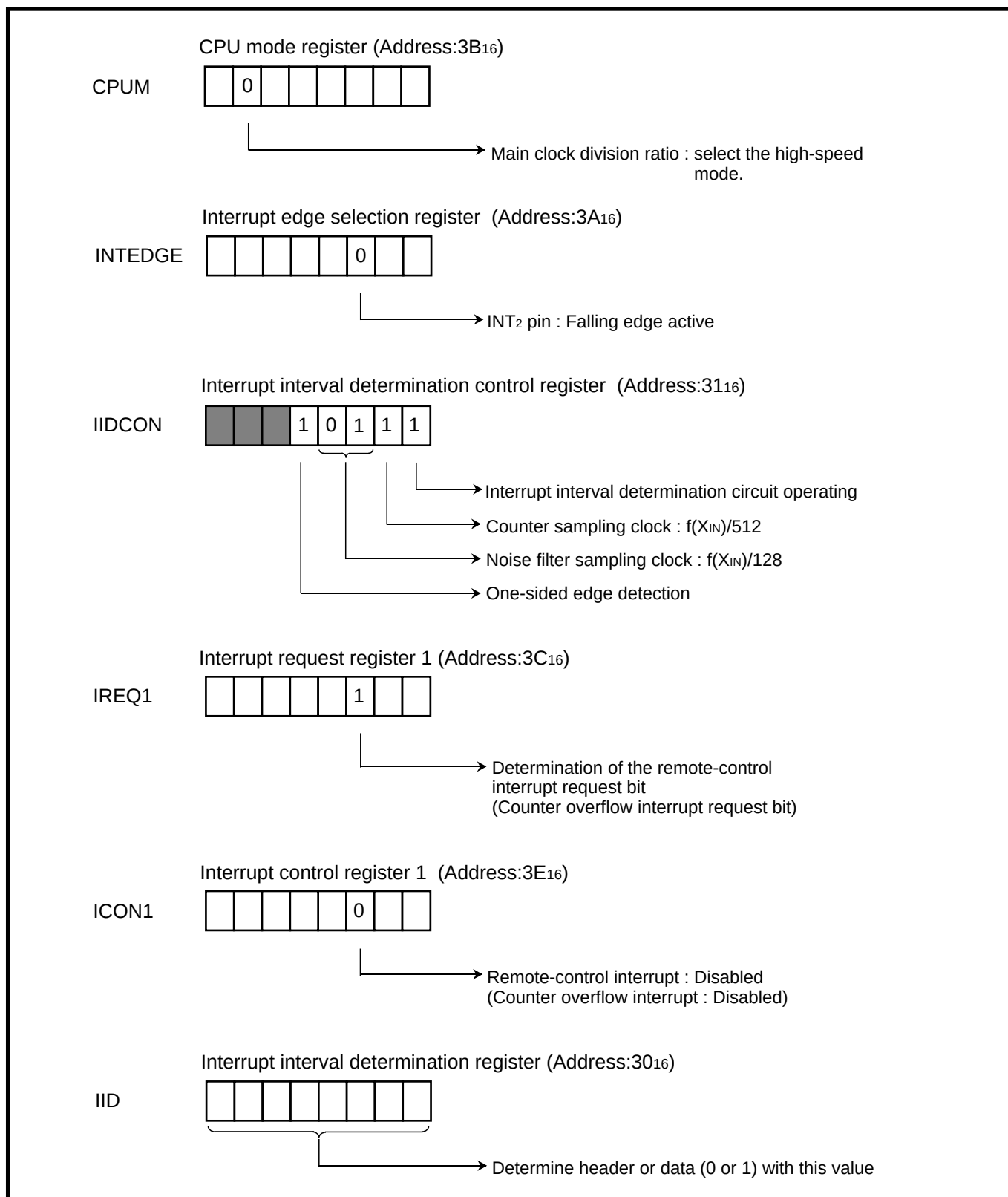


Fig. 2.6.9 Setting of related registers [Reception of remote-control signal]

2. APPLICATION

2.6 Interrupt interval determination function

Control procedure : When the registers are set as shown in Figure 2.6.9, remote-control signals are receivable. Figure 2.6.10 shows a control procedure and Figure 2.6.11 shows reception of remote-control signal (Timer 2 interrupt).

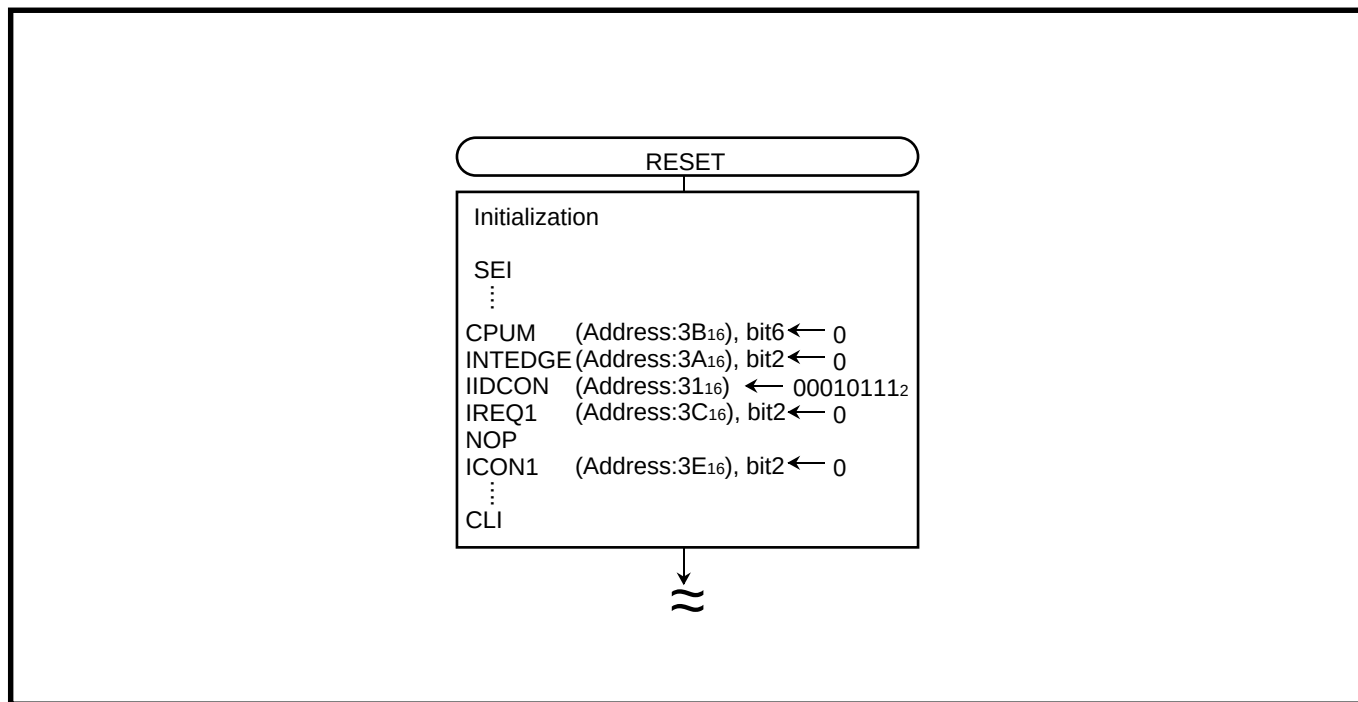


Fig. 2.6.10 Control procedure (1) [Reception of remote-control signal]

2. APPLICATION

2.6 Interrupt interval determination function

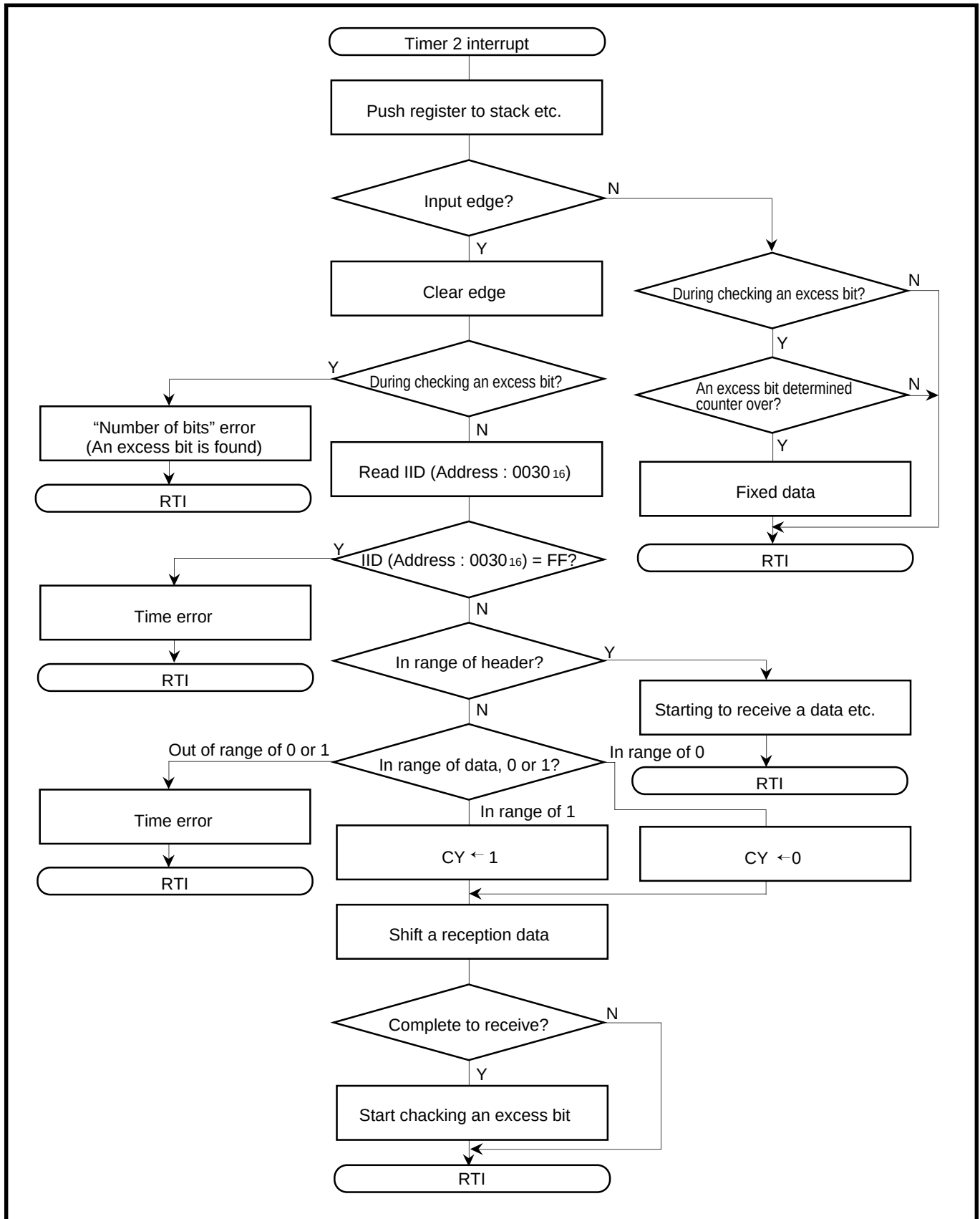


Fig. 2.6.11 Control procedure (2) [Reception of remote-control signal] (Timer 2 interrupt)

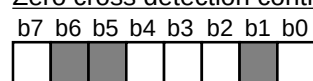
2. APPLICATION

2.7 Zero cross detection circuit

2.7 Zero cross detection circuit

2.7.1 Related registers

Zero cross detection control register



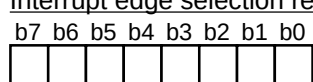
Zero cross detection control register (ZCRCON) [Address:39₁₆]

B	Name	Function	At reset	R	W
0	Zero cross detection ON/OFF selection bit	0 : Without passing through zero cross detection comparator 1 : Passing through zero cross detection comparator	0	○	○
1	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
2	Noise filter sampling clock selection bits (INT ₁)	b3 b2 : Note use noise filter 00 : f(X _{IN})/64 or f(X _{CIN})/64 01 : f(X _{IN})/128 or f(X _{CIN})/128 10 : f(X _{IN})/256 or f(X _{CIN})/256 11 : f(X _{IN})/256 or f(X _{CIN})/256	0	○	○
3			0	○	○
4	One-sided/both-sided edge detection selection bit	0 : One-sided edge detection 1 : Both-sided edges detection (Note)	0	○	○
5	Nothing is allocated for these bits. These are write disabled bits.		0	○	×
6	When these bits are read out, the values are "0."			○	×
7	Zero cross detection circuit input bit (read-only)	0 : Less than 0 V 1 : 0 V or more	0	○	×

Note : When the noise filter sampling clock selection bits (bits 2 and 3) of the Zero cross detection control register (ZCRCON) (Address: 39₁₆) is set to "00" (when no noise filter is used), the both-sided edge detection function is not available.

Fig. 2.7.1 Structure of Zero cross detection control register

Interrupt edge selection register



Interrupt edge selection register (INTEDGE) [Address:3A₁₆]

b	Name	Function	At reset	R	W
0	INT ₀ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
1	INT ₁ /ZCR interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
2	INT ₂ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
3	INT ₃ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
4	INT ₄ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
5	INT ₄ /A-D conversion interrupt switch bit	0 : INT ₄ interrupt 1 : A-D conversion interrupt	0	○	○
6	CNTR ₀ pin active edge switch bit	0 : Falling edge active 1 : Rising edge active	0	○	○
7	CNTR ₁ pin active edge switch bit	0 : Falling edge active 1 : Rising edge active	0	○	○

Fig. 2.7.2 Structure of Interrupt edge selection register

2. APPLICATION

2.7 Zero cross detection circuit

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0



Interrupt request register 1 (IREQ1) [Address:3C16]

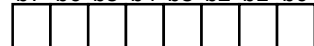
B	Name	Function	At reset	R	W
0	INT ₀ interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	INT ₁ /ZCR interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	• INT ₂ interrupt request bit • Remote control/counter overflow interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	• Serial I/O 1 interrupt request bit • Serial I/O automatic transfer interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	Serial I/O 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	Serial I/O 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	Timer 1 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Timer 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*

* "0" is set by software, but not "1."

Fig. 2.7.3 Structure of Interrupt request register 1

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0



Interrupt control register 1 (ICON1) [Address:3E16]

B	Name	Function	At reset	R	W
0	INT ₀ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT ₁ /ZCR interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	• INT ₂ interrupt enable bit • Remote control/counter overflow interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	• Serial I/O 1 interrupt enable bit • Serial I/O automatic transfer interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Serial I/O 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Serial I/O 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 2.7.4 Structure of Interrupt control register 1

2. APPLICATION

2.7 Zero cross detection circuit

2.7.2 Connection example of Zero cross detection circuit

Figure 2.7.5 shows a connection example of the Zero cross detection circuit.

R1 is a current limiting resistor. Determine its value according to the current standard of the clamp diode. In this case, the AC input is not the effective value of 100 V but is the peak value of 140 V.

R2 is a noise elimination resistor. Connect a resistor of about 1 k Ω near the port.

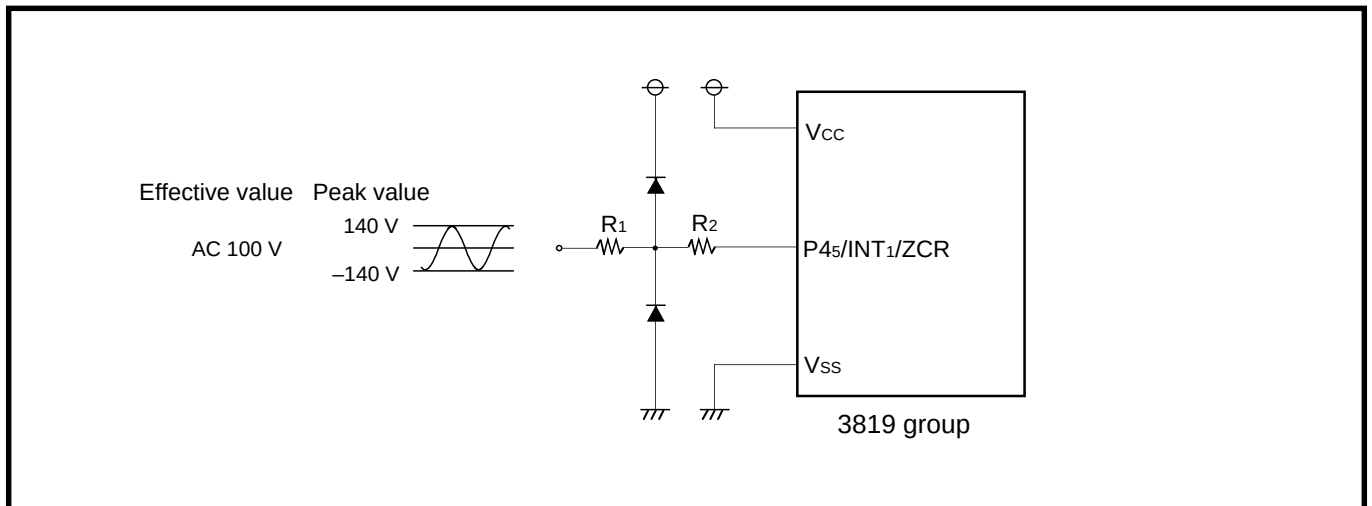


Fig. 2.7.5 Connection example of Zero cross detection circuit

2. APPLICATION

2.7 Zero cross detection circuit

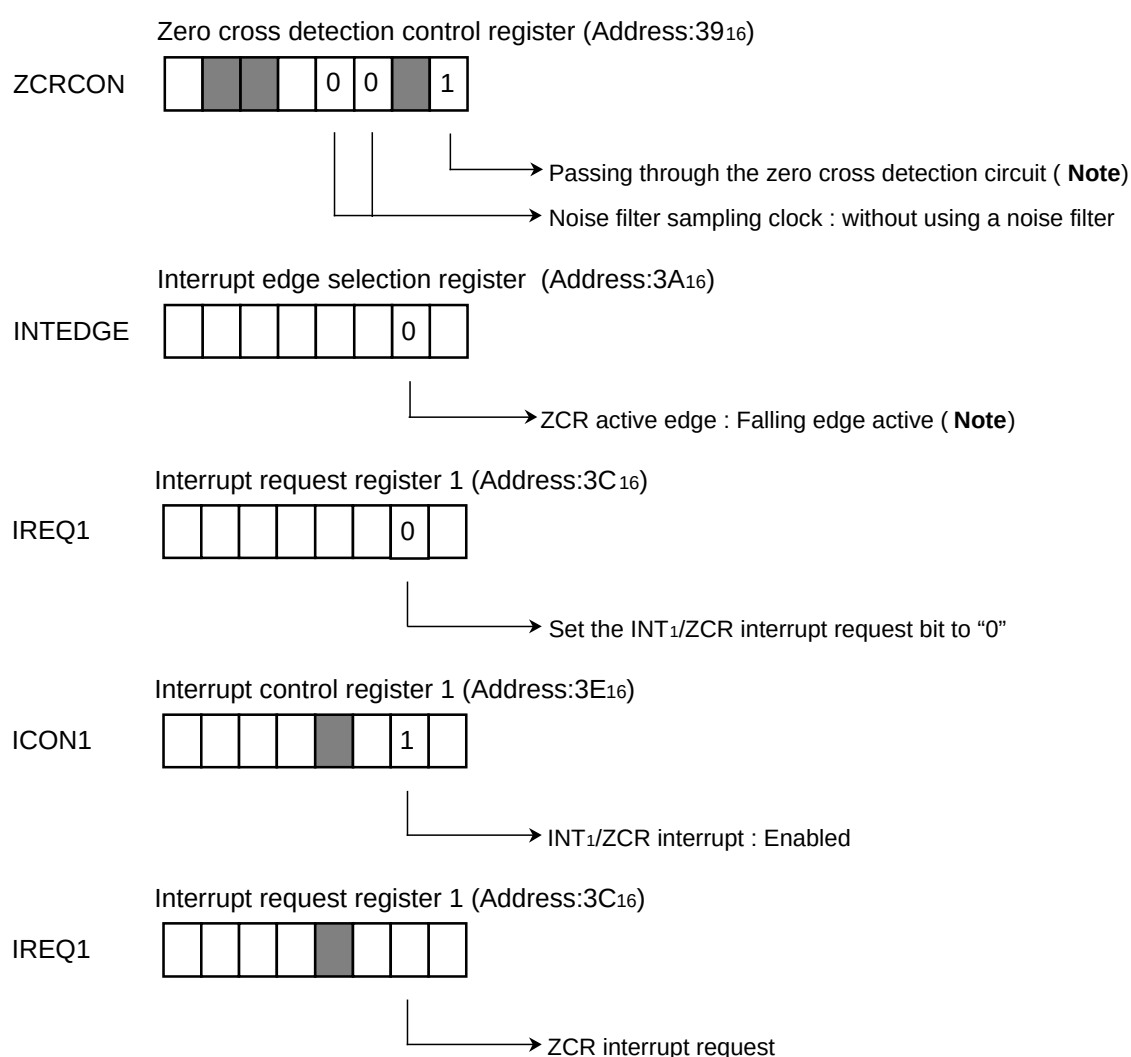
2.7.3 Zero cross detection circuit application example 1

Clock count using ZCR interrupt (without using a noise filter)

Outline : The clock is counted up every second by using the ZCR interrupts.

- Specifications :**
- The noise filter is not used.
 - The commercial frequency (50 Hz or 60 Hz) is input.
 - The clock is counted up by using the ZCR interrupts.

Figure 2. 7. 6 shows a setting of related registers.



Note : When changing the values of bit 0 of the zero cross detection control register and bit 1 of the interrupt edge selection register, make sure the following contents.

1. During changeing, set bit 1 of the interrupt control register 1 to "0".
2. After changeing, set bit 1 of the interrupt request register 1 to "0".

Fig. 2.7.6 Setting of related registers [Clock count using ZCR interrupt (without using a noise filter)]

2. APPLICATION

2.7 Zero cross detection circuit

- Control procedure :**
- ① Set the related registers according to Figure 2.7.6.
 - ② At the falling edge of the commercial frequency (50 Hz or 60 Hz), the ZCR interrupt occurs.
 - ③ The clock is counted up every second in the ZCR interrupt processing routine.

Figure 2.7.7 shows a control procedure.

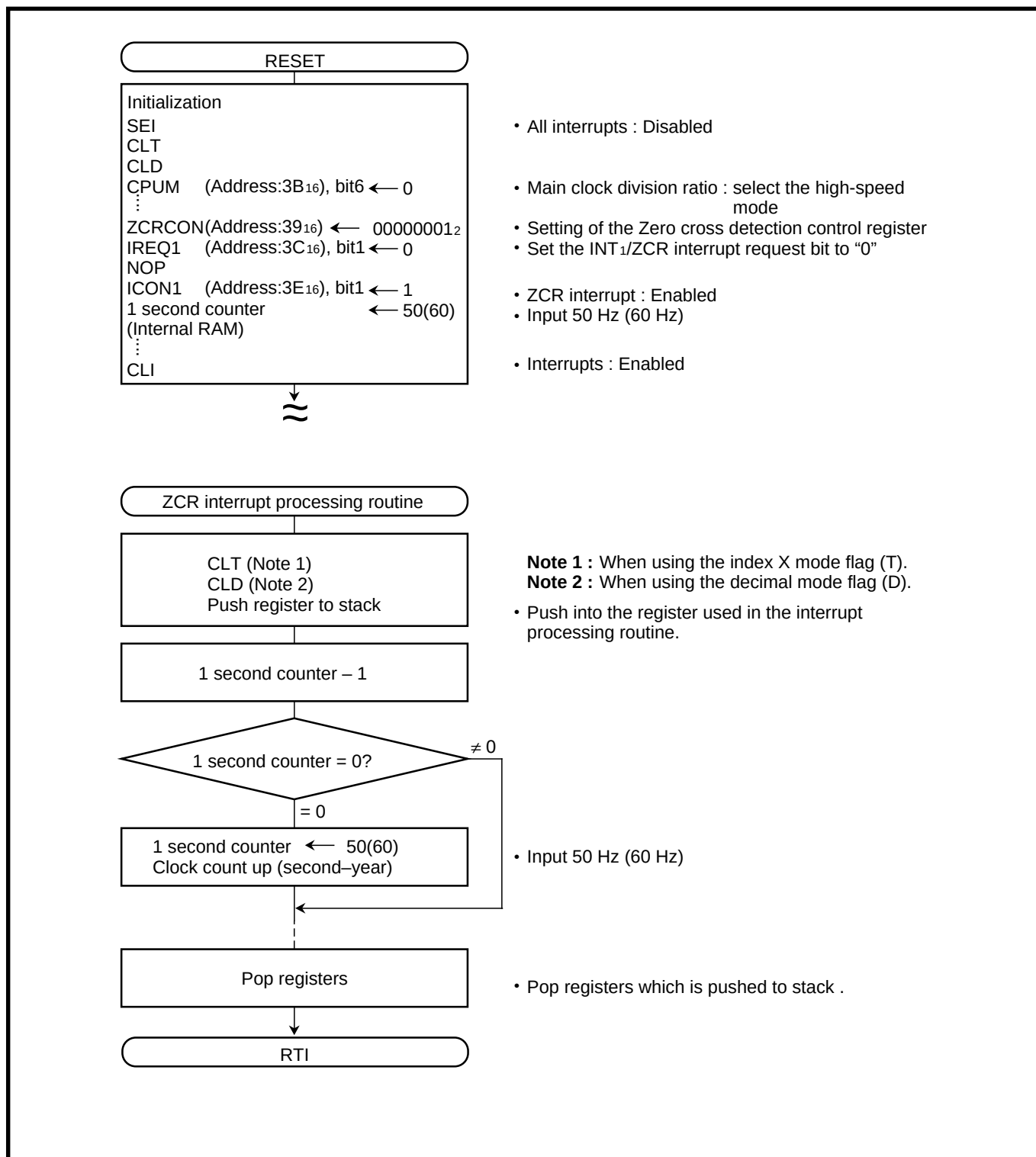


Fig. 2.7.7 Control procedure [Clock count using ZCR interrupt (without using a noise filter)]

2. APPLICATION

2.7 Zero cross detection circuit

2.7.4 Zero cross detection circuit application example 2

Clock count using ZCR interrupt (using a noise filter)

Outline : The clock is counted up every second by using the ZCR interrupts.

- Specifications :**
- $f(X_{IN})=4\text{ MHz}$
 - The noise filter (sampling clock : $f(X_{IN})/256$) is used.
(Pulse less than $64\text{ }\mu\text{s}$ is eliminated as a noise.)
 - The commercial frequency (50 Hz or 60 Hz) is input.
 - The clock is counted up by using the ZCR interrupts.

Figure 2.7.8 shows a setting of related registers.

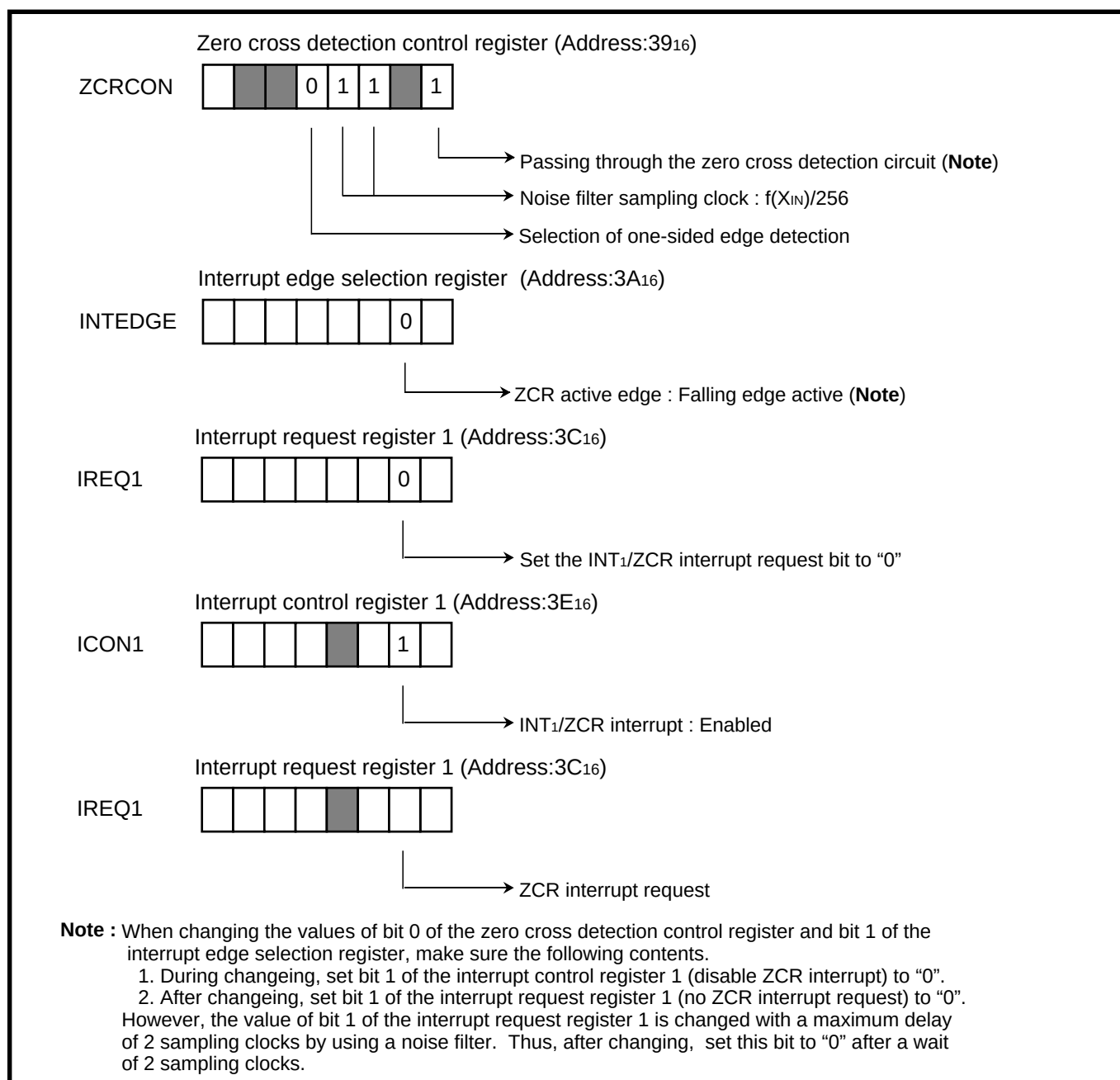


Fig. 2.7.8 Setting of related registers [Clock count using ZCR interrupt (using a noise filter)]

2. APPLICATION

2.7 Zero cross detection circuit

- Control procedure :**
- ① Set the related registers according to Figure 2.7.8.
 - ② At the falling edge of the commercial frequency (50 Hz or 60 Hz), the ZCR interrupt occurs.
 - ③ The clock is counted up every second in the ZCR interrupt processing routine.

Figure 2.7.9 shows a control procedure.

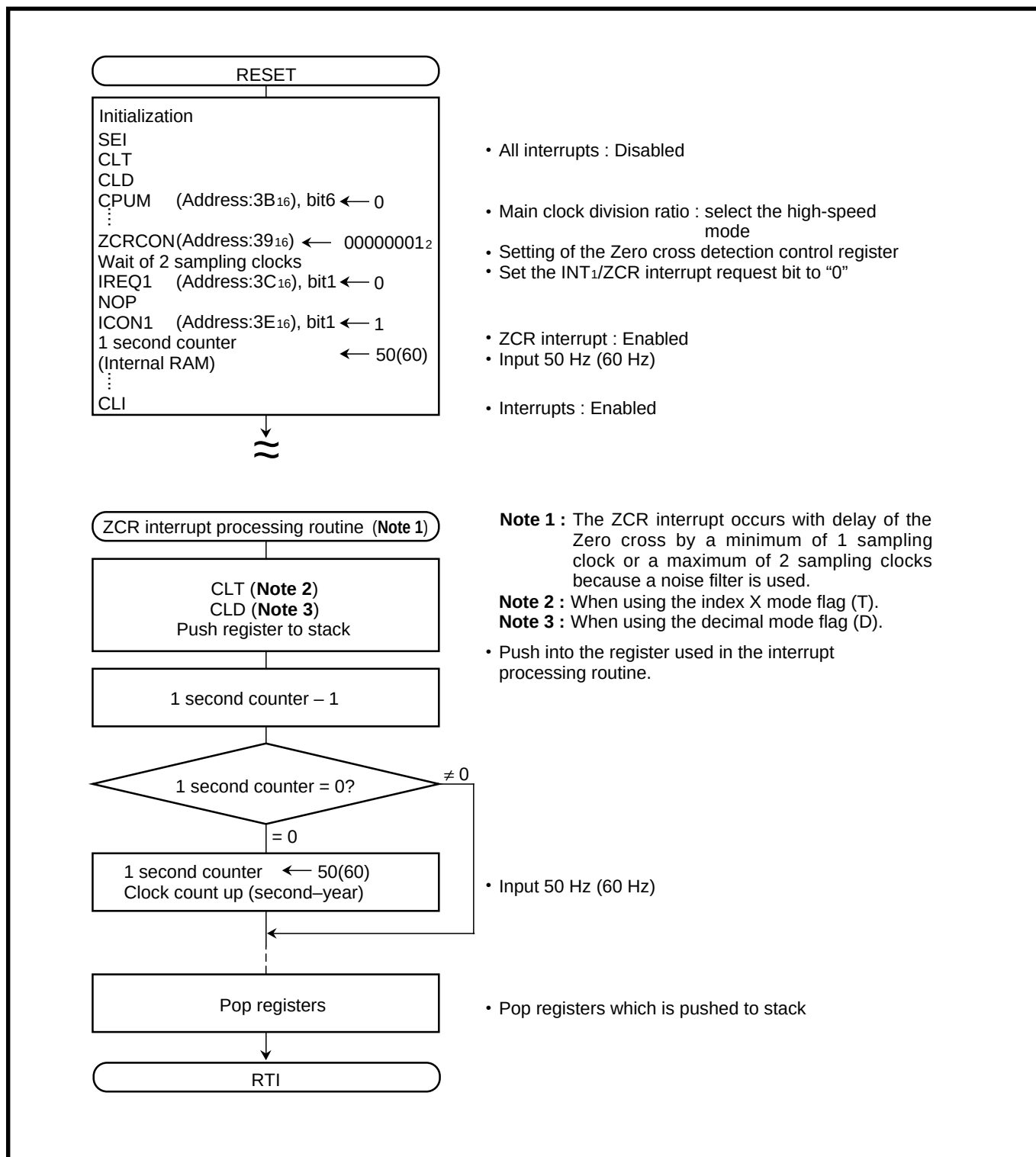


Fig. 2.7.9 Control procedure [Clock count using ZCR interrupt (using a noise filter)]

2. APPLICATION

2.8 Reset

2.8.1 Connection example of reset IC

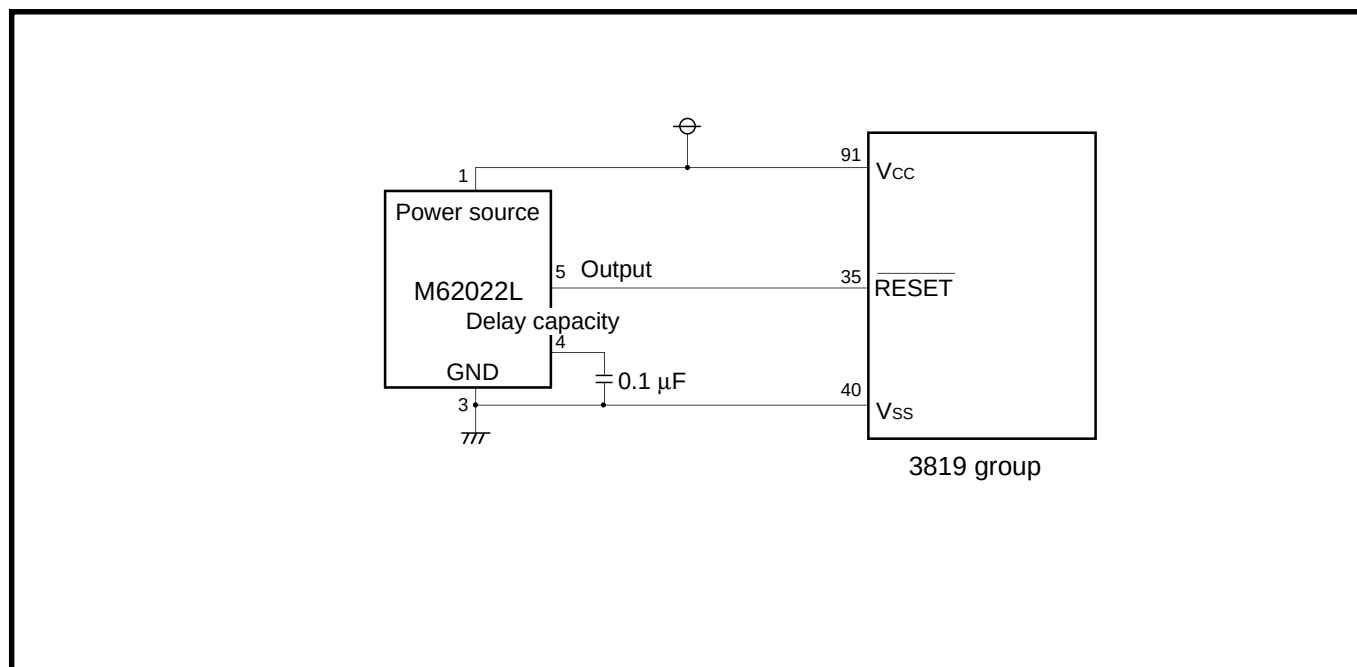


Fig. 2.8.1 Example of Poweron reset circuit

Figure 2.8.2 shows the system example which switch to the RAM backup mode by detecting a drop of the system power source voltage with the INT interrupt.

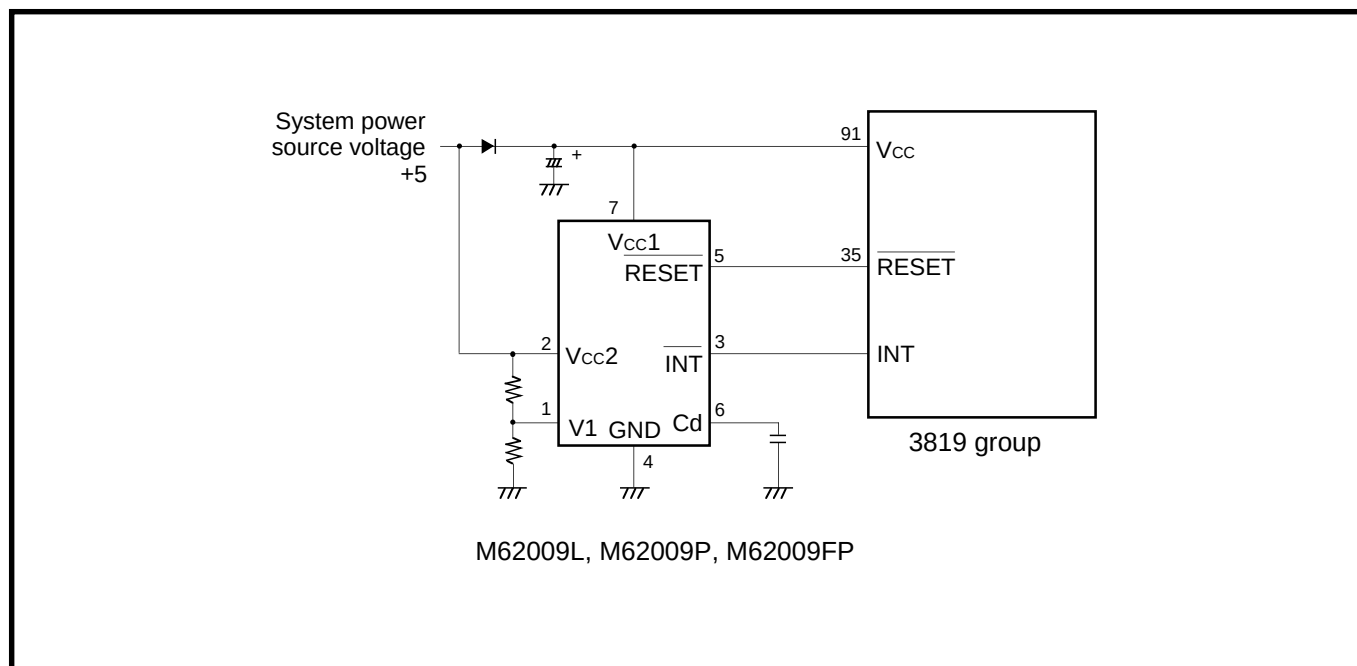


Fig. 2.8.2 RAM back-up system

2. APPLICATION

2.9 Clock generating circuit

2.9 Clock generating circuit

2.9.1 Related registers

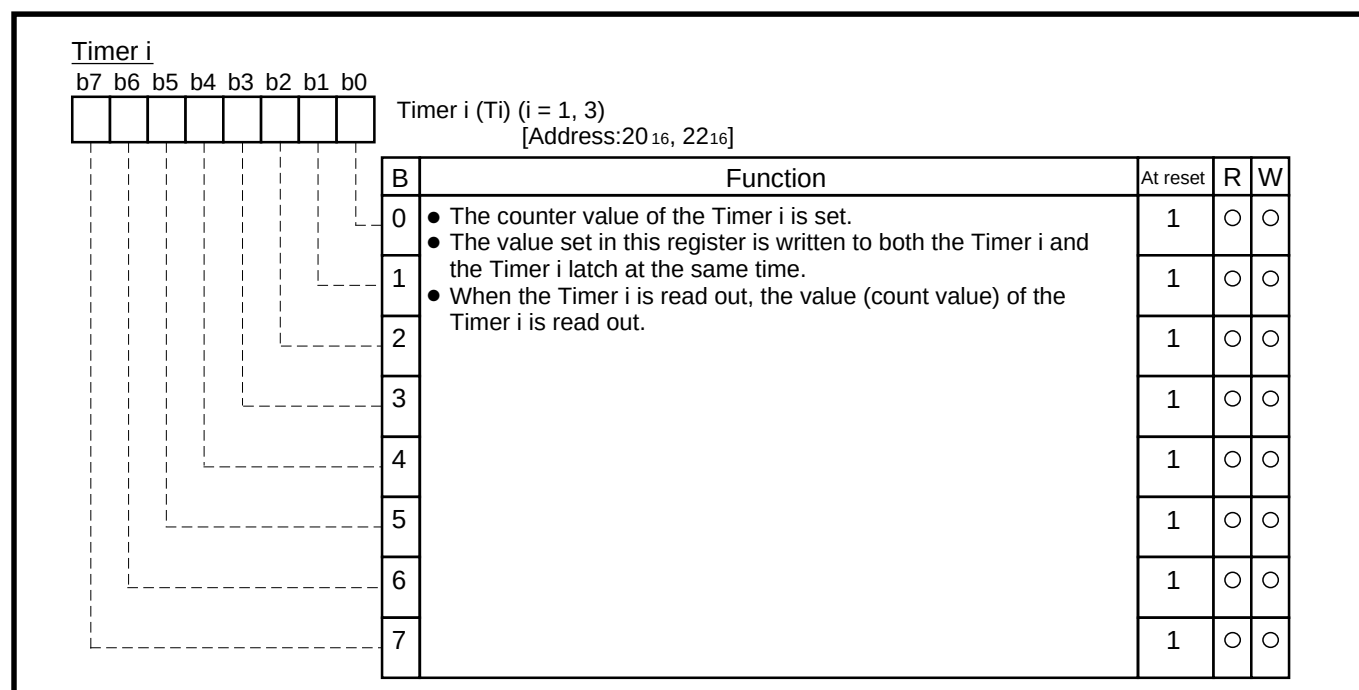


Fig. 2.9.1 Structure of Timer i (i = 1, 3)

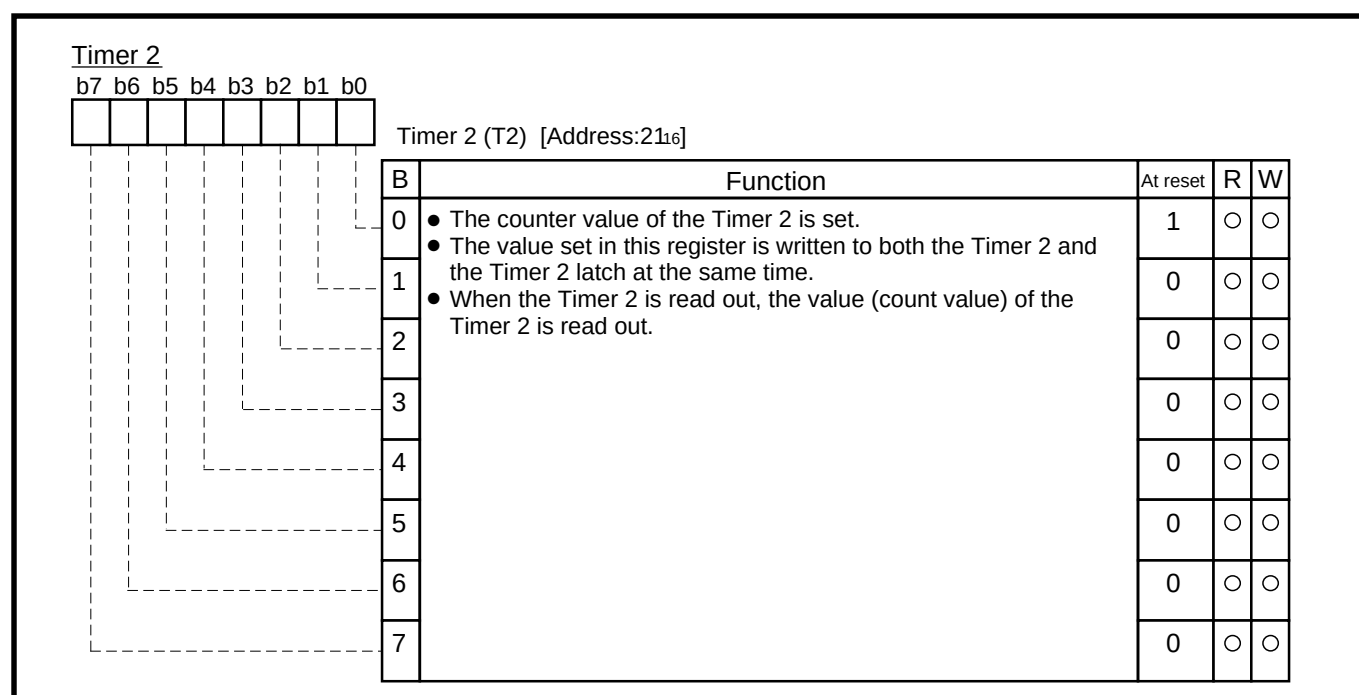


Fig. 2.9.2 Structure of Timer 2

2. APPLICATION

2.9 Clock generating circuit

Timer 12 mode register

b7 b6 b5 b4 b3 b2 b1 b0



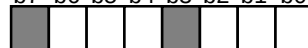
Timer 12 mode register (T12M) [Address:28₁₆]

B	Name	Function	At reset	R	W
0	Timer 1 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 2 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 1 count source selection bit	0 : $f(X_{IN})/16$ or $f(X_{CIN})/16$ 1 : $f(X_{CIN})$	0	○	○
3	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
4	Timer 2 count source selection bits	b5 b4 00 : Timer 1 underflow	0	○	○
5		01 : $f(X_{CIN})$ 10 : External count input CNTR ₀ 11 : Not available	0	○	○
6	Timer 1 output selection bit (P4 ₆)	0 : I/O port 1 : Timer 1 output	0	○	○
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×

Fig. 2.9.3 Structure of Timer 12 mode register

Timer 34 mode register

b7 b6 b5 b4 b3 b2 b1 b0



Timer 34 mode register (T34M) [Address:29₁₆]

B	Name	Function	At reset	R	W
0	Timer 3 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 4 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 3 count source selection bit	0 : $f(X_{IN})/16$ or $f(X_{CIN})/16$ 1 : Timer 2 underflow	0	○	○
3	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
4	Timer 4 count source selection bits	b5 b4 00 : $f(X_{IN})/16$ or $f(X_{CIN})/16$	0	○	○
5		01 : Timer 3 underflow 10 : External count input CNTR ₁ 11 : Not available	0	○	○
6	Timer 3 output selection bit (P4 ₇)	0 : I/O port 1 : Timer 3 output	0	○	○
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×

Fig. 2.9.4 Structure of Timer 34 mode register

2. APPLICATION

2.9 Clock generating circuit

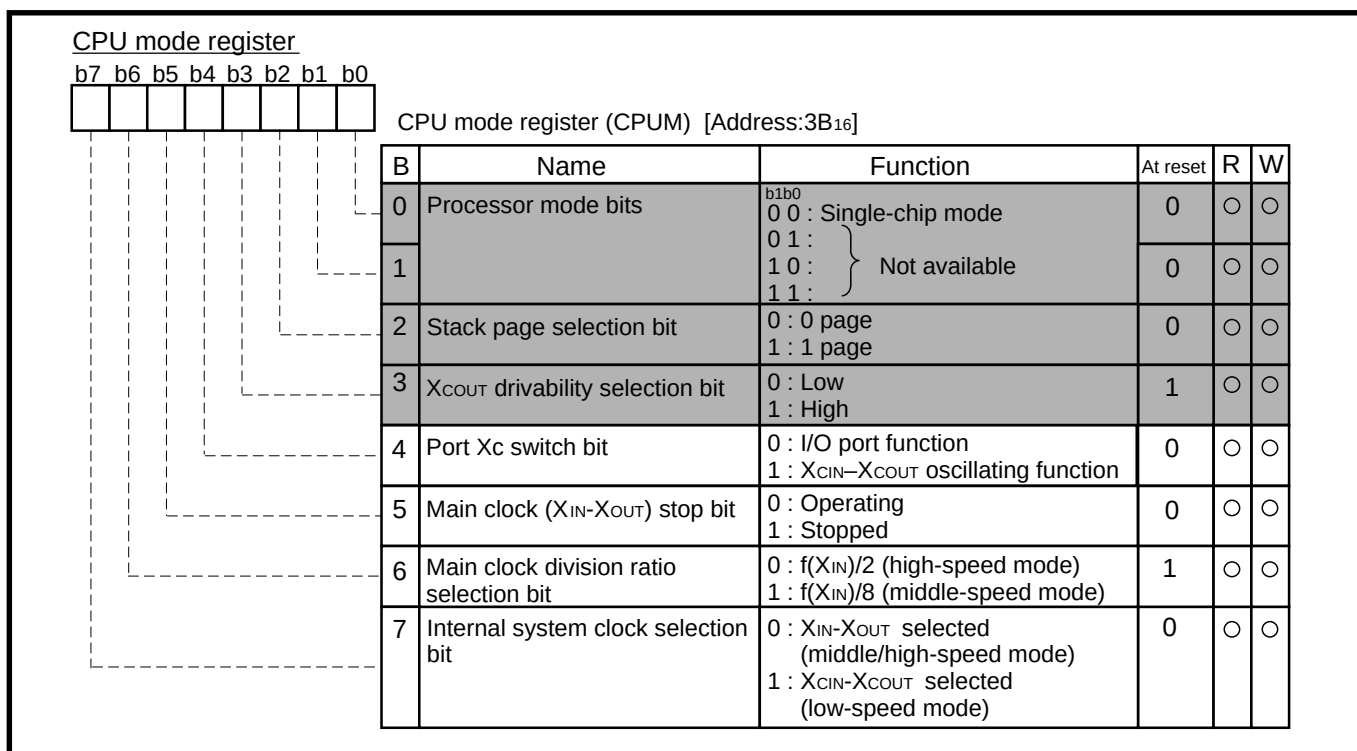


Fig. 2.9.5 Structure of CPU mode register

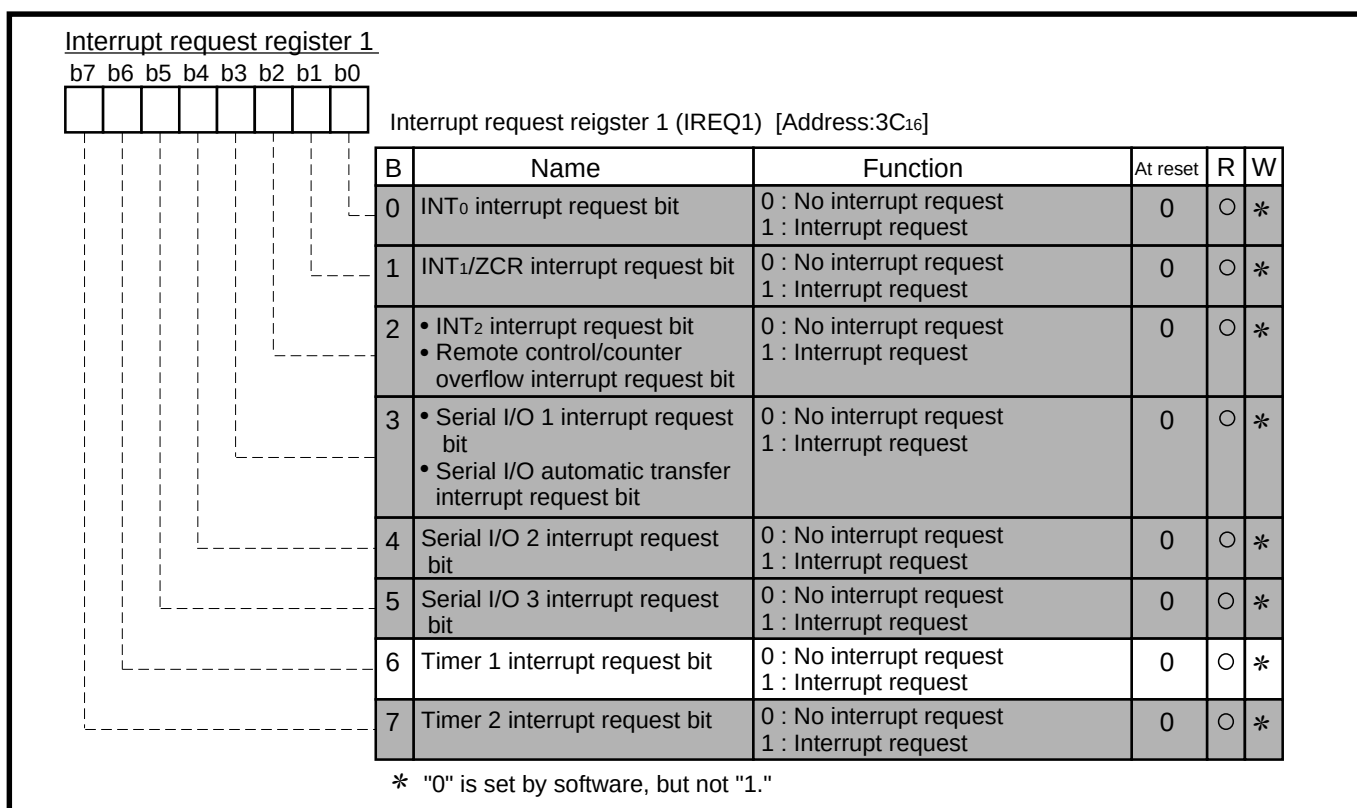


Fig. 2.9.6 Structure of Interrupt request register 1

2. APPLICATION

2.9 Clock generating circuit

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0



Interrupt request register 2 (IREQ2) [Address:3D16]

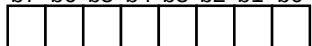
b	Name	Function	At reset	R	W
0	Timer 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	Timer 4 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	Timer 5 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	Timer 6 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	INT ₃ interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	• INT ₄ interrupt request bit • A-D conversion interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	• FLD blanking interrupt request bit • FLD digit interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	*

* "0" is set by software, but not "1."

Fig. 2.9.7 Structure of Interrupt request register 2

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0



Interrupt control register 1 (ICON1) [Address:3E16]

B	Name	Function	At reset	R	W
0	INT ₀ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT ₁ /ZCR interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	• INT ₂ interrupt enable bit • Remote control/counter overflow interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	• Serial I/O 1 interrupt enable bit • Serial I/O automatic transfer interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Serial I/O 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Serial I/O 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 2.9.8 Structure of Interrupt control register 1

2. APPLICATION

2.9 Clock generating circuit

Interrupt control register 2

b7 b6 b5 b4 b3 b2 b1 b0

0							
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Interrupt control register 2 (ICON2) [Address:3F16]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Timer 4 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Timer 5 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Timer 6 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT ₃ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	• INT ₄ interrupt enable bit • A-D conversion interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	• FLD blanking interrupt enable bit • FLD digit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix this bit to "0."		0	○	○

Fig. 2.9.9 Structure of Interrupt control register 2

2. APPLICATION

2.9 Clock generating circuit

2.9.2 Clock generating circuit application examples

(1) Status transition upon a power failure

Outline : The clock is counted up every second by using the timer interrupt during a power failure.

Specifications :

- Keep a power consumption as low as possible while maintaining a clock function.
- $f(X_{IN}) = 4.19 \text{ MHz}$, $f(X_{CIN}) = 32.768 \text{ kHz}$
- Port processing
Input port : Fix to "H" or "L" level in the external unit.
Output port : Fix to an output level which does not cause a current flow to the external unit.

Output port : Fix to an output level which does not cause a current flow to the external unit.

[Example]

When a circuit turns on LED at "L" output level, fix the output level to "H."

I/O port : Input port — Fix to "H" or "L" level in the external unit .

Output port — Output the data which does not consume current.

VREF : Supplying to the Reference voltage input pin is stopped by the external circuit.

P45/ZCR (using as the input port) : Fix to "H" level in the external unit .

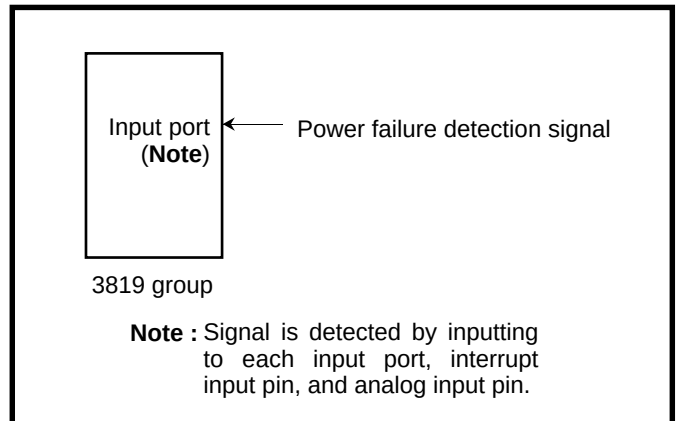


Fig. 2.9.10 Connection diagram

[Status transition upon a power failure]

Figure 2.9.11 shows a status transition diagram upon a power failure, Figure 2.9.12 shows a setting of related registers, and Figure 2.9.13 shows a control procedure.

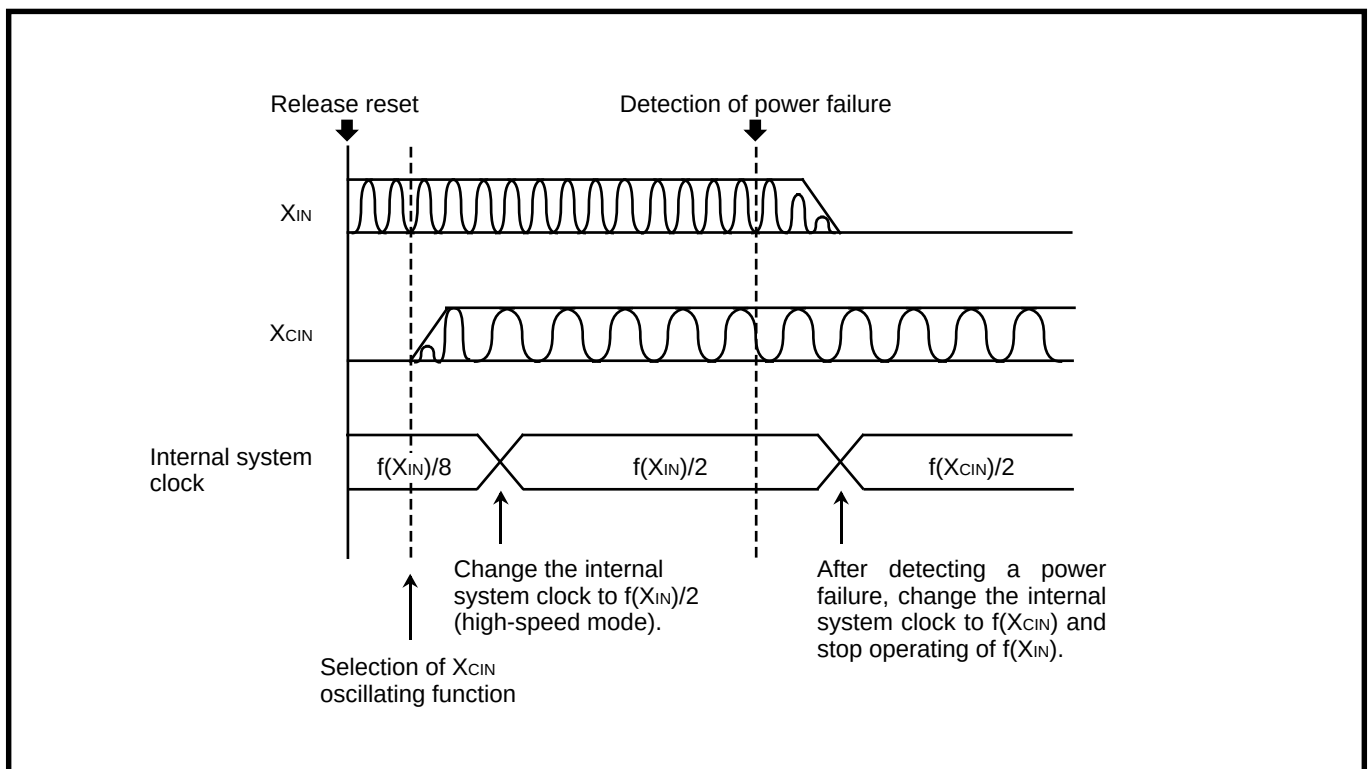


Fig. 2.9.11 Status transition diagram upon a power failure

2. APPLICATION

2.9 Clock generating circuit

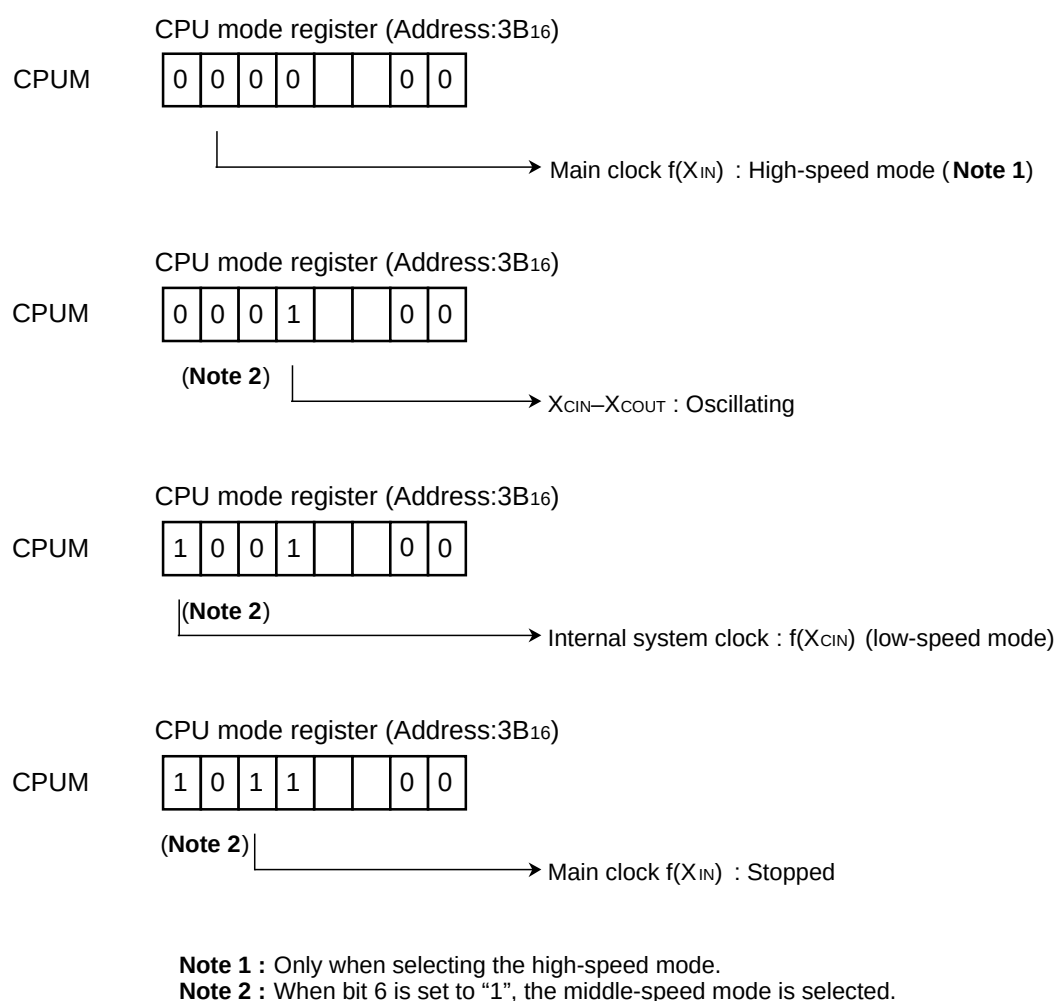


Fig. 2.9.12 Setting of related registers [Status transition upon a power failure]

2. APPLICATION

2.9 Clock generating circuit

Control procedure : Set the related registers in the order shown below to prepare for a power failure.

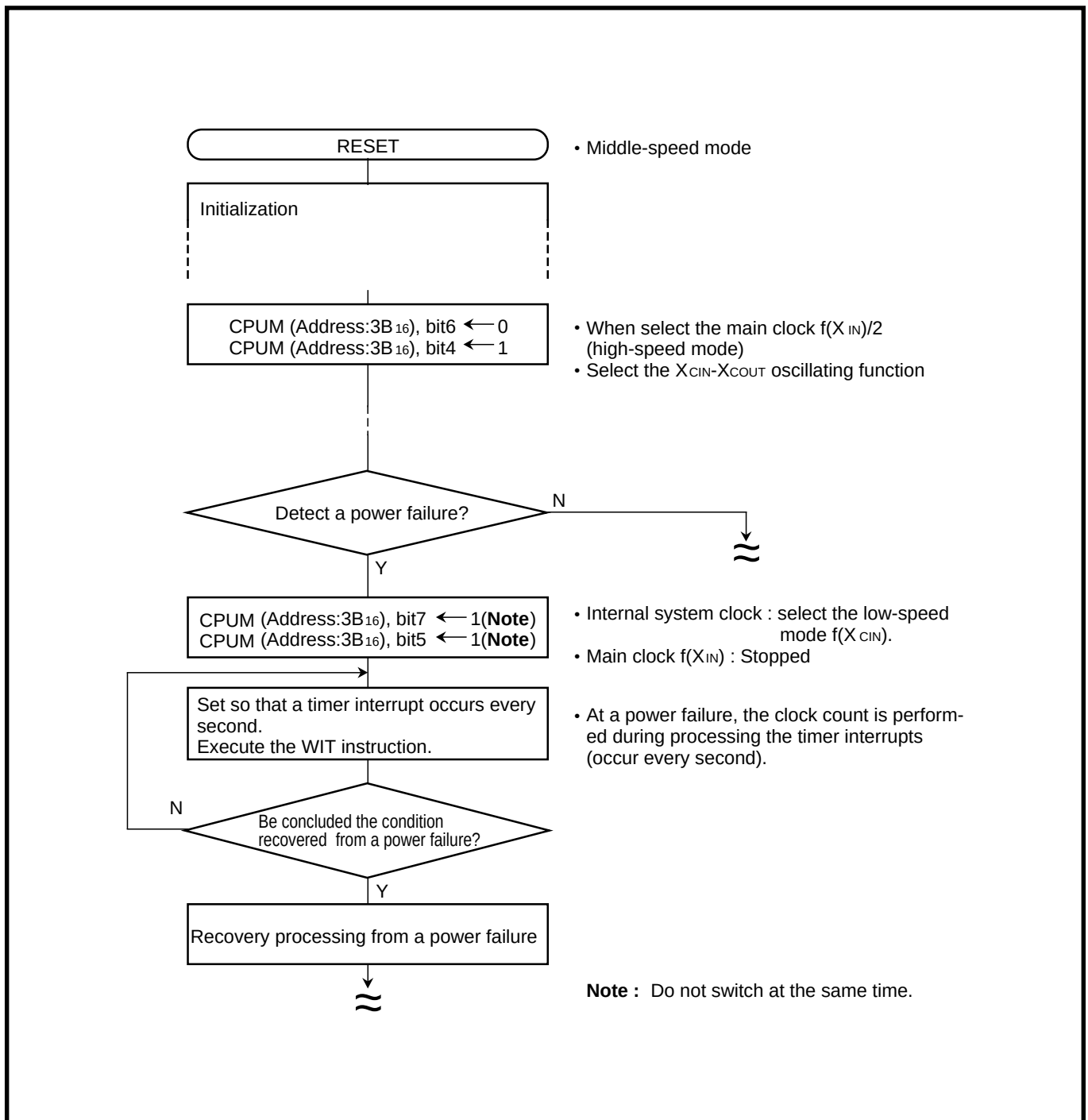


Fig. 2.9.13 Control procedure [Status transition upon a power failure]

2. APPLICATION

2.9 Clock generating circuit

(2) Counting without clock error during a power failure

Outline : It keeps counting without clock errors during a power failure.

Specifications :

- Keep a power consumption as low as possible while maintaining a clock function.
- Keep counting a clock correctly.
- $f(X_{IN}) = 4.19 \text{ MHz}$, $f(X_{CIN}) = 32.768 \text{ kHz}$
- The Timer 1 interrupt is used in a normal power state. The Timer 3 interrupt is used during a power failure.

Port processing

Input port : Fix to "H" or "L" level in the external unit.

Output port : Fix to an output level which does not cause a current flow to the external unit.

[Example]

When a circuit turns on LED at "L" output level, fix the output level to "H".

I/O port : Input port — Fix to "H" or "L" level in the external unit.

Output port — Output the data which does not consume current.

VREF : Supplying to the Reference voltage input pin is stopped by the external circuit.

P45/ZCR (using as the input port) : Fix to "H" level in the external unit.

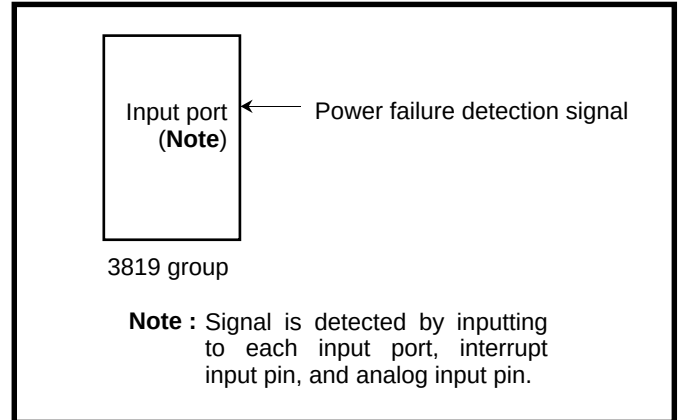


Fig. 2.9.14 Connection diagram [Counting without clock errors during a power failure]

Figure 2.9.15 shows a timing chart of counting without clock errors during a power failure, Figure 2.9.16 shows a structure of a clock counter, and Figures 2.9.17 and 2.9.18 show a setting of related registers.

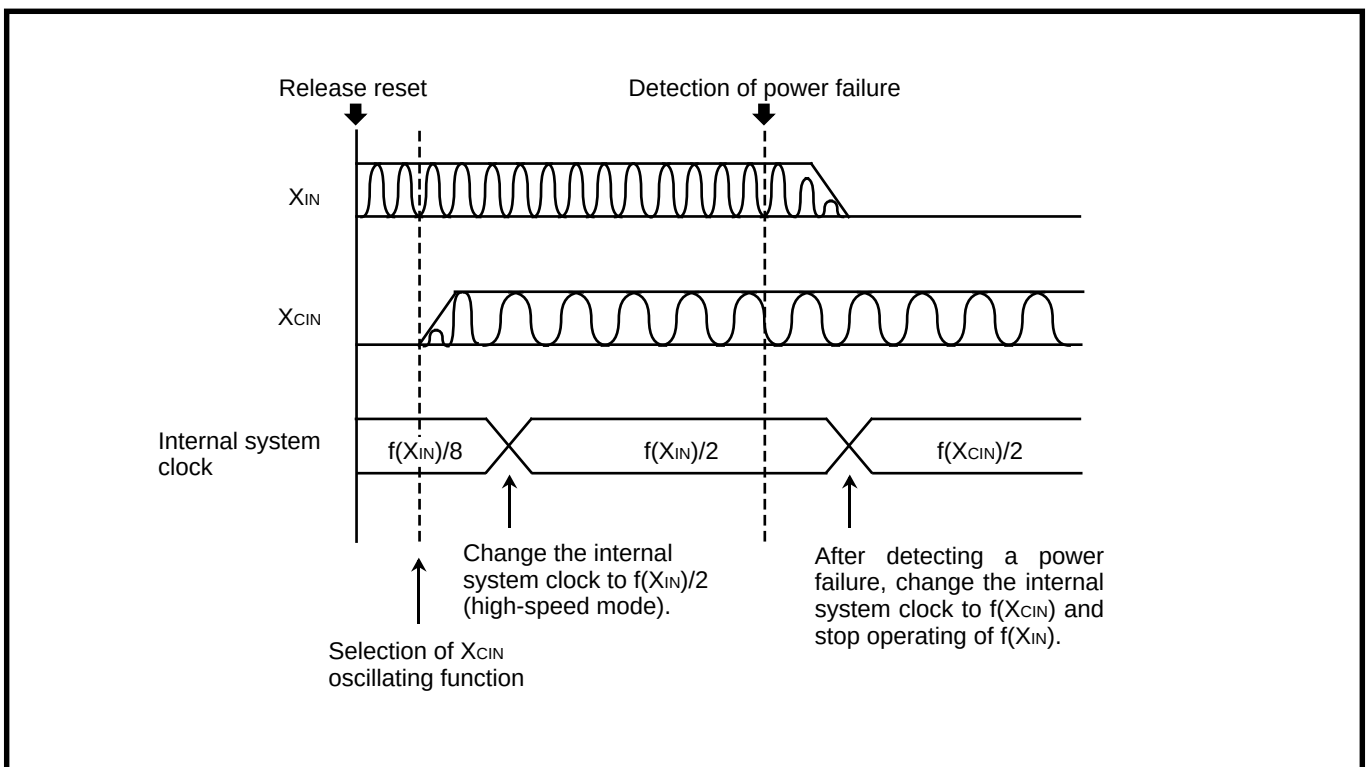


Fig. 2.9.15 Timing chart of counting without clock errors during a power failure

2. APPLICATION

2.9 Clock generating circuit

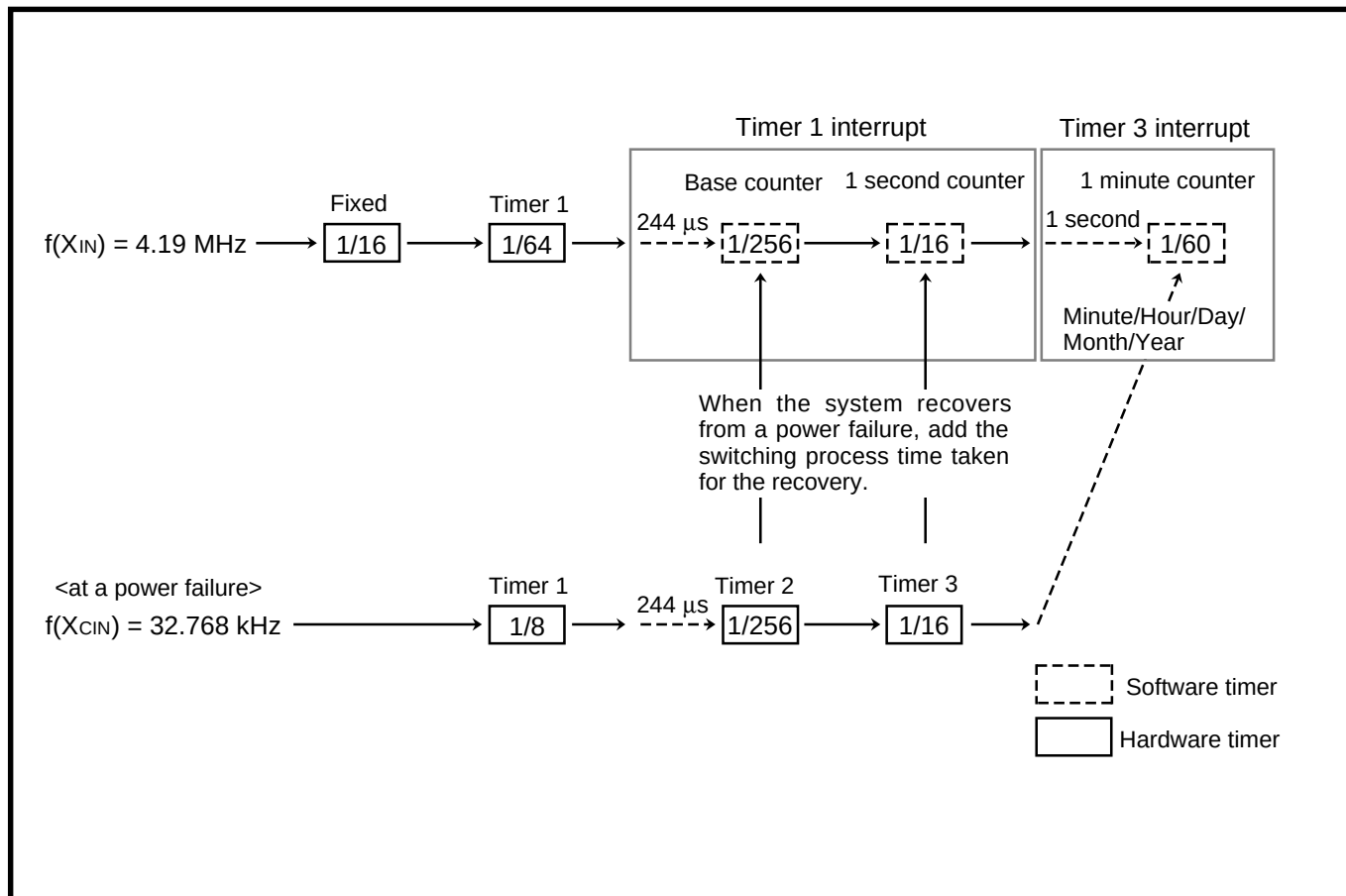


Fig. 2.9.16 Structure of a clock counter

2. APPLICATION

2.9 Clock generating circuit

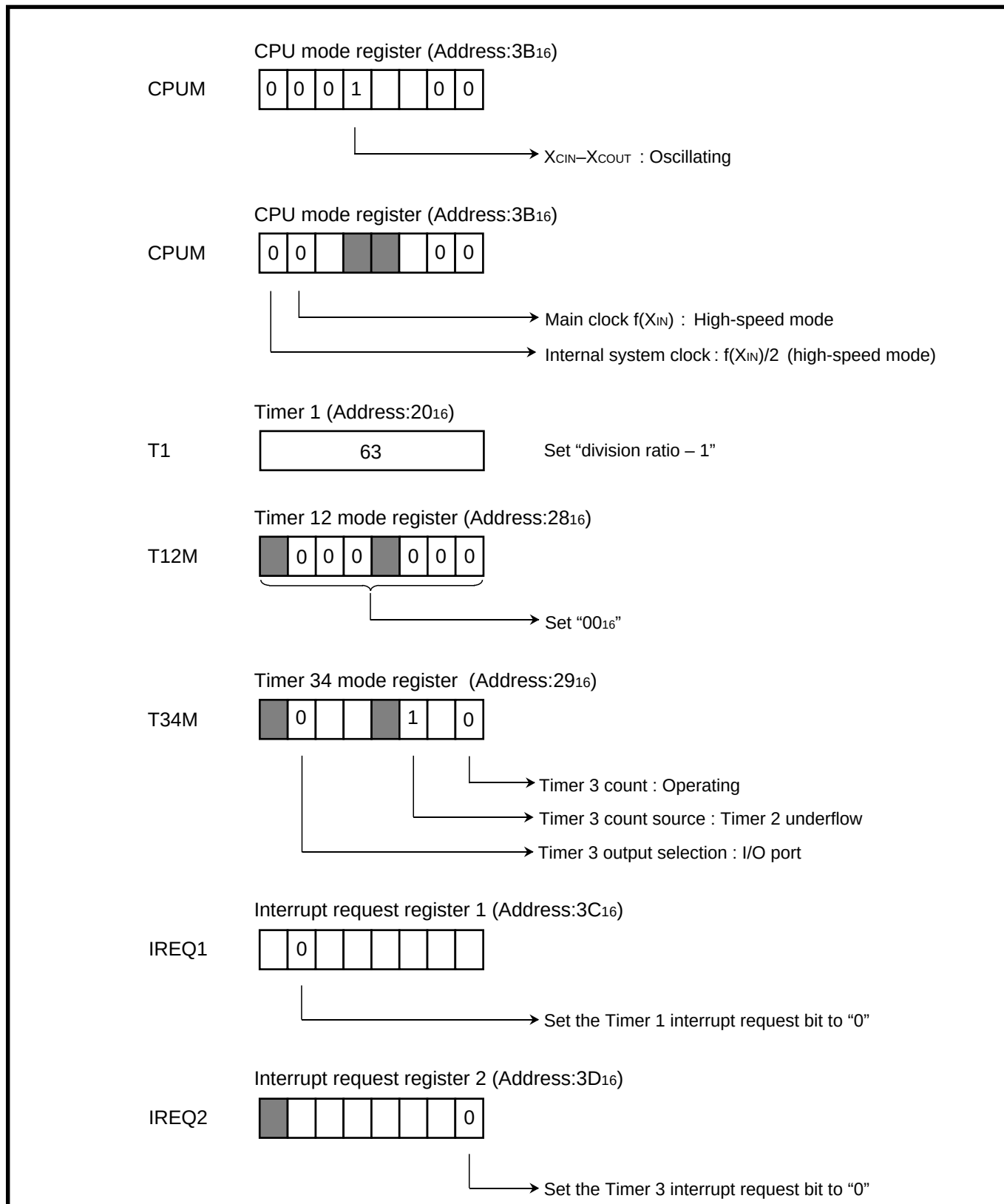


Fig. 2.9.17 Setting of related registers (1) [Counting without clock errors during a power failure]

2. APPLICATION

2.9 Clock generating circuit

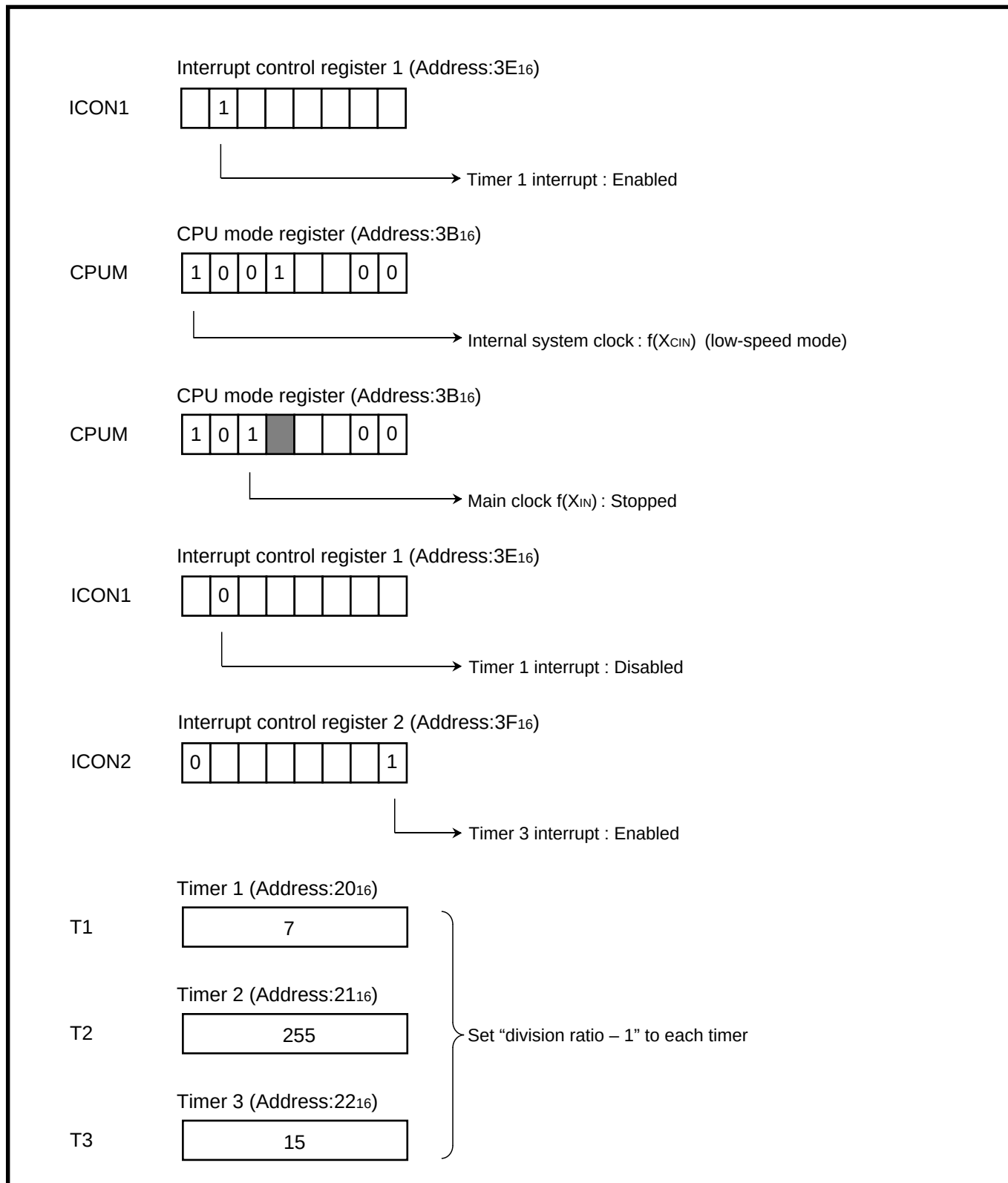


Fig. 2.9.18 Setting of related registers (2) [Counting without clock errors during a power failure]

2. APPLICATION

2.9 Clock generating circuit

Control procedure : Set the related registers in the order shown below to prepare for a power failure.

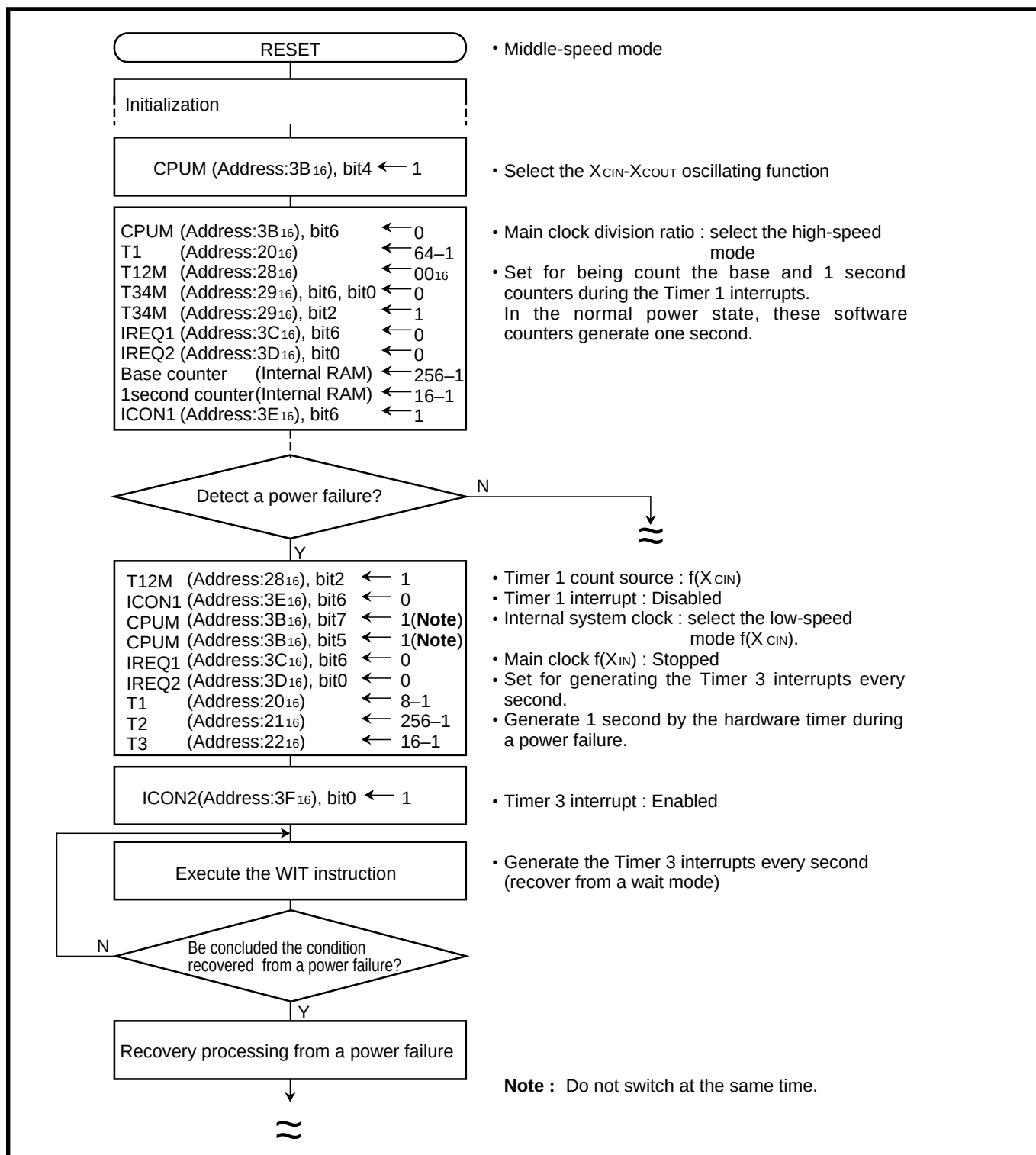


Fig. 2.9.19 Control procedure (1) [Counting without clock errors during a power failure]

2. APPLICATION

2.9 Clock generating circuit

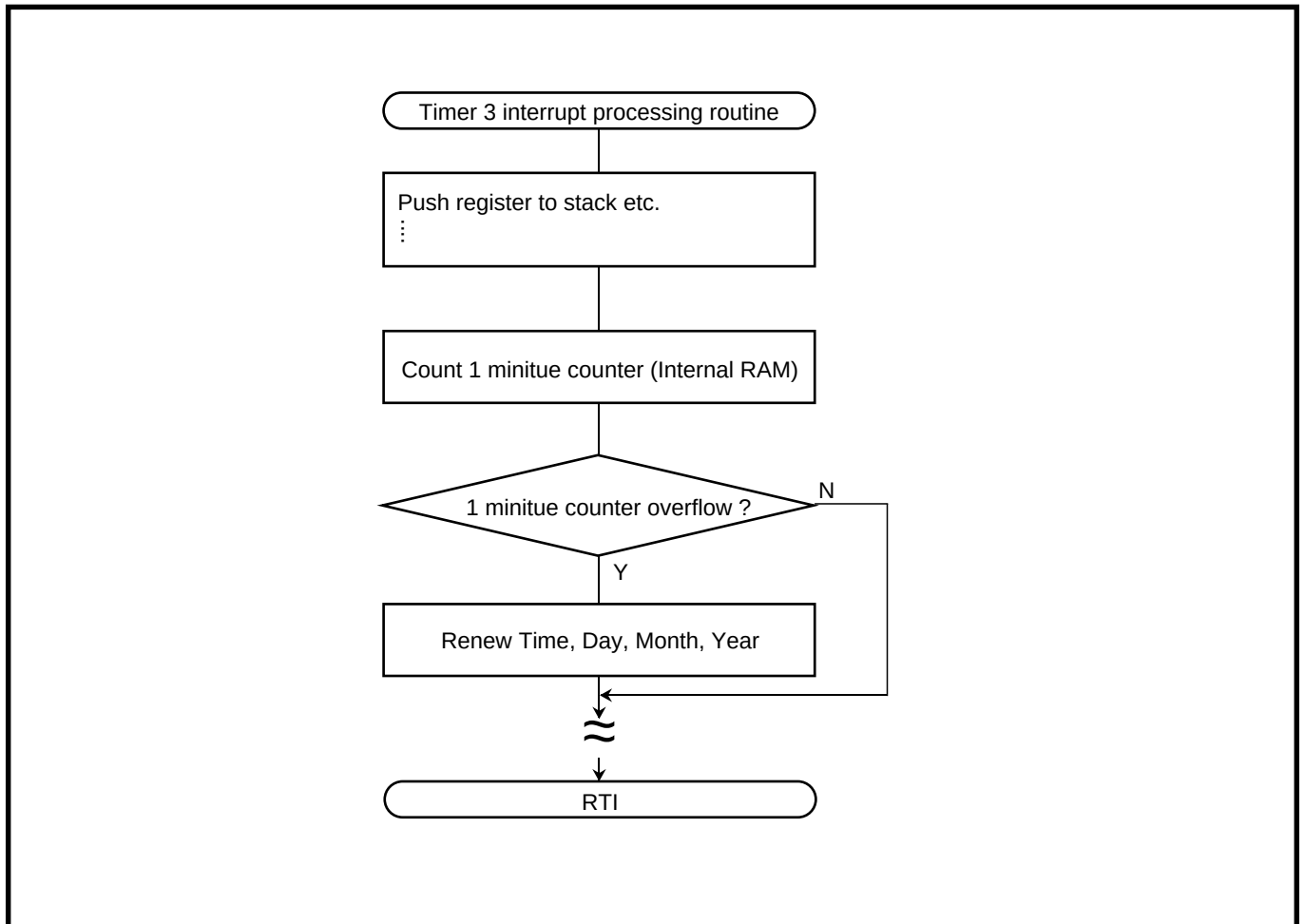
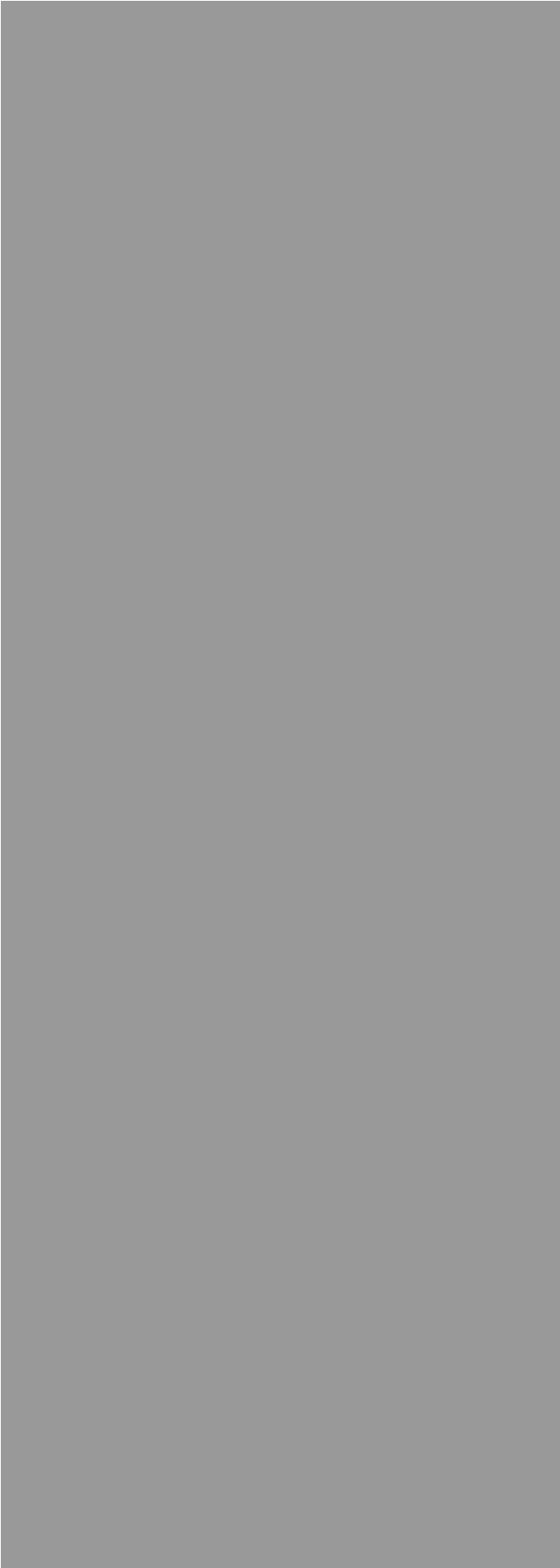


Fig. 2.9.20 Control procedure (2) [Counting without clock errors during a power failure]



CHAPTER 3

APPENDIX

- 3.1 Notes on use
- 3.2 Countermeasures
against noise
- 3.3 Control registers
- 3.4 Mask ROM ordering method
- 3.5 Mark specification form
- 3.6 Package outline
- 3.7 Memory map
- 3.8 Pin configuration

3. APPENDIX

3.1 Notes on use

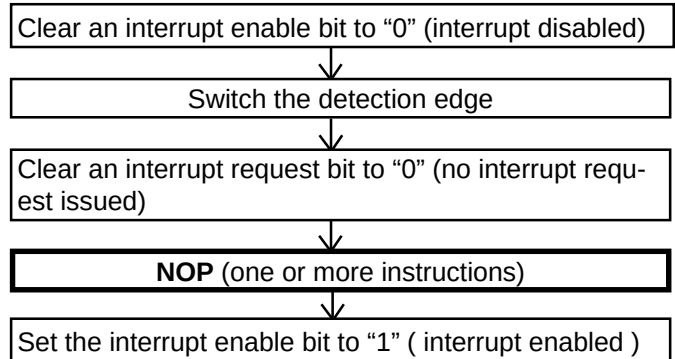
3.1.1 Notes on Interrupts

<Note 1>

For the products able to switch the external interrupt detection edge, switch it as the following sequence.

Reason

The interrupt circuit recognizes the switching of the detection edge as the change of external input signals. This may cause an unnecessary interrupt.



<Note 2>

Fix the bit 7 of the interrupt control register 2 to "0".

Figure 3.1.1 shows the structure of the interrupt control register 2.

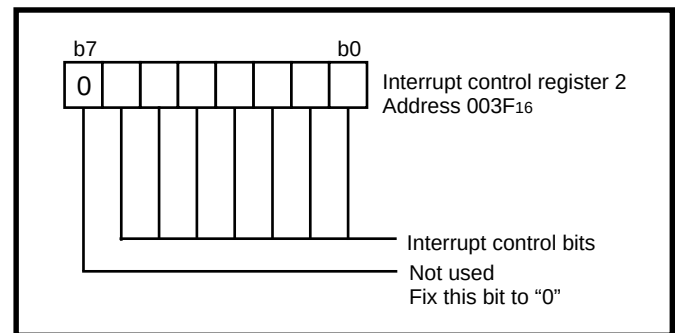


Fig. 3.1.1 Structure of interrupt control register 2

3.1.2 Notes on the FLD controller and the serial I/O automatic transfer function

When using the FLD controller function and the serial I/O automatic transfer function, set the system clock to the high-speed mode or the middle-speed mode.

3.1.3 Notes on the A-D converter

<Note 1>

Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01 μ F to 1 μ F. Further, be sure to verify the operation of application products on the user side.

Reason

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A-D comparison precision to be worse.

<Note 2>

Pins AVcc and AVss are A-D converter power source pins. Connect them as following :

- AVcc : Connect to the Vcc line which is the analog system
- AVss : Connect to the Vss line which is the analog system

3. APPENDIX

<Note 3>

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low. Thus, make sure the following during an A-D conversion.

- $f(X_{IN})$ is 500 kHz or more .
- Do not execute the STP instruction and WIT instruction.

3.1.4 Notes on the RESET pin

<Note>

In case where the RESET signal rise time is long, connect a ceramic capacitor or others across the RESET pin and the Vss pin. And use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following :

- Make the length of the wiring which is connected to a capacitor.
- Be sure to check the operation of application products on the user side.

Reason

If the several nanosecond or several ten nanosecond impulse noise enters the RESET pin, it may cause a microcomputer failure.

3.1.5 Notes on input and output pins

<Note 1>

In stand-by state* for low-power dissipation, do not make input levels of an input and an I/O port "undefined," especially for the I/O ports of the P-channel and the N-channel open-drain.

Pull-up (connect the port to Vcc) or pull-down (connect the port to Vss) these ports through a resistor.

When determining a resistance value, note the following points:

- External circuit
- Variation of output levels during the ordinary operation

When using built-in pull-up or pull-down resistor as an option, note on varied current values.

- When setting as an input port : Fix its input level
- When setting as an output port : Prevent current from flowing out to external

Reason

Even when setting as an output port with its direction register, in the following state :

● P-channel.....when the content of the data register (port latch) is "0"

● N-channel.....when the content of the data register (port latch) is "1"

the transistor becomes the OFF state, which causes the ports to be the high-impedance state. Note that the level becomes "undefined" depending on external circuits.

Accordingly, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of an input and an I/O port are "undefined." This may cause power source current.

* stand-by state : the stop mode by executing the **STP** instruction
the wait mode by executing the **WIT** instruction

3. APPENDIX

<Note 2>

When the data register (port latch) of an I/O port is modified with the bit managing instruction*, the value of the unspecified bit may be changed.

Reason

The bit managing instructions are read-modify-write form instructions for reading and writing data by a byte unit. Accordingly, when these instructions are executed on a bit of the data register of an I/O port, the following is executed to all bits of the data register.

- As for a bit which is set to an input port : The pin state is read in the CPU, and is written to this bit after bit managing.
- As for a bit which is set to an output port : The bit value is read in the CPU, and is written to this bit after bit managing.

Note the following :

- Even when a port which is set as an output port is changed for an input port, its data register holds the output data.
- As for a bit of which is set to an input port , its value may be changed even when not specified with a bit managing instruction in case where the pin state differs from its data register contents

* bit managing instructions : **SEB** and **CLB** instruction

<Note 3>

When not using the A-D converter, connect the A-D converter power source AVss pin as follows :

- AVss : Connect to the Vss pin

Reason

If the AVss pin is opened, the microcomputer may have a failure because of noise or others.

3.1.6 Notes on clock synchronous serial I/O

<Note>

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to "1" at "H" of the SCLK input level. Also, write data to the transmit buffer register at "H" of the SCLK input level.

3. APPENDIX

3.2 Countermeasures against noise

3.2 Countermeasures against noise

Countermeasures against noise are described below. The following countermeasures are effective against noise in theory, however, it is necessary not only to take measures as follows but to evaluate before actual use.

3.2.1 Shortest wiring length

The wiring on a printed circuit board can be as an antenna which feeds noise into the microcomputer.

The shorter the total wiring length (by mm unit), the less the possibility of noise insertion into a microcomputer.

(1) Wiring for the $\overline{\text{RESET}}$ pin

Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the Vss pin with the shortest possible wiring (within 20mm).

Reason

The reset works to initialize a microcomputer.

The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

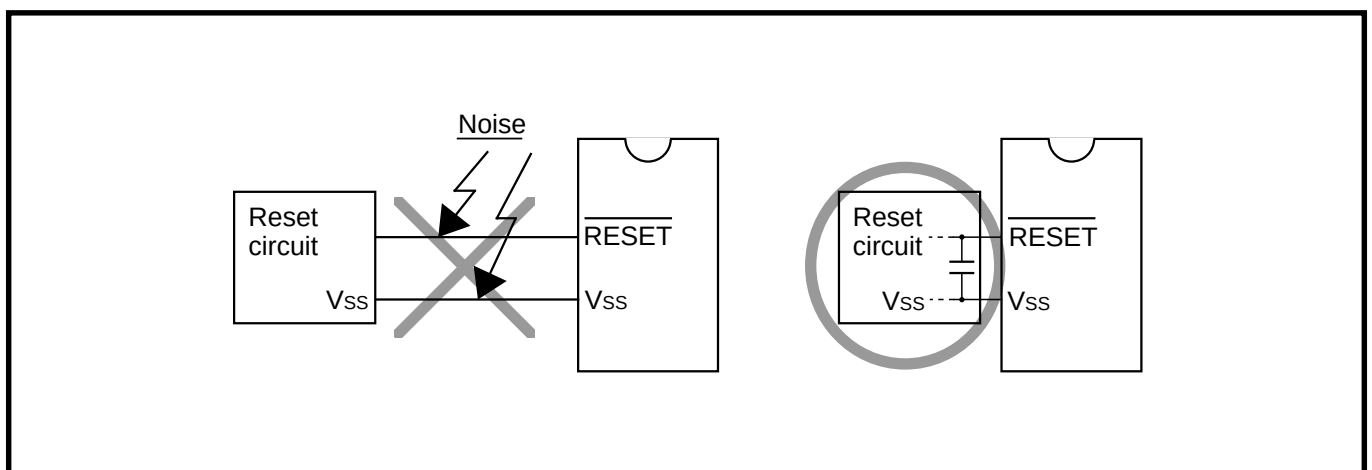


Fig. 3.2.1 Wiring for the $\overline{\text{RESET}}$ pin

(2) Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

Reason

A microcomputer's operation synchronizes with a clock generated by the oscillator (circuit). If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway.

Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

3. APPENDIX

3.2 Countermeasures against noise

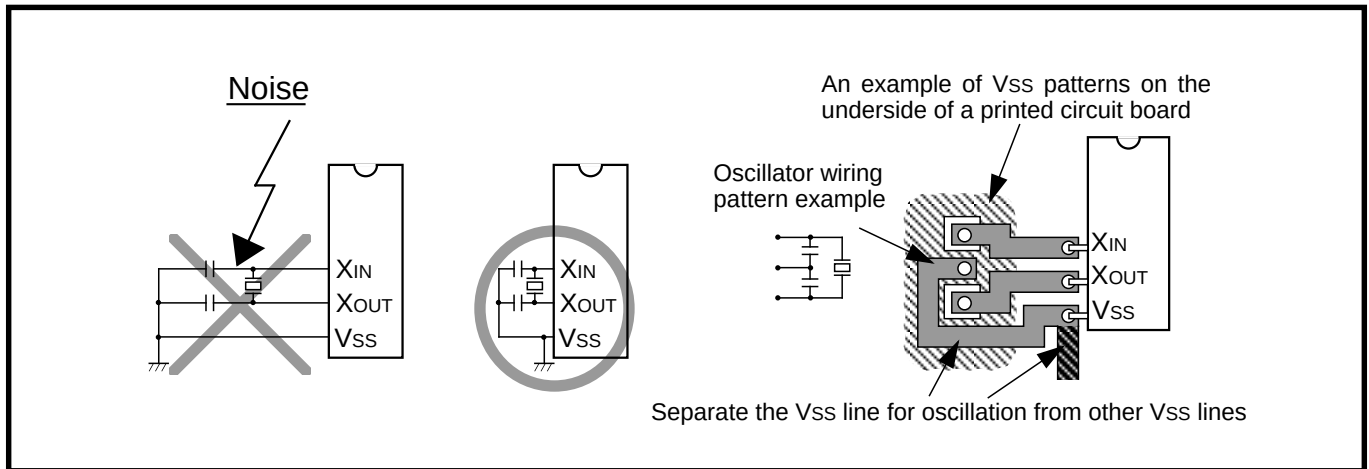


Fig. 3.2.2 Wiring for clock I/O pins

(3) Wiring for the VPP pin of the One Time PROM version and the eeprom version

- Make the length of wiring which is connected to the VPP pin as short as possible.
- Connect an approximately 5 kΩ resistor to the VPP pin in serial.

Reason

The VPP pin of the One Time PROM and the EPROM version is the power source input pin for the built-in PROM. When programming in the built-in PROM, the impedance of the VPP pin is low to allow the electric current for wiring flow into the PROM. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the built-in PROM, which may cause a program runaway.

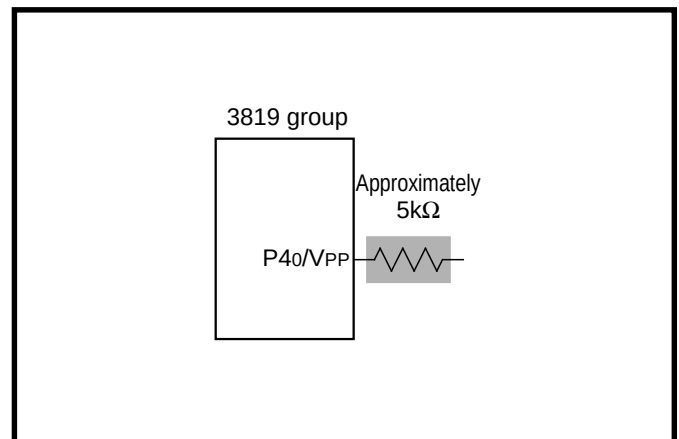


Fig. 3.2.3 Wiring for the VPP pin of the One Time PROM and the EPROM version

3.2.2 Connection of a bypass capacitor across the Vss line and the Vcc line

Connect an approximately 0.1 μF bypass capacitor across the Vss line and the Vcc line as follows:

- Connect a bypass capacitor across the Vss pin and the Vcc pin at equal length.
- Connect a bypass capacitor across the Vss pin and the Vcc pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for Vss line and Vcc line.

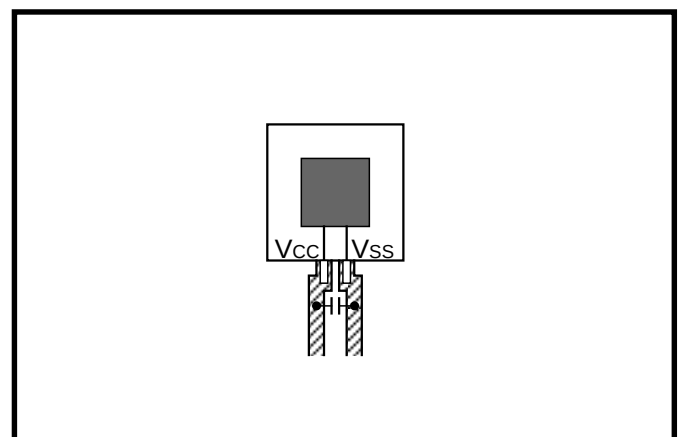


Fig. 3.2.4 Bypass capacitor across the Vss line and the Vcc line

3. APPENDIX

3.2 Countermeasures against noise

3.2.3 Wiring to analog input pins

- Connect an approximately 100 Ω to 1 k Ω resistor to an analog signal line which is connected to an analog input pin in series. Besides, connect the resistor to the microcomputer as close as possible.
- Connect an approximately 1000 pF capacitor across the Vss pin and the analog input pin. Besides, connect the capacitor to the Vss pin as close as possible.

Reason

Signals which is input in an analog input pin (such as an A-D converter input pin) are usually output signals from sensor. The sensor which detects a change of event is installed far from the printed circuit board with a microcomputer, the wiring to an analog input pin is longer necessarily. This long wiring functions as an antenna which feeds noise into the microcomputer, which causes noise to an analog input pin. If a capacitor between an analog input pin and the Vss pin is grounded at a position far away from the Vss pin, noise on the GND line may enter a microcomputer through the capacitor.

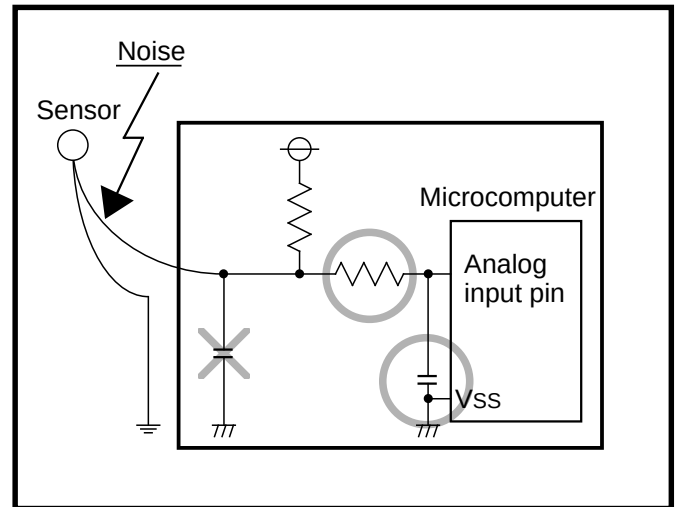


Fig.3.2.5 Analog signal line and a resistor and a capacitor

3.2.4. Oscillator concerns

Take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

(1) Keeping an oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

Reason

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

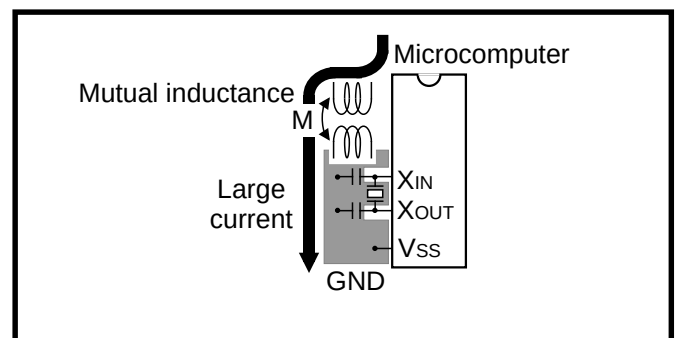


Fig.3.2.6 Wiring for a large current signal line

(2) Keeping an oscillator away from signal lines where potential levels change frequently

Install an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

Reason

Signal lines where potential levels change frequently (such as the CNTR pin line) may affect other lines at signal rising or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

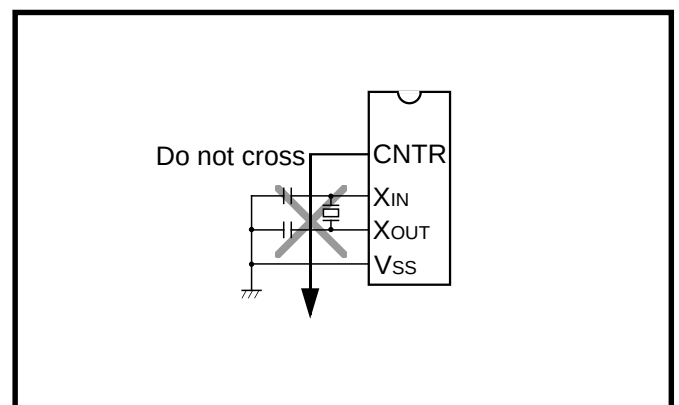


Fig.3.2.7 Wiring to a signal line where potential levels change frequently

3. APPENDIX

3.2 Countermeasures against noise

3.2.5 Setup for I/O ports

Setup I/O ports using hardware and software as follows:

<Hardware>

- Connect a resistor of 100 Ω or more to an I/O port in series.

<Software>

- As for an input port, read data several times by a program for checking whether input levels are equal or not.
- As for an output port, since the output data may reverse because of noise, rewrite data to its data register at fixed periods.
- Rewrite data to direction registers and pull-up control registers (only the product having it) at fixed periods.

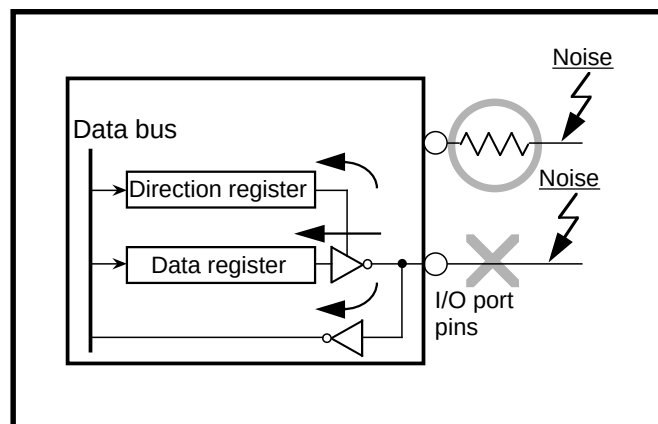


Fig. 3.2.8 Setup for I/O ports

When a direction register is set to input port again at fixed periods, a several-nanosecond short pulse may be output from this port. If this is undesirable, connect a capacitor to this port to remove the noise pulse.

3.2.6 Providing of watchdog timer function by software

If a microcomputer runs away because of noise or others, it can be detected by a software watchdog timer and the microcomputer can be reset to normal operation. This is equal to or more effective than program runaway detection by a hardware watchdog timer. The following shows an example of a watchdog timer provided by software.

In the following example, to reset a microcomputer to normal operation, the main routine detects errors of the interrupt processing routine and the interrupt processing routine detects errors of the main routine.

This example assumes that interrupt processing is repeated multiple times in a single main routine processing.

<The main routine>

- Assigns a single byte of RAM to a software watchdog timer (SWDT) and writes the initial value N in the SWDT once at each execution of the main routine. The initial value N should satisfy the following condition:

$$N+1 \geq (\text{Counts of interrupt processing executed in each main routine})$$

As the main routine execution cycle may change because of an interrupt processing or others, the initial value N should have a margin.

- Watches the operation of the interrupt processing routine by comparing the SWDT contents with counts of interrupt processing count after the initial value N has been set.
- Detects that the interrupt processing routine has failed and determines to branch to the program initialization routine for recovery processing in the following cases:
 - ① If the SWDT contents do not change after interrupt processing
 - ② If the changed SWDT contents are abnormal
(In Figure 3.2.9, the main routine determines that the interrupt processing routine has failed only if the SWDT contents do not change).

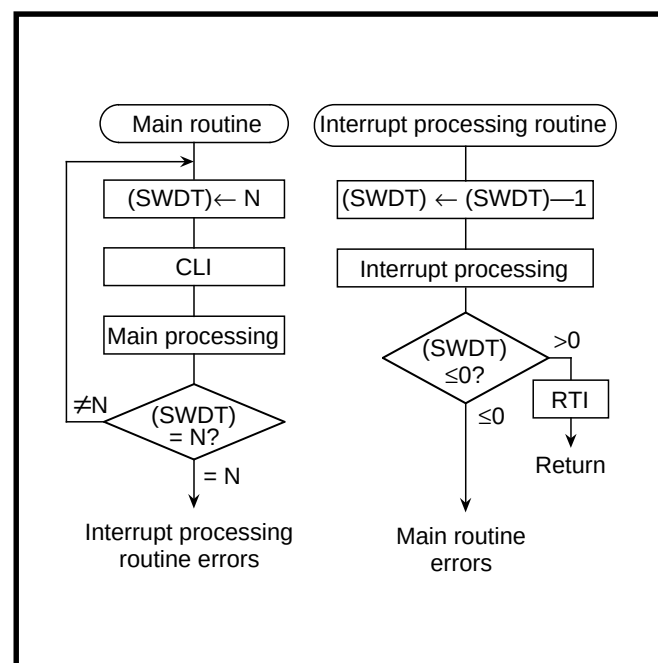


Fig. 3.2.9 Watchdog timer by software

3. APPENDIX

3.2 Countermeasures against noise

<The interrupt processing routine>

- Decrements the SWDT contents by 1 at each interrupt processing.
- Determines that the main routine operates normally when the SWDT contents are reset to the initial value N at almost fixed cycles (at the fixed interrupt processing count).
- Detects that the main routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
 - ① If the SWDT contents are not initialized to the initial value N but continued to decrement and if they exceed the limit (and reach 0 or less).

3. APPENDIX

3819 Group 3.3 Control registers

3.3 Control registers

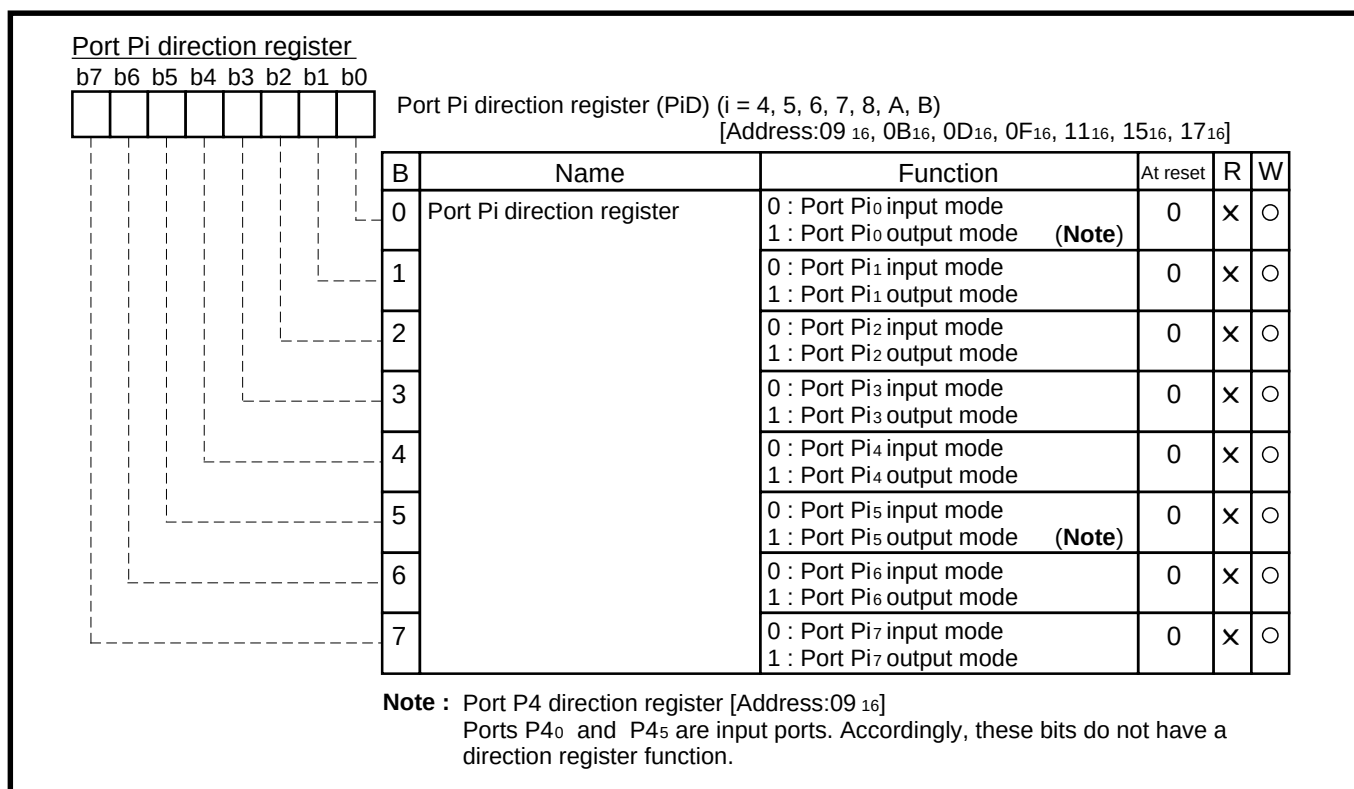


Fig. 3.3.1 Structure of Port Pi direction register (i = 4, 5, 6, 7, 8, A, B)

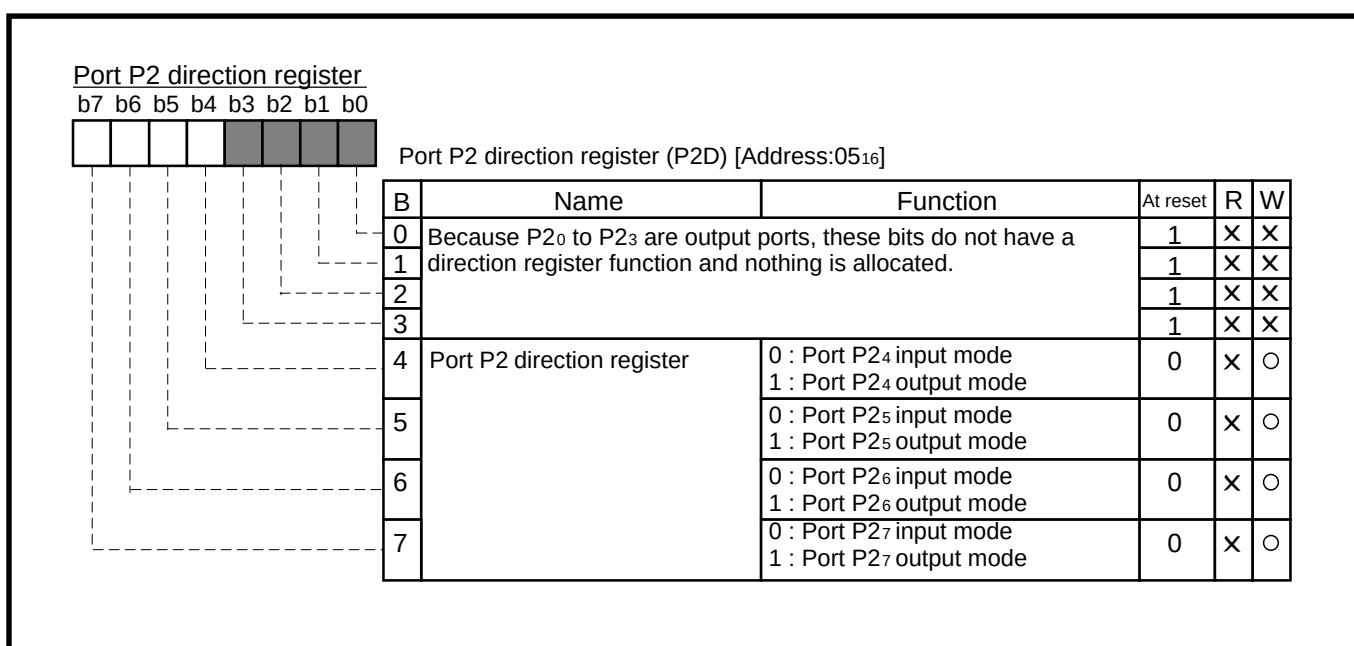


Fig. 3.3.2 Structure of Port P2 direction register

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3819 Group 3.3 Control registers

Serial I/O automatic transfer data pointer

Serial I/O automatic transfer data pointer

b7	b6	b5	b4	b3	b2	b1	b0

Serial I/O automatic transfer data pointer (SIODP) [Address:18₁₆]

B	Function	At reset	R	W
0	Indicate an address of Serial I/O automatic transfer RAM.	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."	0	○	×
6		0	○	×
7		0	○	×

Fig. 3.3.3 Structure of Serial I/O automatic transfer data pointer

Serial I/O 1 control register

Serial I/O 1 control register (SIO1CON) [Address:19 ₁₆]							
B	Name	Function	At reset	R	W		
0	Internal synchronous clock selection bits	b2 b1b0 000 : f(X _{IN})/8 or f(X _{CIN})/8	0	○	○		
1		001 : f(X _{IN})/16 or f(X _{CIN})/16	0	○	○		
2		010 : f(X _{IN})/32 or f(X _{CIN})/32	0	○	○		
		011 : f(X _{IN})/64 or f(X _{CIN})/64					
		110 : f(X _{IN})/128 or f(X _{CIN})/128	0	○	○		
		111 : f(X _{IN})/256 or f(X _{CIN})/256					
3	Serial I/O 1 port selection bit (P6 ₅ ,P6 ₆ ,P6 ₇ *)	0 : I/O port 1 : SOUT1, SCLK11, SCLK12* signal pins	0	○	○		
4	S _{RDY1} output selection bit (P6 ₇)	0 : I/O port 1 : S _{RDY1} /CS* signal pin (Note)	0	○	○		
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○		
6	Synchronous clock selection bit	0 : External clock 1 : Internal clock	0	○	○		
7	P6 ₅ /SOUT1 P-channel output disable bit	0 : CMOS output (in output mode) 1 : N-channel open-drain output (in output mode)	0	○	○		

* Valid only in the Serial I/O automatic transfer mode

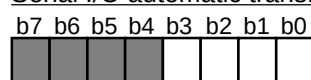
Note : When an external clock is selected in the serial I/O 1 automatic transfer mode, the S_{RDY1} signal pin is used as the CS signal input pin.

Fig. 3.3.4 Structure of Serial I/O 1 control register

3. APPENDIX

3819 Group 3.3 Control registers

Serial I/O automatic transfer control register

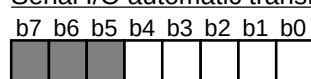


Serial I/O automatic transfer control register (SIOAC) [Address:1A₁₆]

B	Name	Function	At reset	R	W
0	Automatic transfer control bit	0 : Serial I/O ordinary mode (serial I/O 1 interrupt) 1 : Automatic transfer mode (serial I/O automatic transfer interrupt)	0	○	○
1	Automatic transfer start bit	0 : Transfer completion 1 : Transferring (starts by writing "1")	0	○	○
2	Transfer mode switch bit	0 : Fullduplex (transmit / receive) mode 1 : Transmit-only mode	0	○	○
3	Synchronous clock output pin selection bit	0 : SCLK ₁₁ 1 : SCLK ₁₂	0	○	○
4	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."		0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 3.3.5 Structure of Serial I/O automatic transfer control register

Serial I/O automatic transfer interval register



Serial I/O automatic transfer interval register (SIOAI) [Address:1C₁₆]

B	Function	At reset	R	W
0	$T_i = (n + 2) \times T_c$ $\left\{ \begin{array}{l} T_i = \text{a length of transfer interval} \\ n = \text{a setting value} \\ T_c = \text{a length of a bit of transfer clock} \end{array} \right.$	0	○	○
1		0	○	○
2		0	○	○
3		0	○	○
4		0	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."	0	○	×
6		0	○	×
7		0	○	×

Fig. 3.3.6 Structure of Serial I/O automatic transfer interval register

3. APPENDIX

3819 Group 3.3 Control registers

Serial I/O 2 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O 2 control register (SIO2CON) [Address:1D16]

B	Name	Function	At reset	R	W
0	Internal synchronous clock selection bits	b2 b1b0 000 : $f(X_{IN})/8$ or $f(X_{CIN})/8$	0	○	○
1		001 : $f(X_{IN})/16$ or $f(X_{CIN})/16$	0	○	○
2		010 : $f(X_{IN})/32$ or $f(X_{CIN})/32$	0	○	○
		011 : $f(X_{IN})/64$ or $f(X_{CIN})/64$			
		110 : $f(X_{IN})/128$ or $f(X_{CIN})/128$			
		111 : $f(X_{IN})/256$ or $f(X_{CIN})/256$			
3	Serial I/O 2 port selection bit (P5 ₁ ,P5 ₂)	0 : I/O port 1 : SOUT ₂ , SCLK ₂ signal pins	0	○	○
4	SRDY ₂ output selection bit (P5 ₃)	0 : I/O port 1 : SRDY ₂ signal pin	0	○	○
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○
6	Synchronous clock selection bit	0 : External clock 1 : Internal clock	0	○	○
7	P5 ₁ /SOUT ₂ P-channel output disable bit	0 : CMOS output (in output mode) 1 : N-channel open-drain output (in output mode)	0	○	○

Fig. 3.3.7 Structure of Serial I/O 2 control register

Serial I/O 3 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O 3 control register (SIO3CON) [Address:1E16]

B	Name	Function	At reset	R	W
0	Internal synchronous clock selection bits	b2 b1b0 000 : $f(X_{IN})/8$ or $f(X_{CIN})/8$	0	○	○
1		001 : $f(X_{IN})/16$ or $f(X_{CIN})/16$	0	○	○
2		010 : $f(X_{IN})/32$ or $f(X_{CIN})/32$	0	○	○
		011 : $f(X_{IN})/64$ or $f(X_{CIN})/64$			
		110 : $f(X_{IN})/128$ or $f(X_{CIN})/128$			
		111 : $f(X_{IN})/256$ or $f(X_{CIN})/256$			
3	Serial I/O 3 port selection bit (P5 ₅ ,P5 ₆)	0 : I/O port 1 : SOUT ₃ , SCLK ₃ signal pins	0	○	○
4	SRDY ₃ output selection bit (P5 ₇)	0 : I/O port 1 : SRDY ₃ signal pin	0	○	○
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○
6	Synchronous clock selection bit	0 : External clock 1 : Internal clock	0	○	○
7	P5 ₅ /SOUT ₃ P-channel output disable bit	0 : CMOS output (in output mode) 1 : N-channel open-drain output (in output mode)	0	○	○

Fig. 3.3.8 Structure of Serial I/O 3 control register

3. APPENDIX

3819 Group 3.3 Control registers

Timer 12 mode register

b7 b6 b5 b4 b3 b2 b1 b0



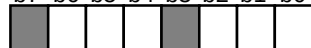
Timer 12 mode register (T12M) [Address:28₁₆]

B	Name	Function	At reset	R	W
0	Timer 1 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 2 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 1 count source selection bit	0 : f(X _{IN})/16 or f(X _{CIN})/16 1 : f(X _{CIN})	0	○	○
3	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
4	Timer 2 count source selection bits	b5 b4 00 : Timer 1 underflow	0	○	○
5		01 : f(X _{CIN}) 10 : External count input CNTR ₀ 11 : Not available	0	○	○
6	Timer 1 output selection bit (P4 ₆)	0 : I/O port 1 : Timer 1 output	0	○	○
7	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0."		0	○	×

Fig. 3.3.9 Structure of Timer 12 mode register

Timer 34 mode register

b7 b6 b5 b4 b3 b2 b1 b0



Timer 34 mode register (T34M) [Address:29₁₆]

B	Name	Function	At reset	R	W
0	Timer 3 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 4 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 3 count source selection bit	0 : f(X _{IN})/16 or f(X _{CIN})/16 1 : Timer 2 underflow	0	○	○
3	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
4	Timer 4 count source selection bits	b5 b4 00 : f(X _{IN})/16 or f(X _{CIN})/16	0	○	○
5		01 : Timer 3 underflow 10 : External count input CNTR ₁ 11 : Not available	0	○	○
6	Timer 3 output selection bit (P4 ₇)	0 : I/O port 1 : Timer 3 output	0	○	○
7	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0."		0	○	×

Fig. 3.3.10 Structure of Timer 34 mode register

3819 Group

3.3 Control registers

3. APPENDIX

Timer 56 mode register

b7 b6 b5 b4 b3 b2 b1 b0

0							
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Timer 56 mode register (T56M) [Address:2A₁₆]

B	Name	Function	At reset	R	W
0	Timer 5 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 6 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 5 count source selection bit	0 : f(X _{IN})/16 or f(X _{CIN})/16 1 : Timer 4 underflow	0	○	○
3	Timer 6 operation mode selection bit	0 : Timer mode 1 : PWM mode	0	○	○
4	Timer 6 count source selection bits	b5 b4 00 : f(X _{IN})/16 or f(X _{CIN})/16 01 : Timer 5 underflow 10 : Timer 4 underflow 11 : Not available	0	○	○
5			0	○	○
6	Timer 6 (PWM) output selection bit (P6 ₁)	0 : I/O port 1 : Timer 6 output	0	○	○
7	Fix this bit to "0."		0	○	○

Fig. 3.3.11 Structure of Timer 56 mode register

3. APPENDIX

AD/DA control register

b7 b6 b5 b4 b3 b2 b1 b0



AD/DA control register (ADCON) [Address:2C16]

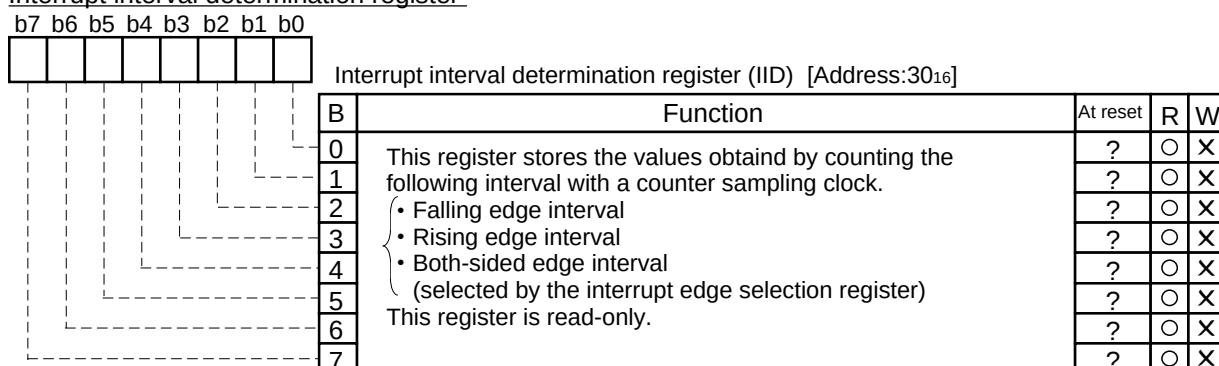
B	Name	Function	At reset	R	W
0	Analog input pin selection bits	b3 b2 b1 b0 0 0 0 0 : P7 ₀ /AN ₀ 0 0 0 1 : P7 ₁ /AN ₁ 0 0 1 0 : P7 ₂ /AN ₂ 0 0 1 1 : P7 ₃ /AN ₃ 0 1 0 0 : P7 ₄ /AN ₄ 0 1 0 1 : P7 ₅ /AN ₅ 0 1 1 0 : P7 ₆ /AN ₆ 0 1 1 1 : P7 ₇ /AN ₇	0	○	○
1		0 1 0 0 : P7 ₄ /AN ₄ 0 1 0 1 : P7 ₅ /AN ₅ 0 1 1 0 : P7 ₆ /AN ₆ 0 1 1 1 : P7 ₇ /AN ₇	0	○	○
2		1 0 0 0 : P5 ₀ /SIN ₂ /AN ₈ 1 0 0 1 : P5 ₁ /SOUT ₂ /AN ₉ 1 0 1 0 : P5 ₂ /SCLK ₂ /AN ₁₀ 1 0 1 1 : P5 ₃ /SRDY ₂ /AN ₁₁	0	○	○
3		1 1 0 0 : P5 ₄ /SIN ₃ /AN ₁₂ 1 1 0 1 : P5 ₅ /SOUT ₃ /AN ₁₃ 1 1 1 0 : P5 ₆ /SCLK ₃ /AN ₁₄ 1 1 1 1 : P5 ₇ /SRDY ₃ /AN ₁₅	0	○	○
4	A-D conversion completion bit	0 : Conversion in progress 1 : Conversion completed	1	○	○
5	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
6	D-A output enable bit	0 : Disable 1 : Enable	0	○	○
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×

Fig. 3.3.12 Structure of AD/DA control register

3. APPENDIX

3819 Group 3.3 Control registers

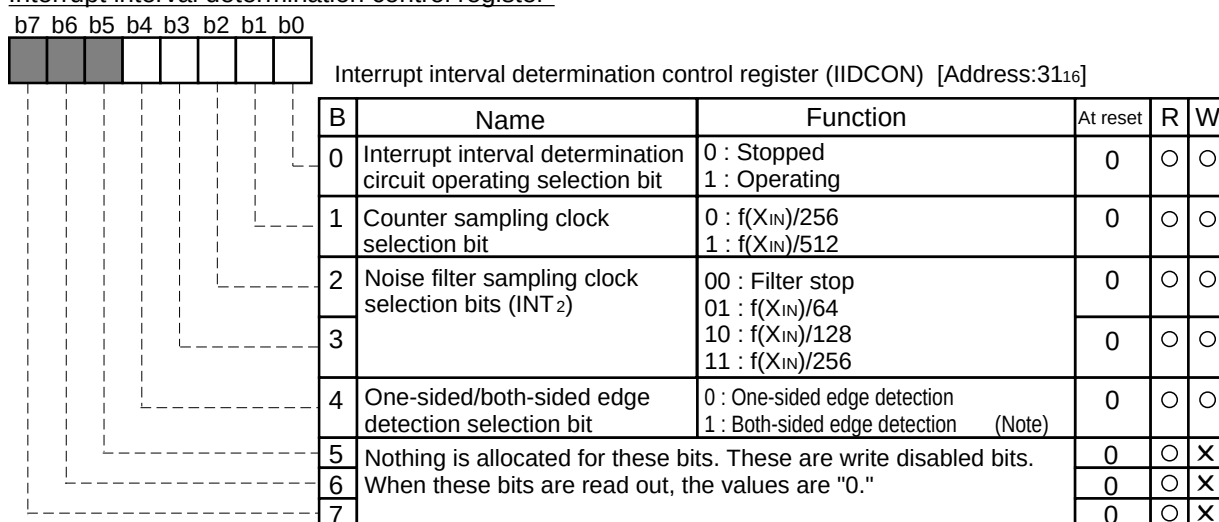
Interrupt interval determination register



Note : When the noise filter sampling clock selection bits (bits 2 and 3) of the Interrupt interval determination control register (IIDCON) (Address: 31₁₆) is set to "00" (when no noise filter is used), the both-sided edge detection function is not available.

Fig. 3.3.13 Structure of Interrupt interval determination register

Interrupt interval determination control register



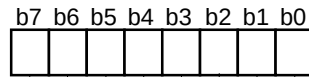
Note : When the noise filter sampling clock selection bits (bits 2 and 3) of the Interrupt interval determination control register (IIDCON) (Address: 31₁₆) is set to "00" (when no noise filter is used), the both-sided edge detection function is not available.

Fig. 3.3.14 Structure of Interrupt interval determination control register

3. APPENDIX

3819 Group 3.3 Control registers

Port P0 segment/digit switch register

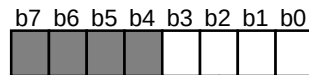


Port P0 segment/digit switch register (P0SDR) [Address:32₁₆]

B	Name	Function	At reset	R	W
0	Port P0 segment/digit switch register	0 : DIG ₀ 1 : SEG ₃₂	0	○	○
1		0 : DIG ₁ 1 : SEG ₃₃	0	○	○
2		0 : DIG ₂ 1 : SEG ₃₄	0	○	○
3		0 : DIG ₃ 1 : SEG ₃₅	0	○	○
4		0 : DIG ₄ 1 : SEG ₃₆	0	○	○
5		0 : DIG ₅ 1 : SEG ₃₇	0	○	○
6		0 : DIG ₆ 1 : SEG ₃₈	0	○	○
7		0 : DIG ₇ 1 : SEG ₃₉	0	○	○

Fig. 3.3.15 Structure of Port P0 segment/digit switch register

Port P2 digit/port switch register



Port P2 digit/port switch register (P2DPR) [Address:33₁₆]

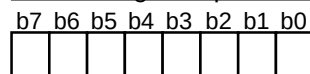
B	Name	Function	At reset	R	W
0	Port P2 digit/port switch register	0 : Port P2 ₀ output-only 1 : DIG ₁₆	0	○	○
1		0 : Port P2 ₁ output-only 1 : DIG ₁₇	0	○	○
2		0 : Port P2 ₂ output-only 1 : DIG ₁₈	0	○	○
3		0 : Port P2 ₃ output-only 1 : DIG ₁₉	0	○	○
4	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."		0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 3.3.16 Structure of Port P2 digit/port switch register

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3819 Group 3.3 Control registers

Port P8 segment/port switch register

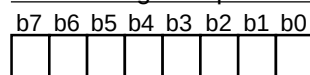


Port P8 segment/port switch register (P8SPR) [Address:34₁₆]

B	Name	Function	At reset	R	W
0	Port P8 segment/port switch register	0 : Port P8 ₀ for I/O 1 : SEG ₈	0	○	○
1		0 : Port P8 ₁ for I/O 1 : SEG ₉	0	○	○
2		0 : Port P8 ₂ for I/O 1 : SEG ₁₀	0	○	○
3		0 : Port P8 ₃ for I/O 1 : SEG ₁₁	0	○	○
4		0 : Port P8 ₄ for I/O 1 : SEG ₁₂	0	○	○
5		0 : Port P8 ₅ for I/O 1 : SEG ₁₃	0	○	○
6		0 : Port P8 ₆ for I/O 1 : SEG ₁₄	0	○	○
7		0 : Port P8 ₇ for I/O 1 : SEG ₁₅	0	○	○

Fig. 3.3.17 Structure of Port P8 segment/port switch register

Port PA segment/port switch register



Port PA segment/port switch register (PASPR) [Address:35₁₆]

B	Name	Function	At reset	R	W
0	Port PA segment/port switch register	0 : Port PA ₀ for I/O 1 : SEG ₀	0	○	○
1		0 : Port PA ₁ for I/O 1 : SEG ₁	0	○	○
2		0 : Port PA ₂ for I/O 1 : SEG ₂	0	○	○
3		0 : Port PA ₃ for I/O 1 : SEG ₃	0	○	○
4		0 : Port PA ₄ for I/O 1 : SEG ₄	0	○	○
5		0 : Port PA ₅ for I/O 1 : SEG ₅	0	○	○
6		0 : Port PA ₆ for I/O 1 : SEG ₆	0	○	○
7		0 : Port PA ₇ for I/O 1 : SEG ₇	0	○	○

Fig. 3.3.18 Structure of Port PA segment/port switch register

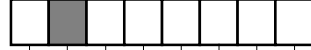
3819 Group

3.3 Control registers

3. APPENDIX

FLDC mode register 1

b7 b6 b5 b4 b3 b2 b1 b0



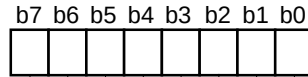
FLDC mode register 1 (FLDM1) [Address:36₁₆]

B	Name	Function	At reset	R	W
0	Tscan control bits	b1b0 0 0 : FLD digit interrupt (at rising edge of each digit)	0	○	○
1		0 1 : 1 × Tdisp } FLD blanking 1 0 : 2 × Tdisp } interrupt 1 1 : 3 × Tdisp } (at falling edge of the last digit)	0	○	○
2	Toff control bit (Setting of digit/segment OFF time)	b5 b4 b3 b2 0 0 0 0 : 1/16 × Tdisp 0 0 0 1 : 2/16 × Tdisp 0 0 1 0 : 3/16 × Tdisp 0 0 1 1 : 4/16 × Tdisp 0 1 0 0 : 5/16 × Tdisp 0 1 0 1 : 6/16 × Tdisp 0 1 1 0 : 7/16 × Tdisp 0 1 1 1 : 8/16 × Tdisp 1 0 0 0 : 9/16 × Tdisp 1 0 0 1 : 10/16 × Tdisp 1 0 1 0 : 11/16 × Tdisp 1 0 1 1 : 12/16 × Tdisp 1 1 0 0 : 13/16 × Tdisp 1 1 0 1 : 14/16 × Tdisp 1 1 1 0 : 15/16 × Tdisp 1 1 1 1 : 16/16 × Tdisp	0	○	○
3			0	○	○
4			0	○	○
5			0	○	○
6	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
7	High-breakdown-voltage drivability selection bit	0 : Strong drivability 1 : Weak drivability	0	○	○

Fig. 3.3.19 Structure of FLDC mode register 1

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FLDC mode register 2


FLDC mode register 2 (FLDM2) [Address:37₁₆]

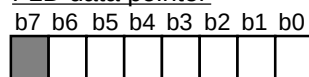
B	Name	Function	At reset	R	W
0	Automatic display control bit (P0,P1,P2 ₀ –P2 ₃ ,P3,P8,P9,PA)	0 : Ordinary mode 1 : Automatic display mode	0	○	○
1	Display start bit	0 : Display stopped 1 : Display in progress (display starts by writing "1" to this bit which is set to "0".)	0	○	○
2	Tdisp control bits (digit time setting) (at 8 MHz oscillation frequency)	b5 b4 b3 b2 0 0 0 0 : 128 μs 0 0 0 1 : 256 μs 0 0 1 0 : 384 μs 0 0 1 1 : 512 μs 0 1 0 0 : 640 μs 0 1 0 1 : 768 μs 0 1 1 0 : 896 μs 0 1 1 1 : 1024 μs 1 0 0 0 : 1152 μs 1 0 0 1 : 1280 μs 1 0 1 0 } ⋮ } Not available 1 1 1 1 }	0	○	○
3			0	○	○
4			0	○	○
5			0	○	○
6	P1 ₀ segment/digit switch bit	0 : Digit (DIG ₈) 1 : Segment (SEG ₄₀)	0	○	○
7	P1 ₁ segment/digit switch bit	0 : Digit (DIG ₉) 1 : Segment (SEG ₄₁)	0	○	○

Fig. 3.3.20 Structure of FLDC mode register 2

3. APPENDIX

3819 Group 3.3 Control registers

FLD data pointer

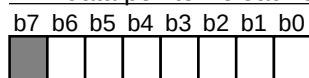


FLD data pointer (FLDDP) [Address:38₁₆]

B	Function	At reset	R	W
0	Indicate the address of data which is transferred to the segment of the FLD automatic display RAM.	?	○	×
1		?	○	×
2		?	○	×
3		?	○	×
4		?	○	×
5		?	○	×
6		?	○	×
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."	0	○	×

Fig. 3.3.21 Structure of FLD data pointer

FLD data pointer reload register



FLD data pointer reload register (FLDDP) [Address:38₁₆]

B	Function	At reset	R	W
0	Indicate the first digit address of the high-order segment.	?	×	○
1		?	×	○
2		?	×	○
3		?	×	○
4		?	×	○
5		?	×	○
6		?	×	○
7	Nothing is allocated for this bit. This is a write disabled bit.	?	×	×

Fig. 3.3.22 Structure of FLD data pointer reload register

3. APPENDIX

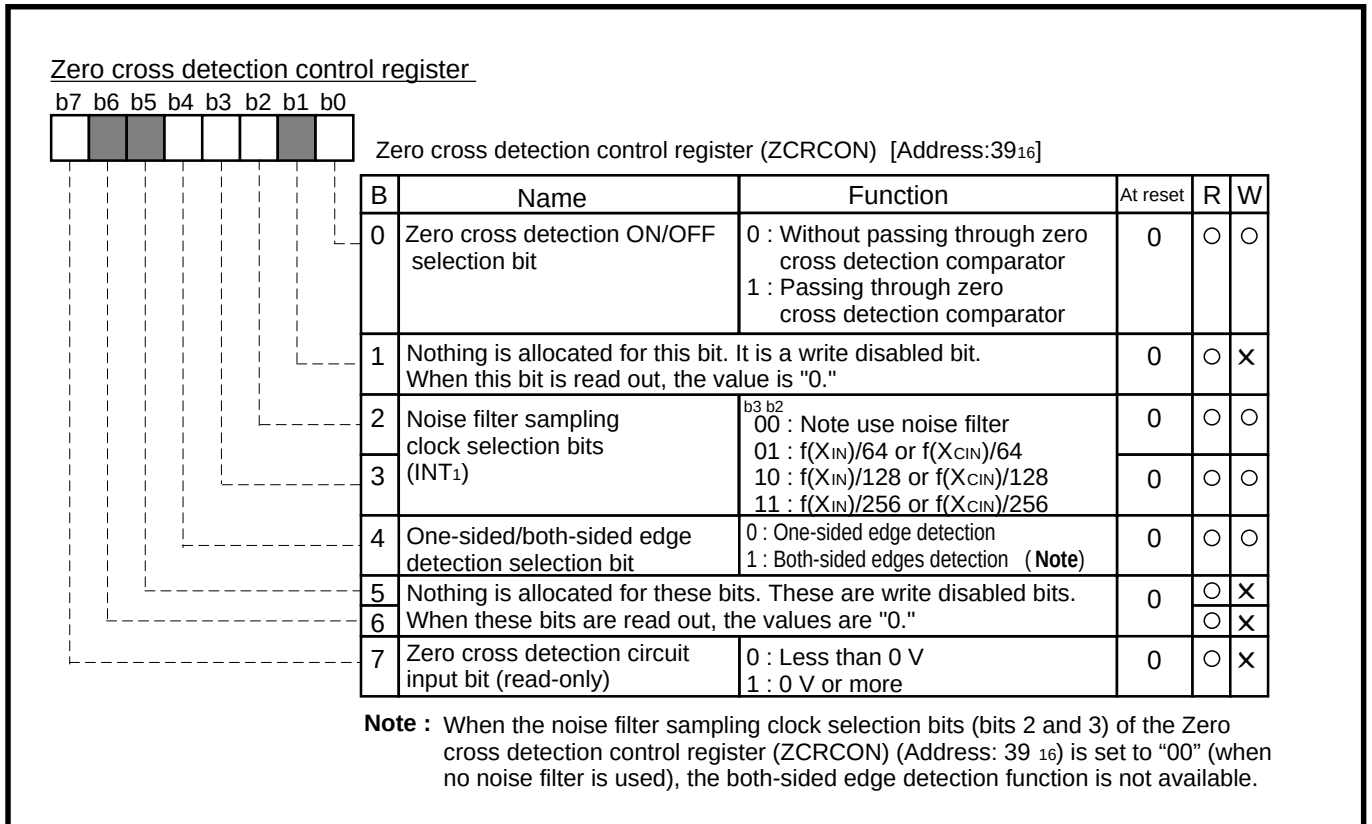


Fig. 3.3.23 Structure of Zero cross detection control register

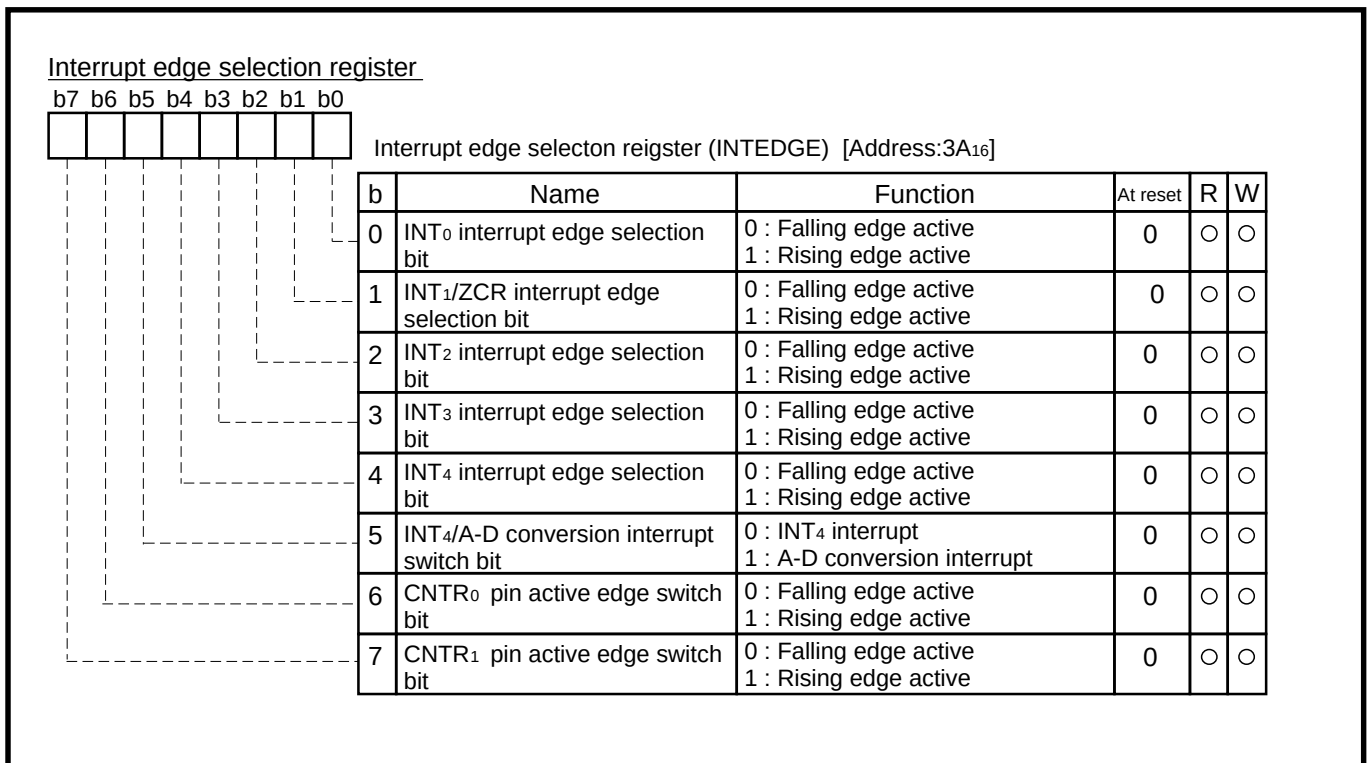


Fig. 3.3.24 Structure of Interrupt edge selection register

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3819 Group 3.3 Control registers

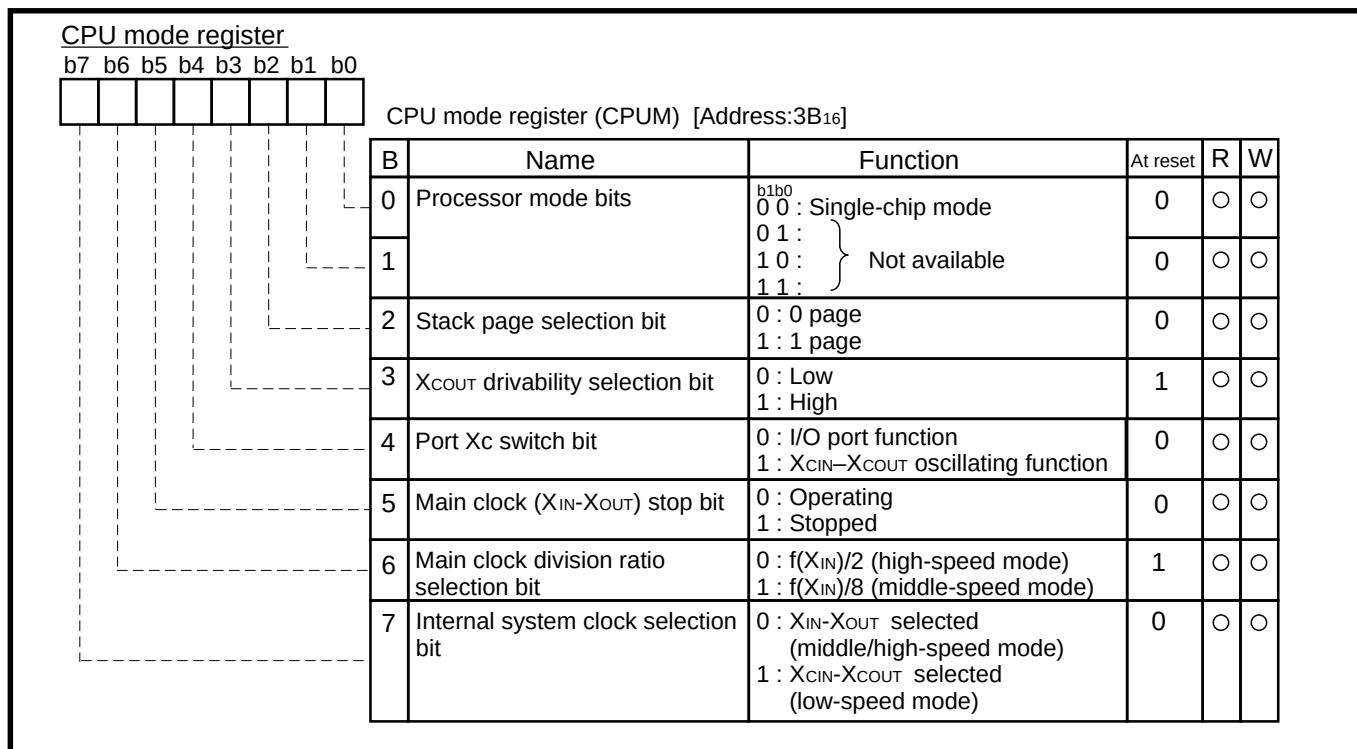


Fig. 3.3.25 Structure of CPU mode register

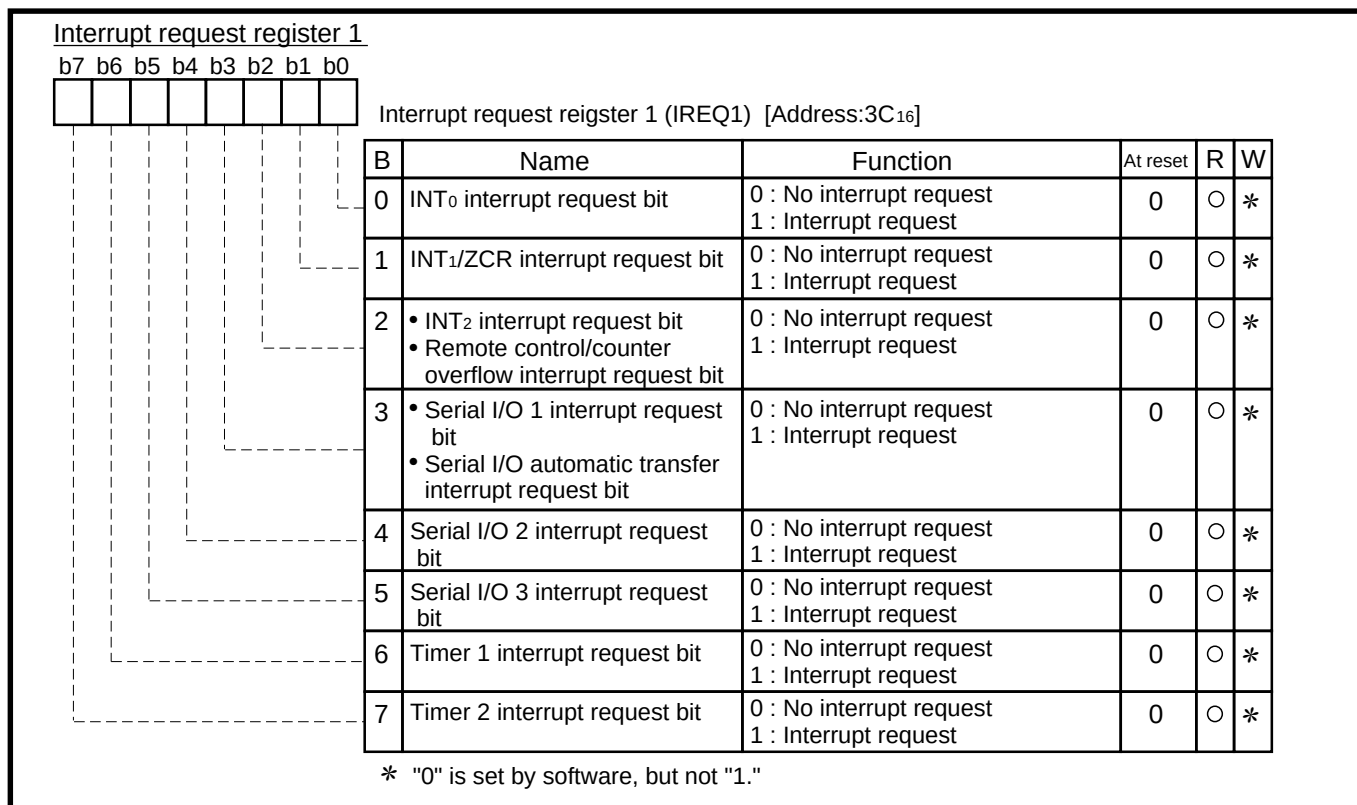
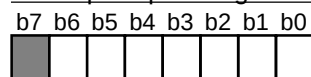


Fig. 3.3.26 Structure of Interrupt request register 1

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3819 Group 3.3 Control registers

Interrupt request register 2



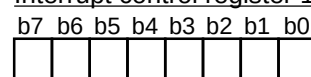
Interrupt request register 2 (IREQ2) [Address:3D16]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	Timer 4 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	Timer 5 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	Timer 6 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	INT ₃ interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	• INT ₄ interrupt request bit • A-D conversion interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	• FLD blanking interrupt request bit • FLD digit interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	*

* "0" is set by software, but not "1."

Fig. 3.3.27 Structure of Interrupt request register 2

Interrupt control register 1



Interrupt control register 1 (ICON1) [Address:3E16]

B	Name	Function	At reset	R	W
0	INT ₀ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT ₁ /ZCR interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	• INT ₂ interrupt enable bit • Remote control/counter overflow interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	• Serial I/O 1 interrupt enable bit • Serial I/O automatic transfer interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Serial I/O 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Serial I/O 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 3.3.28 Structure of Interrupt control register 1

3. APPENDIX

Interrupt control register 2

b7 b6 b5 b4 b3 b2 b1 b0

0							
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Interrupt control register 2 (ICON2) [Address:3F16]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Timer 4 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Timer 5 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Timer 6 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT ₃ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	• INT ₄ interrupt enable bit • A-D conversion interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	• FLD blanking interrupt enable bit • FLD digit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix this bit to "0."		0	○	○

Fig. 3.3.29 Structure of Interrupt control register 2

3. APPENDIX

3.4 Mask ROM ordering method

3.4 Mask ROM ordering method

GZZ-SH07-32B <33B0 >

740 FAMILY MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M38197MA-XXXFP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked *.

*	Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM

--	--	--	--

(hexadecimal notation)

EPROM type (indicate the type used)

☐	27512
EPROM address	
0000 ₁₆	Product name ASCII code : "M38197MA -"
000F ₁₆	
0010 ₁₆	
607F ₁₆	data ROM 40830 bytes
6080 ₁₆	
FFFD ₁₆	
FFFE ₁₆	
FFFF ₁₆	

In the address space of the microcomputer, the internal ROM area is from address 6080₁₆ to FFFD₁₆. The reset vector is stored in addresses FFFC₁₆ and FFFD₁₆.

- (1) Set the data in the unused area (the shaded area of the diagram) to "FF₁₆".
- (2) The ASCII codes of the product name "M38197MA-" must be entered in addresses 0000₁₆ to 0008₁₆. And set the data "FF₁₆" in addresses 0009₁₆ to 000F₁₆.
The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000 ₁₆	'M' = 4 D ₁₆	0008 ₁₆	'-' = 2 D ₁₆
0001 ₁₆	'3' = 3 3 ₁₆	0009 ₁₆	FF ₁₆
0002 ₁₆	'8' = 3 8 ₁₆	000A ₁₆	FF ₁₆
0003 ₁₆	'1' = 3 1 ₁₆	000B ₁₆	FF ₁₆
0004 ₁₆	'9' = 3 9 ₁₆	000C ₁₆	FF ₁₆
0005 ₁₆	'7' = 3 7 ₁₆	000D ₁₆	FF ₁₆
0006 ₁₆	'M' = 4 D ₁₆	000E ₁₆	FF ₁₆
0007 ₁₆	'A' = 4 1 ₁₆	000F ₁₆	FF ₁₆

3. APPENDIX

3.4 Mask ROM ordering method

GZZ-SH07-32B <33B0 >

740 FAMILY MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M38197MA-XXXFP MITSUBISHI ELECTRIC

Mask ROM number	
-----------------	--

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27512
The pseudo-command	*=△\$0000 .BYTE△ 'M38197MA-'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

* 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (100P6S for M38197MA-XXXFP) and attach it to the mask ROM confirmation form.

* 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the XIN-XOUT oscillator?

- | | |
|---|---|
| ☐ Ceramic resonator | ☐ Quartz crystal |
| ☐ External clock input | ☐ Other () |

At what frequency?

f(XIN) = MHz

(2) In which operation mode will you use your microcomputer ?

- | | |
|--|--|
| ☐ Single-chip mode | ☐ Memory expansion mode |
| ☐ Microprocessor mode | |

* 4. Comments

3. APPENDIX

3819 Group 3.5 Mark specification form

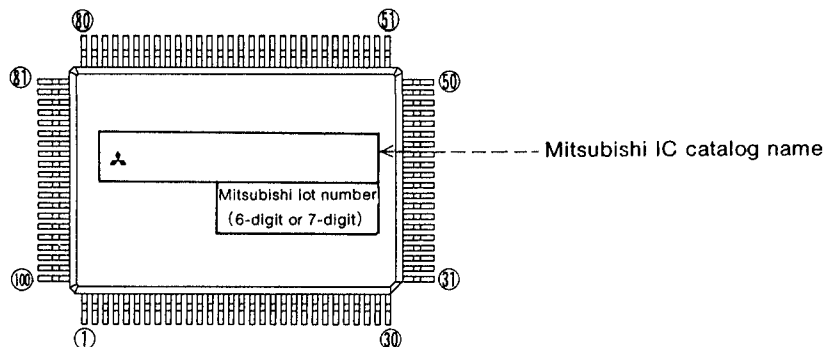
3.5 Mark specification form

100P6S (100-PIN QFP) MARK SPECIFICATION FORM

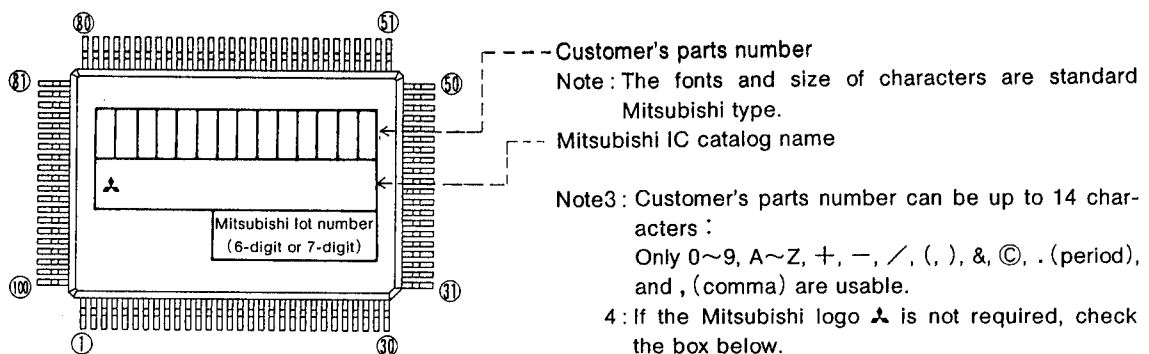
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



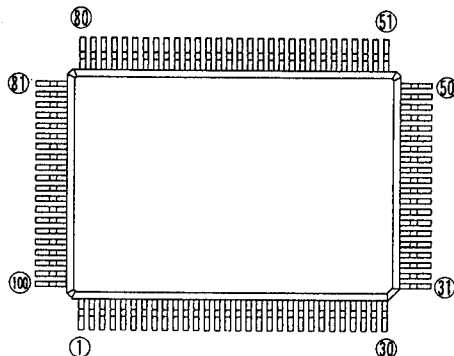
B. Customer's Parts Number + Mitsubishi Catalog Name



Note1: The mark field should be written right aligned.

2: The fonts and size of characters are standard Mitsubishi type.

C. Special Mark Required



Note1: If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and mask ROM number (3-digit) are always marked.

2: If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

☐

The standard Mitsubishi font is used for all characters except for a logo.

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3.6 Package outline

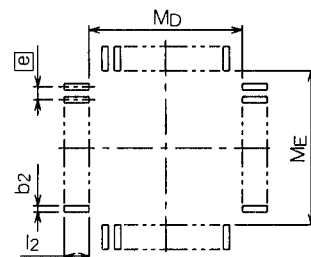
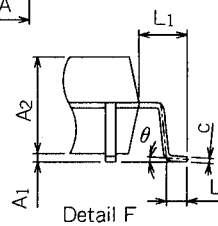
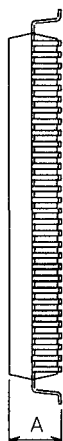
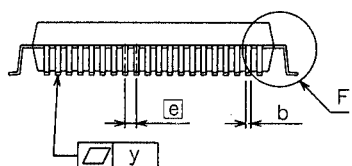
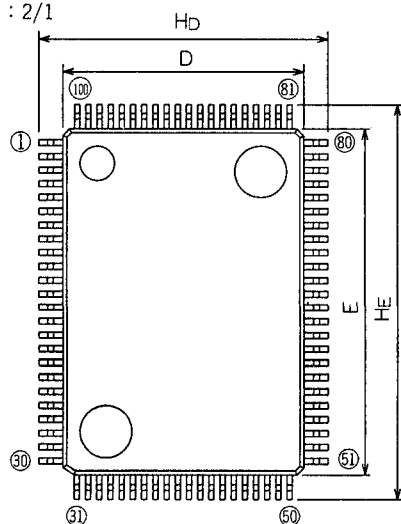
3.6 Package outline

100P6S-A

Plastic 100pin 14X20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)
*QFP100-P-1420	—	1.58

Scale : 2/1



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A1	0	0.1	0.2
A2	—	2.8	—
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	—	0.65	—
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	—	1.4	—
y	—	—	0.1
θ	0°	—	10°
b2	—	0.35	—
l2	1.3	—	—
MD	—	14.6	—
ME	—	20.6	—

3819 Group

3.7 Memory map

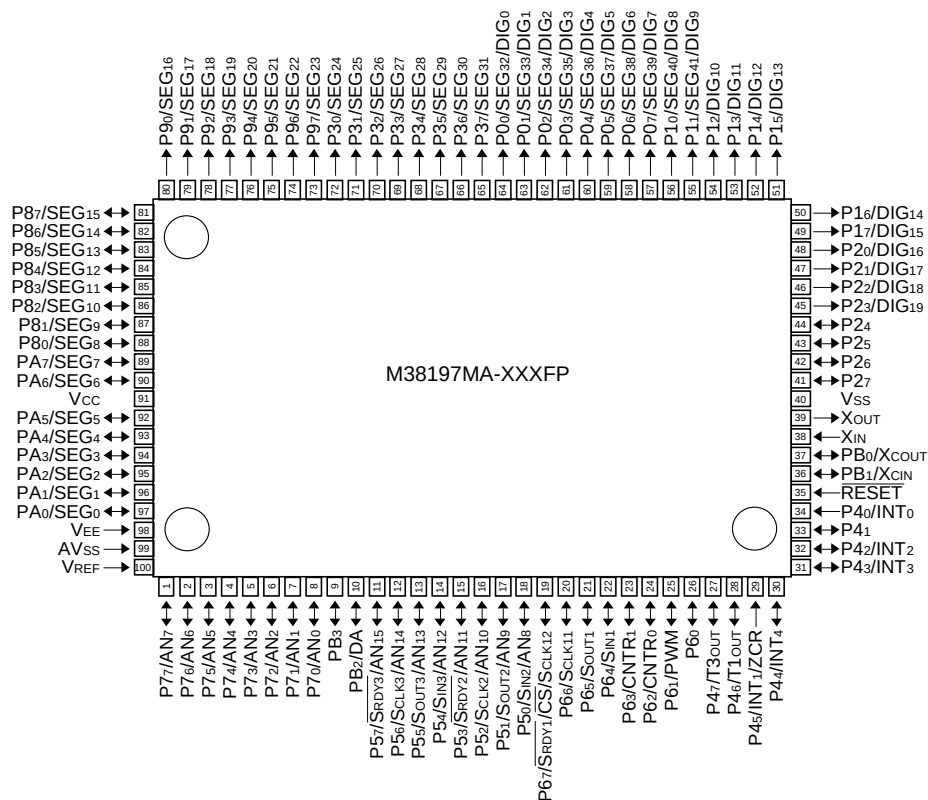
3.7 Memory map

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Timer 1 (T1)
0001 ₁₆		0021 ₁₆	Timer 2 (T2)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer 3 (T3)
0003 ₁₆		0023 ₁₆	Timer 4 (T4)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Timer 5 (T5)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer 6 (T6)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Serial I/O3 register (SIO3)
0007 ₁₆		0027 ₁₆	Timer 6 PWM register (T6PWM)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Timer 12 mode register (T12M)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	Timer 34 mode register (T34M)
000A ₁₆	Port P5 (P5)	002A ₁₆	Timer 56 mode register (T56M)
000B ₁₆	Port P5 direction register (P5D)	002B ₁₆	D-A conversion register (DA)
000C ₁₆	Port P6 (P6)	002C ₁₆	AD-DA control register (ADCON)
000D ₁₆	Port P6 direction register (P6D)	002D ₁₆	A-D conversion register (AD)
000E ₁₆	Port P7 (P7)	002E ₁₆	
000F ₁₆	Port P7 direction register (P7D)	002F ₁₆	
0010 ₁₆	Port P8 (P8)	0030 ₁₆	Interrupt interval determination register (IID)
0011 ₁₆	Port P8 direction register (P8D)	0031 ₁₆	Interrupt interval determination control register (IIDCON)
0012 ₁₆	Port P9 (P9)	0032 ₁₆	Port P0 segment/digit switch register (P0SDR)
0013 ₁₆		0033 ₁₆	Port P2 digit/port switch register (P2DPR)
0014 ₁₆	Port PA (PA)	0034 ₁₆	Port P8 segment/port switch register (P8SPR)
0015 ₁₆	Port PA direction register (PAD)	0035 ₁₆	Port PA segment/port switch register (PASPR)
0016 ₁₆	Port PB (PB)	0036 ₁₆	FLDC mode register 1 (FLDM1)
0017 ₁₆	Port PB direction register (PBD)	0037 ₁₆	FLDC mode register 2 (FLDM2)
0018 ₁₆	Serial I/O automatic transfer data pointer (SIODP)	0038 ₁₆	FLD data pointer (FLDDP)
0019 ₁₆	Serial I/O1 control register (SIO1CON)	0039 ₁₆	Zero cross detection control register (ZCRCON)
001A ₁₆	Serial I/O automatic transfer control register (SIOAC)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	Serial I/O1 register (SIO1)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Serial I/O automatic transfer interval register (SIOAI)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆	Serial I/O2 control register (SIO2CON)	003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆	Serial I/O3 control register (SIO3CON)	003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆	Serial I/O2 register (SIO2)	003F ₁₆	Interrupt control register 2 (ICON2)

3. APPENDIX

3819 Group 3.8 Pin configuration

3.8 Pin configuration



Package type : 100P6S-A
100-pin plastic-molded QFP

**MITSUBISHI SEMICONDUCTORS
USER'S MANUAL
3819 Group**

Mar. First Edition 1995

Edited by
Committee of editing of Mitsubishi Semiconductor USER'S MANUAL

Published by
Mitsubishi Electric Corp., Semiconductor Marketing Division

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User's Manual

3819 Group



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