GRADE A

MESC TECHNICAL NEWS

No. M7700-66-9912

Corrections and Supplementary Explanation for "7751 Group User's Manual" (REV. C)

This news includes a few corrections and supplementary explanation for "7751 Group User's Manual".

And also, this news includes the information previously announced by the MESC TECHNICAL NEWS (No. M7700-59-9912, Corrections and Supplementary Explanation for "7751 Group User's Manual" REV. B). ★ represents the new information.

The information about the product expansion, electrical characteristics, and development support tools will not be announced by the MESC TECHNICAL NEWS, even if the above information is updated.
So, for the product expansion, electrical characteristics, and development support tools, please refer to the latest version of the following documents in our web site:

- Product Expansion
  Mitsubishi Microcomputers General Catalog❋
- Electrical Characteristics
  Datasheets
- Development Support Tools
  Datasheets
  Microcomputers Development Support Tools Catalog❋
  Microcomputers Development Support Tools Accessory Guide

Please Visit Our Web Site.

- Mitsubishi MCU Technical Information (http://www.infomicom.mesc.co.jp/indexe.htm)
- Mitsubishi Microcomputer Development Support Tools
  (http://www.tool-spt.mesc.co.jp/index_e.htm)

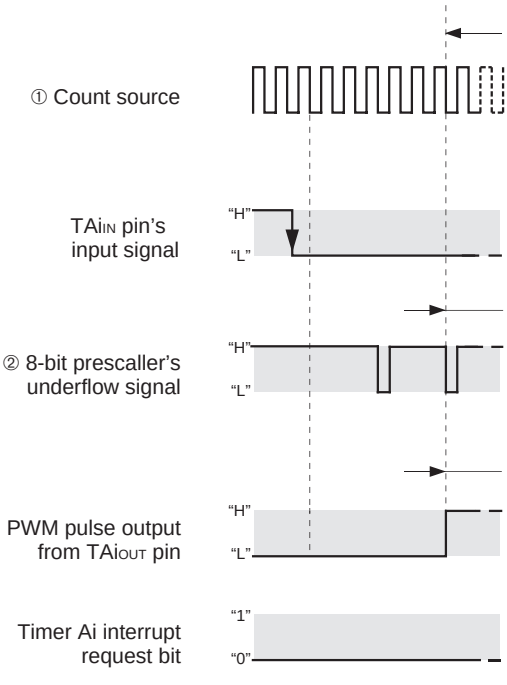
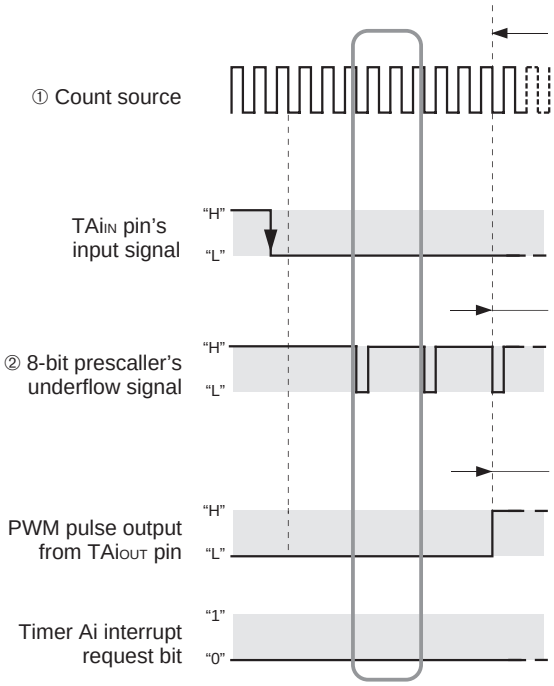
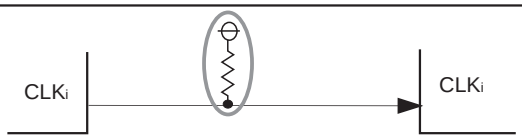
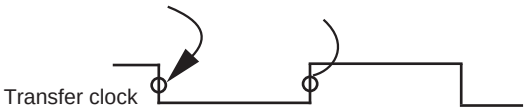
❋ The printed version is also released.

Note: For products not included in the above web site, refer to "1996 MITSUBISHI SEMICONDUCTORS DATA BOOK ⟨SINGLE-CHIP 16-BIT MICROCOMPUTERS⟩ Vol. 1 to 2."

Corrections and Supplementary Explanation for “7751 Group User’s Manual” (REV.C) No.1

<table>
<tr><th>Page</th><th>Error</th><th>Correction</th></tr>
<tr><td>P2-8
(2) Bit 1:
Zero flag (Z)</td><td>Note: This flag is invalid in the decimal mode addition (the ADC instruction).</td><td>Note: This flag is invalid in the decimal mode addition (the ADC instruction) and subtraction (the SBC instruction).</td></tr>
<tr><td>P2-27
Fig. 2.5.4,
P12-7
Fig.12.1.4,
P13-12
Fig. 13.2.1,
P20-28
address 5E16</td><td>Processor mode register 0 (Address 5E16)
<table><tr><th>Bit</th><th>Bit name</th><th>Functions</th></tr><tr><td>4
5</td><td>Interrupt priority detection time select bits</td><td>b5 b4
0 0 : 7 cycles of ϕ
0 1 : 4 cycles of ϕ
1 0 : 2 cycles of ϕ
1 1 : Not selected.</td></tr></table></td><td>Processor mode register 0 (Address 5E16)
<table><tr><th>Bit</th><th>Bit name</th><th>Functions</th></tr><tr><td>4
5</td><td>Interrupt priority detection time select bits</td><td>b5 b4
0 0 : 7 cycles of ϕBIU
0 1 : 4 cycles of ϕBIU
1 0 : 2 cycles of ϕBIU
1 1 : Not selected.</td></tr></table></td></tr>
<tr><td>P4-13
Line 5</td><td>As the interrupt priority level detection time, normally select “2 cycles of internal clock ϕ.”</td><td>As the interrupt priority level detection time, normally select “2 cycles of ϕBIU.”</td></tr>
<tr><td>P4-13
Fig. 4.6.1</td><td>b5, b4
<table><tr><th>Interrupt priority detection time select bits</th></tr><tr><td>0 0 7 cycles of ϕ [(a) shown below]</td></tr><tr><td>0 1 4 cycles of ϕ [(b) shown below]</td></tr><tr><td>1 0 2 cycles of ϕ [(c) shown below]</td></tr></table>
ϕ •••
Note: Pulse exists when “2 cycles of ϕ” is selected.</td><td>b5, b4
<table><tr><th>Interrupt priority detection time select bits</th></tr><tr><td>0 0 7 cycles of ϕBIU [(a) shown below]</td></tr><tr><td>0 1 4 cycles of ϕBIU [(b) shown below]</td></tr><tr><td>1 0 2 cycles of ϕBIU [(c) shown below]</td></tr></table>
ϕBIU •••
Note: Pulse exists when “2 cycles of ϕBIU” is selected.</td></tr>
<tr><td>P4-26
Lines 2, 3</td><td>•••, 2 to 7 cycles of ϕ are required •••</td><td>•••, 2 to 7 cycles of ϕBIU are required •••</td></tr>
<tr><td>P4-26
Table 4.11.1</td><td><table><tr><th></th><th>Interrupt priority level detection time</th><th></th></tr><tr><td></td><td>7 cycles of ϕ</td><td></td></tr><tr><td></td><td>4 cycles of ϕ</td><td></td></tr><tr><td></td><td>2 cycles of ϕ</td><td></td></tr></table></td><td><table><tr><th></th><th>Interrupt priority level detection time</th><th></th></tr><tr><td></td><td>7 cycles of ϕBIU</td><td></td></tr><tr><td></td><td>4 cycles of ϕBIU</td><td></td></tr><tr><td></td><td>2 cycles of ϕBIU</td><td></td></tr></table></td></tr>
<tr><td>P5-44
Note 2</td><td>•••, the TAiOUT pin outputs “L” level of the PWM pulse which has the same width as set “H” level of the PWM pulse after a trigger generated. •••</td><td>•••, the TAiOUT pin outputs “L” level for a period of (1/fi) × (m + 1) × (n + 1) after a trigger generated. •••</td></tr>
</table>

Corrections and Supplementary Explanation for “7751 Group User’s Manual” (REV.C) No.2

Page	Error	Correction
P5-46 Fig. 5.6.6		
P7-30 Fig. 7.3.9		
P7-49 Line 2	...and reception starts at detecting ST.	...and transfer clock is generated at detecting ST, and reception starts.
P7-50 Fig. 7.4.11	 Reception started at falling of start bit	 Transfer clock is generated at falling of start bit, and reception starts.
P9-8 Line 6 and after	2. When the **STP** instruction (refer to **“Chapter 10. STOP MODE”**) is executed, Watchdog timer stops. When Watchdog timer is used to detect the program runaway, select “**STP** instruction disable” with mask option.	2. When the **STP** instruction (refer to **“CHAPTER 10. STOP MODE”**) is executed, the watchdog timer stops. Unexpected execution of the **STP** instruction code (DB_{16}) owing to a program runaway causes Watchdog timer to stop. Therefore, when the watchdog timer is used to detect a program runaway, we recommend the user to select “**STP** instruction disabled” with “**STP** instruction option” on “MASK ROM ORDER CONFIRMATION FORM.”

Corrections and Supplementary Explanation for "7751 Group User's Manual" (REV.C) No.3

Page	Error	Correction
P10-4 Last 3 lines before **"Note"**	**(Note)** ••• MSB becomes "0." For interrupts not to be accepted, •••	**(Note)** ••• MSB becomes "0." (When the level sense of an INT_i interrupt is used, an interrupt request is not retained. Therefore, if the level at the INT_i pin is invalid when the watchdog timer's MSB becomes "0," the interrupt request is not accepted.) For interrupts not to be accepted, •••
★ P20-35 **Note 4**	**4:** When supplying V_{SS} level to the CNV_{SS} pin, these pins remain set to the input mode until they are switched to the output mode by software after reset (until the pin function is switched in the case of the ϕ_1 pin in the memory expansion mode). While pins remain set to the input mode, consequently, voltage levels of pins are unstable, and a power source current can increase.	**4:** When V_{SS} level is applied to the CNV_{SS} pin, note the following: this pin functions as an input port from reset until the processor mode is switched to the memory expansion mode or microprocessor mode by software (in the case of the ϕ_1 pin in the memory expansion mode, until the pin function is switched). Therefore, a voltage level of this pin is undefined and the power source current may increase while this pin functions as an input port.
P20-63 First line	**(4) Wiring for CNV_{SS} (V_{PP}) pin of built-in PROM version**	**(4) Wiring for CNV_{SS} (V_{PP}) pin of built-in PROM version and flash memory version**
P20-63 Last line	••• built-in PROM. This may cause a program runaway.	••• built-in PROM. This may cause a program runaway. For the CNV_{SS} (V_{PP}) pin of the built-in flash memory version, the above caution is also applied.
P20-69 5. Setup for I/O ports	<Software protection> ● As for an input port, ••• equal or not. ● As for an output port, •••, rewrite data to its port Pi register periodically. ● Rewrite data to port Pi direction registers periodically.	<Software protection> ● As for an input port, ••• equal or not. ● As for an output port, •••, rewrite (**Note**) data to its port Pi register periodically. ● Rewrite (**Note**) data to port Pi direction registers periodically. **Note:** Be sure to use the **LDM** or **STA** instruction for the above rewriting.
P20-72 [Q] Last line	● The interrupt ••• 2 cycles of ϕ.	● The interrupt ••• 2 cycles of ϕ_{BIU}.