GRADE A

MESC TECHNICAL NEWS

No. M7700-65-9912

Corrections and Supplementary Explanation for "7733/7735/7736 Group User's Manual" (REV. B)

This news includes a few corrections and supplementary explanation for "7733/7735/7736 Group User's Manual".

And also, this news includes the information previously announced by the MESC TECHNICAL NEWS (No. M7700-37-9803, Corrections and Supplementary Explanation for "7733/7735/7736 Group User's Manual" REV. A).

Notes 1: ★ represents the new information.
2: ☆ represents the information corrected only in the PDF version, not in the printed version (No. H-EF490-A) .

As previously announced by the MESC TECHNICAL NEWS (No. M7700-40-9809), the specifications of the 7733/7735/7736 Group MCUs have been revised. The revised points for the 7733/7735/7736 Group User's Manual are described on the last three pages of this news. For details of this revision, please refer to the MESC TECHNICAL NEWS, No. M7700-40-9809.

The information about the product expansion, electrical characteristics, and development support tools will not be announced by the MESC TECHNICAL NEWS, even if the above information is updated.
So, for the product expansion, electrical characteristics, and development support tools, please refer to the latest version of the following documents in our web site:

- Product Expansion
  Mitsubishi Microcomputers General Catalog❋
- Electrical Characteristics
  Datasheets
- Development Support Tools
  Datasheets
  Microcomputers Development Support Tools Catalog❋
  Microcomputers Development Support Tools Accessory Guide

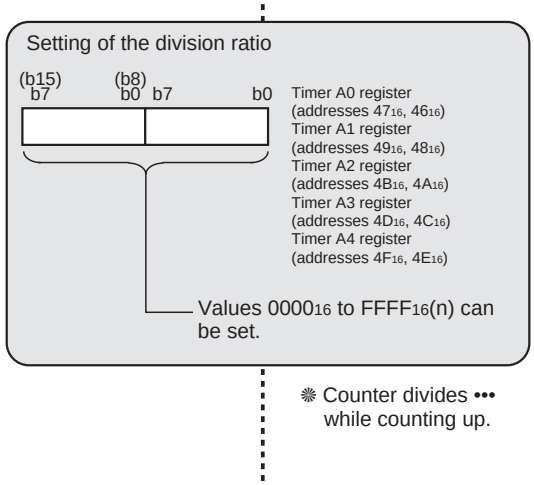
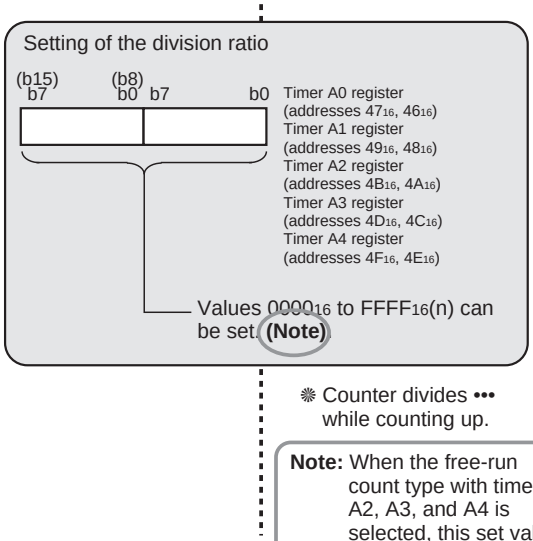
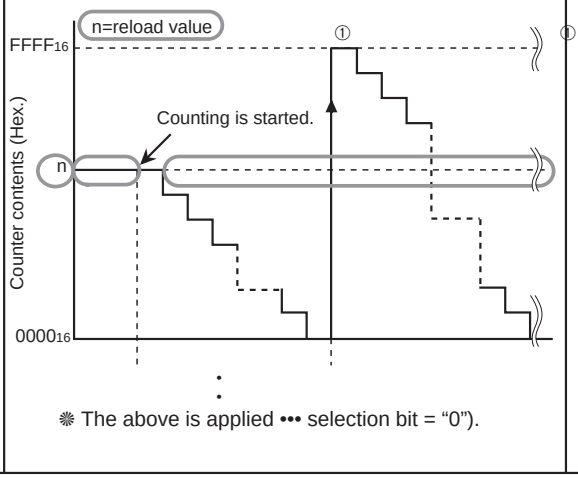
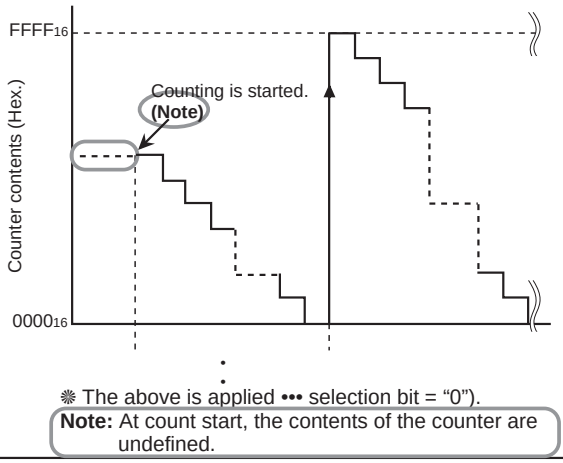
Please Visit Our Web Site.

- Mitsubishi MCU Technical Information (http://www.infomicom.mesc.co.jp/indexe.htm)
- Mitsubishi Microcomputer Development Support Tools
  (http://www.tool-spt.mesc.co.jp/index_e.htm)

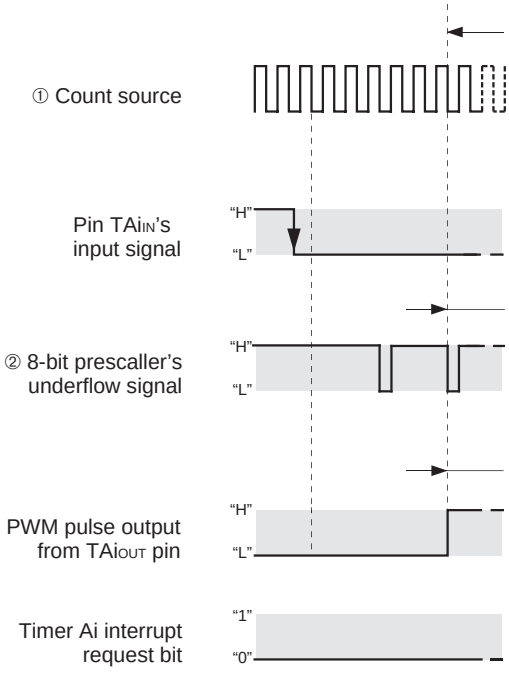
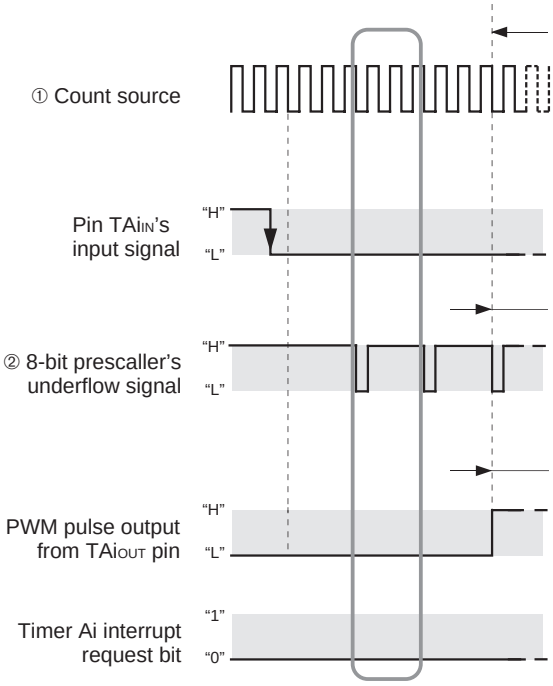
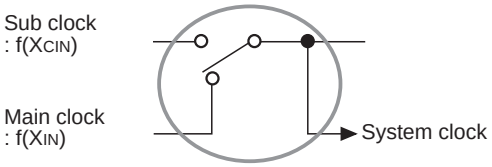
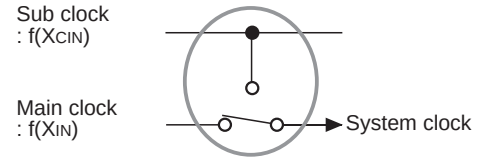
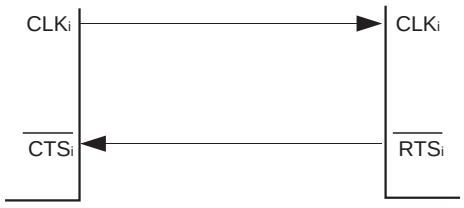
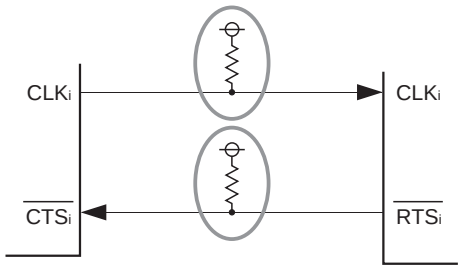
❋ The printed version is also released.

Notes 3: For products not included in the above web site, refer to "1996 MITSUBISHI SEMICONDUCTORS DATA BOOK 〈SINGLE-CHIP 16-BIT MICROCOMPUTERS〉 Vol. 1 to 2."

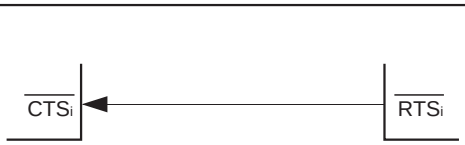
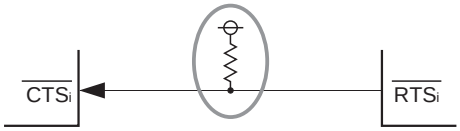
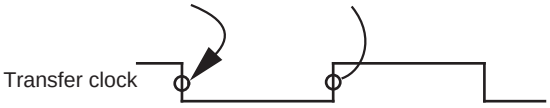
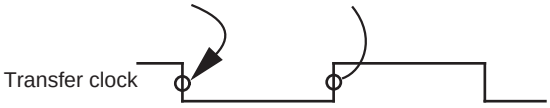
Corrections and Supplementary Explanation for “7733/35/36 Group User’s Manual” (REV. B) No. 1

<table>
<tr><th>Page</th><th>Error</th><th>Correction</th></tr>
<tr><td>☆ PART 1
P2-8
(2) Bit 1:
Zero flag (Z)</td><td>This flag is ignored for an addition instruction in the decimal mode (the ADC instruction).</td><td>This flag is ignored for an addition and subtraction instructions (the ADC and the SBC instructions) in the decimal mode.</td></tr>
<tr><td>★ PART 1
P2-19
Fig. 2.4.1,
P21-31
address 63₁₆</td><td>Procedure
••••••••••••••••••••••••••••••••
Note: When changing ••• this procedure.</td><td>Procedure
••••••••••••••••••••••••••••••••
Note: When changing ••• this procedure.
The occurrence of an interrupt between ① and ② makes writing invalid.
If there is a possibility that an interrupt occurs at this timing, be sure to read and confirm this bit’s value after writing.</td></tr>
<tr><td>★ PART 1
P6-23
Fig. 6.4.3</td><td> 
</td><td> 
</td></tr>
<tr><td>★ PART 1
P6-27
Fig. 6.4.7</td><td> 
</td><td> 
</td></tr>
</table>

Corrections and Supplementary Explanation for “7733/35/36 Group User’s Manual” (REV. B) No. 2

	Page	Error	Correction
★ ☆	PART 1 P6-47 Line 23	**2:** •••, pin TAiOUT outputs “L” level of which width is the same as the PWM pulse’s “H” level width which was set. •••	**2:** •••, after a trigger occurs (☆), pin TAiOUT outputs “L” level for a period of (1/fi) × (m + 1) × (n + 1). ••• (★)
★	PART 1 P6-49 Fig. 6.6.6		
☆	PART 1 P7-31 Line 7	The timer Bi overflow flag is cleared to “0” when a value is written to the timer Bi mode register with the count start flag = “1.”	The timer Bi overflow flag is cleared to “0” at the next count timing of the count source when a value is written to the timer Bi mode register with the count start flag = “1.”
★	PART 1 P7-36 Fig. 7.6.2, P17-55 Fig. 17.5.3		
★	PART 1 P8-32 Line 4, P8-39 Lines 3 and 4, P8-53 Lines 3 and 4	••• after one cycle of the transfer clock has passed.	••• after a maximum of 1 cycle of the transfer clock has passed.
☆	PART 1 P8-40 Fig. 8.3.13		

Corrections and Supplementary Explanation for “7733/35/36 Group User’s Manual” (REV. B) No. 3

	Page	Error	Correction
☆	PART 1 P8-46 Table 8.4.4	14400 | f_2 | 52($3F_{16}$) | 14490.57 | 53(40_{16}) | 14467.59	14400 | f_2 | 52(34_{16}) | 14490.57 | 53(35_{16}) | 14467.59
☆	PART 1 P8-59 Line 2	And then, reception is started when ST is detected.	And then, the transfer clock is generated when ST is detected, and reception is started.
☆	PART 1 P8-59 Fig. 8.4.11		
☆	PART 1 P8-60 Fig. 8.4.12	 Reception is started at the falling edge of start bit.	 The transfer clock is generated at the falling edge of start bit, and reception is started.
☆	PART 1 P8-62 Line 20	⑤ For the slave microcomputer whose address matches bits 6 to 0 in the receive data, clear the sleep mode. (Do not terminate the sleep mode for the other slave microcomputers.)	⑤ For the slave microcomputer whose address matches bits 6 to 0 in the receive data, terminate the sleep mode. (Do not terminate the sleep mode for the other slave microcomputers.)
★	PART 1 P10-9 Fig. 10.2.3, P11-5 Fig. 11.2.4, P14-9 Fig. 14.3.4, P21-36 (When writing ••), PART 2 P10-3 Fig. 10.2.3, P11-3 Fig. 11.2.4, P14-3 Fig. 14.3.4, PART3 P20-11 for PDF version, P20-10 for printed version (When writing ••)	(Under Figure)	(Under Figure) **Note:** The occurrence of an interrupt in the above procedure makes writing invalid. If there is a possibility that an interrupt occurs at this timing, be sure to read and confirm this bit’s value after writing.
★	PART 1 P10-10 Line 13 and after	4. When the **STP** instruction (Refer to chapter **“**11. **STOP AND WAIT MODES”**) is executed, the watchdog timer stops operating. For the system where the watchdog timer is used to detect a program runaway, select “**STP** instruction disabled” with “**STP** instruction option” on “MASK ROM ORDER CONFIRMATION FORM.”	4. When the **STP** instruction (refer to **“CHAPTER 11. STOP AND WAIT MODES”**) is executed, the watchdog timer stops operating. Unexpected execution of the **STP** instruction code (DB_{16}) owing to a program runaway causes Watchdog timer to stop. Therefore, when Watchdog timer is used to detect a program runaway, we recommend the user to select “**STP** instruction disabled” with “**STP** instruction option” on “MASK ROM ORDER CONFIRMATION FORM.”

Corrections and Supplementary Explanation for “7733/35/36 Group User’s Manual” (REV. B) No. 4

<table>
<tr><th></th><th>Page</th><th>Error</th><th>Correction</th></tr>
<tr><td>★</td><td>PART 1
P11-10
Lines 10, 11</td><td>priority after ••• MSB becomes “0.” For interrupts which have no need to be accepted, •••</td><td>priority after ••• MSB becomes “0.” (When the level sense of an INTi interrupt is used, an interrupt request is not retained. Therefore, if the level at the INTi pin is invalid when the watchdog timer’s MSB becomes “0,” the interrupt request is not accepted.)
For interrupts which have no need to be accepted, •••</td></tr>
<tr><td>☆</td><td>PART 1
P11-17
Table 11.4.3</td><td>
<table>
<tr><th rowspan="2">Interrupt</th><th colspan="2">Conditions for each function which generates interrupt request</th></tr>
<tr><th>when clocks f2 and f512 are stopped</th><th>when clocks f2 and f512 are not stopped</th></tr>
<tr><td>A-D conversion interrupt</td><td>Disabled</td><td>Enabled</td></tr>
</table>
</td><td>
<table>
<tr><th rowspan="2">Interrupt</th><th colspan="2">Conditions for each function which generates interrupt request</th></tr>
<tr><th>when clocks f2 and f512 are stopped</th><th>when clocks f2 and f512 are not stopped</th></tr>
<tr><td>A-D conversion interrupt</td><td>Disabled</td><td>Enabled in one-shot mode and single sweep mode</td></tr>
</table>
</td></tr>
<tr><td>★</td><td>PART 1
P17-43
Lines 1, 2</td><td>1. The watchdog timer stops counting hen the STP instruction is executed, the watchdog timer stops operating. For systems which use the watchdog timer, select “STP instruction disabled” with “STP instruction option” on “MASK ROM ORDER CONFIRMATION FORM.”</td><td>1. The watchdog timer stops counting hen the STP instruction is executed, the watchdog timer stops operating. Unexpected execution of the STP instruction code (DB16) owing to a program run-away causes Watchdog timer to stop. Therefore, for systems which use the watchdog timer, we recommend the user to select “STP instruction disabled” with “STP instruction option” on “MASK ROM ORDER CONFIRMATION FORM.”</td></tr>
<tr><td>★</td><td>PART 1
P21-69
5. Setup for I/O ports
<Software></td><td>● Read the data of •••equal.
● Periodically rewrite data •••, due to noise.
● Rewrite data to ••• periodically.</td><td>● Read the data of ••• are equal.
● Periodically rewrite (Note) data •••, due to noise.
● Rewrite (Notes 1, 2) data to ••• periodically.

Notes 1: Be sure to use the LDM or STA instruction for the above rewriting.
2: Rewrite the direction registers of ports P4–P8, P9, and P10 as follows:
(1) Disable interrupts with the SEI instruction, etc.
(2) Write dummy data to addresses 1A16 and 1B16 (when rewriting an even address, write data to address 1A16; when an odd address, write to address 1B16).
(3) Rewrite the targeted direction register.

(Refer to Technical News No. 7700-48-9906 for details of Note 2 and a program example.)</td></tr>
</table>

Corrections and Supplementary Explanation for “7733/35/36 Group User’s Manual” (REV. B) No. 5

<table>
<tr><th>Page</th><th>Error</th><th>Correction</th></tr>
<tr><td>★ PART 1
P21-80
☆ A ②, ③</td><td>A
② When writing data ••• procedure shown below.
• When writing to bits 0 to 2
Write data “01010101_{16}.” (LDM instruction)
Next instruction
Write data “$00000XXX_{16}$.” (LDM instruction)
Bits 0 to 2 are set.
③ When writing data ••• procedure shown below.
Write data “01010101_{16}.” (LDM instruction)
Next instruction
Write data “$00001XXX_{16}$.” (LDM instruction)
Bits 0 to 2 are set.</td><td>A
② When writing data ••• procedure shown below.
• When writing to bits 0 to 2
Write data “01010101_{2}.” (LDM instruction)
Next instruction
Write data “$00001XXX_{2}$.” (LDM instruction)
(Note 1)
Bits 0 to 2 are set.
Notes 1: In the case of the 7735 Group, write data “$00000XXX_{2}$.” (☆)
2: The occurrence of an interrupt in the above procedure makes writing invalid. If there is a possibility that an interrupt occurs at this timing, be sure to read and confirm this bit’s value after writing. (★)
③ When writing data ••• procedure shown below.
Write data “01010101_{2}.” (LDM instruction)
Next instruction
Write data “$00000XXX_{2}$.” (LDM instruction)
Bits 0 to 2 are set.
Note 3 : The occurrence of an interrupt in the above procedure makes writing invalid. If there is a possibility that an interrupt occurs at this timing, be sure to read and confirm this bit’s value after writing.</td></tr>
<tr><td>★ PART 2
P17-14
Table 17.1.5</td><td>Memory | Usage condition
EPROM | $2 \cdot f(f_2) \leq 20$ MHz
:</td><td>Memory | Usage condition
EPROM | $2 \cdot f(f_2) \leq 25$ MHz
:</td></tr>
</table>

Revised Points for “7733/7735/7736 Group User’s Manual” (REV. A) No. 1

<table>
<tr><th>Page</th><th>Previous Version</th><th>Revised Version</th></tr>
<tr><td>☆ PART 1
Page 2-21
Fig. 2.4.1,

PART 1
Page 21-30</td><td>
<table>
<tr><th>Functions</th></tr>
<tr><td>b2 b1 b0 ROM size (addresses)
0 0 0 : 124 K (001000₁₆ to 01FFFF₁₆)
0 0 1 : 120 K (002000₁₆ to 01FFFF₁₆)
0 1 0 : Do not select.
0 1 1 : Do not select.
1 0 0 : Do not select.
1 0 1 : Do not select.
1 1 0 : 96 K (008000₁₆ to 01FFFF₁₆)
1 1 1 : 32 K (008000₁₆ to 00FFFF₁₆)</td></tr>
</table>
</td><td>
<table>
<tr><th>Functions</th></tr>
<tr><td>ROM size RAM size
0 0 0 : 124 Kbytes, 3968 bytes
0 0 1 : 120 Kbytes, 3968 bytes
0 1 0 : 60 Kbytes. 2048 bytes
0 1 1 : Do not select.
1 0 0 : 32 Kbytes. 2048 bytes
1 0 1 : 16 Kbytes. 2048 bytes
1 1 0 : 96 Kbytes, 3968 bytes
1 1 1 : Do not select.</td></tr>
</table>
</td></tr>
<tr><td></td><td>Notes 1: •••
2: When changing these bits, this change must be performed in an area which is internal ROM area before and after this change, for example addresses 008000₁₆ to 00FFFF₁₆. Also, when changing these bits, be sure to follow the procedure listed below.
3: In the M37733S4BFP, M37733S4LHP, M37735S4BFP, or M37735S4LHP, writing to address 63₁₆ is disabled.</td><td>Notes 1: •••
2: When changing these bits, this change must be performed in an area which is internal ROM area before and after this change, for example addresses 00C000₁₆ to 00FFFF₁₆. Also, when changing these bits, be sure to follow the procedure listed below.
3: This figure is applied only to the M37733MHBXXXFP. For the other microcomputers, please refer to the latest datasheets.</td></tr>
<tr><td>☆ PART 1
Page 2-23
Fig. 2.4.3,
PART 1
Page 21-3
Fig. 2,

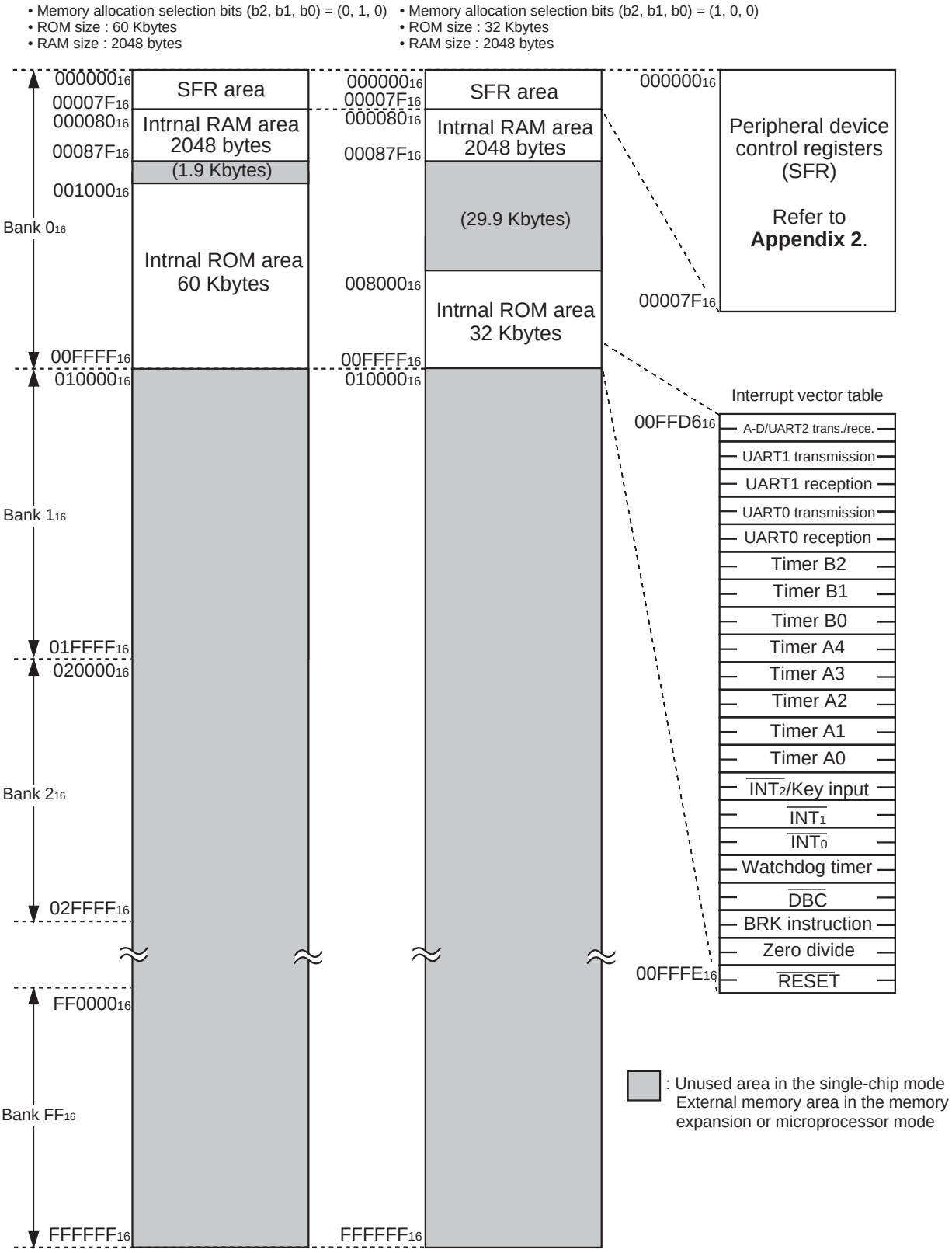
PART 2
Page 21-4
Fig. 2,

PART 3
Page 20-4
Fig. 2</td><td>(Omitted)</td><td>See pages 2 and 3.</td></tr>
<tr><td>☆ PART 1
Page 19-4
Table 19.1.3</td><td>
<table>
<tr><th colspan="3">Memory allocation selection bits</th><th rowspan="2">Programmable area</th></tr>
<tr><th>b2</th><th>b1</th><th>b0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>01000₁₆–1FFFF₁₆</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>02000₁₆–1FFFF₁₆</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>08000₁₆–1FFFF₁₆</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>08000₁₆–0FFFF₁₆</td></tr>
</table>
</td><td>
<table>
<tr><th colspan="3">Memory allocation selection bits</th><th rowspan="2">Programmable area</th></tr>
<tr><th>b2</th><th>b1</th><th>b0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>01000₁₆–1FFFF₁₆</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>02000₁₆–1FFFF₁₆</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>01000₁₆–0FFFF₁₆</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>08000₁₆–0FFFF₁₆</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0C000₁₆–0FFFF₁₆</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>08000₁₆–1FFFF₁₆</td></tr>
</table>
</td></tr>
<tr><td>☆ PART 1
Page 21-87
Line 18</td><td>•••• addresses 008000₁₆ to 00FFFF₁₆.</td><td>•••• addresses 00C000₁₆ to 00FFFF₁₆.</td></tr>
</table>

Revised Points for “7733/7735/7736 Group User’s Manual” (REV. A) No. 2

Revised Version

☆

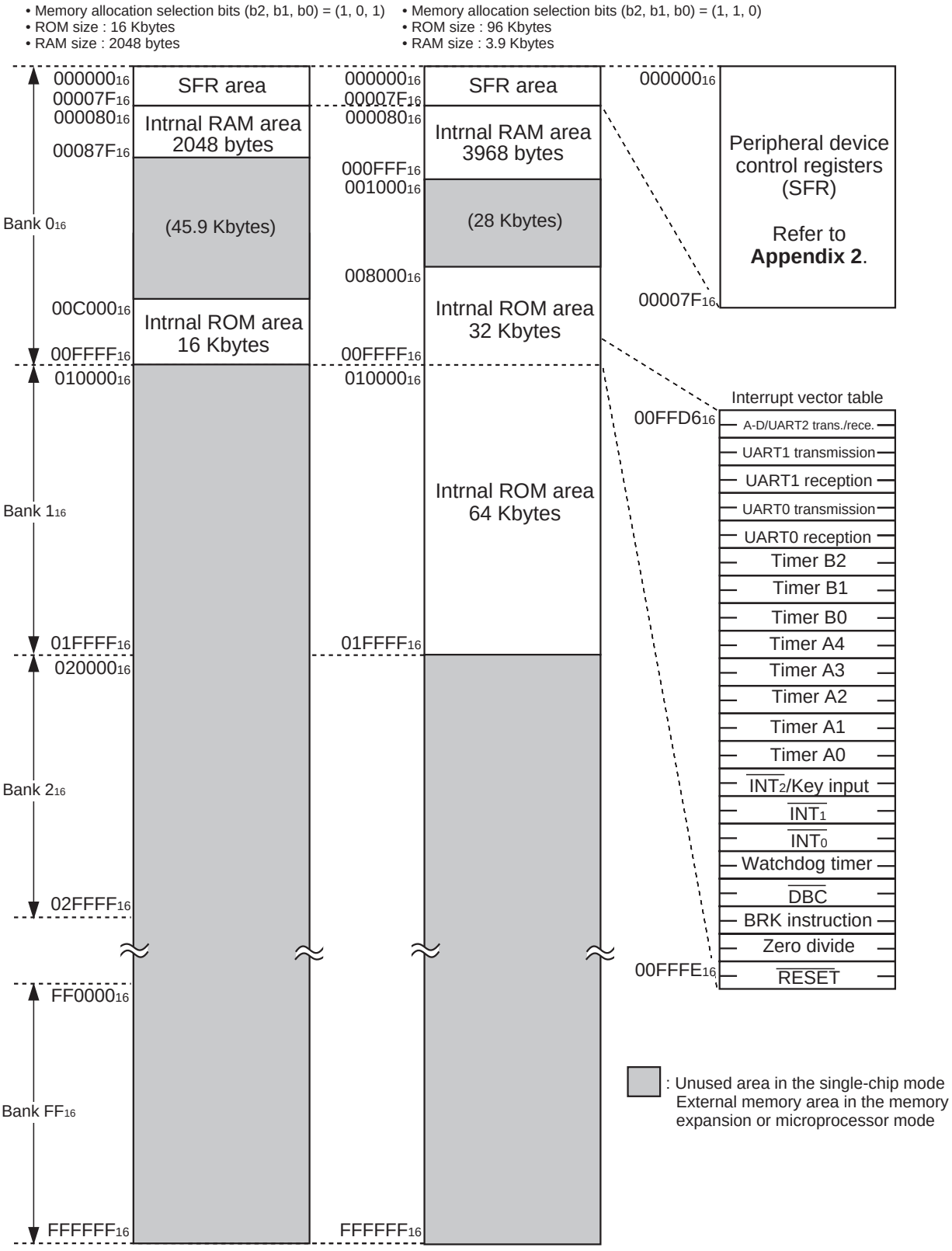


Notes 1: Access to internal ROM area is disabled in the microprocessor mode. (Refer to section **“2.5 Processor modes.”**)
2: Banks 10_{16} to FF_{16} cannot be accessed in the 7735 Group and in external bus mode B of the 7736 Group.

Revised Points for “7733/7735/7736 Group User’s Manual” (REV. A) No. 3

Revised Version

☆



Notes 1: Access to internal ROM area is disabled in the microprocessor mode. (Refer to section **“2.5 Processor modes.”**)
2: Banks 10_{16} to FF_{16} cannot be accessed in the 7735 Group and in external bus mode B of the 7736 Group.