GRADE A

MESC TECHNICAL NEWS

No. M7700-62-9912

Corrections and Supplementary Explanation for "7721 Group User's Manual" (REV. B)

This news includes a few corrections and supplementary explanation for "7721 Group User's Manual".

And also, this news includes the information previously announced by the MESC TECHNICAL NEWS (No. M7700-36-9803, Corrections and Supplementary Explanation for "7721 Group User's Manual" REV. A). ★ represents the new information.

The information about the product expansion, electrical characteristics, and development support tools will not be announced by the MESC TECHNICAL NEWS, even if the above information is updated.
So, for the product expansion, electrical characteristics, and development support tools, please refer to the latest version of the following documents in our web site:

- Product Expansion
  Mitsubishi Microcomputers General Catalog❋
- Electrical Characteristics
  Datasheets
- Development Support Tools
  Datasheets
  Microcomputers Development Support Tools Catalog❋
  Microcomputers Development Support Tools Accessory Guide

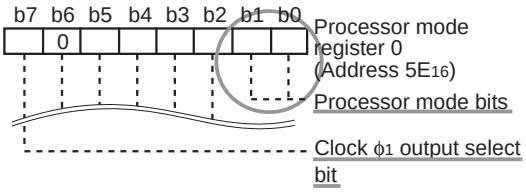
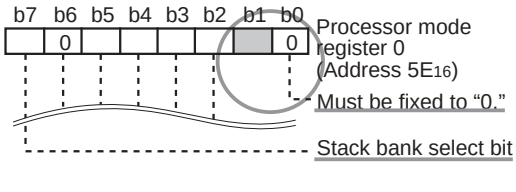
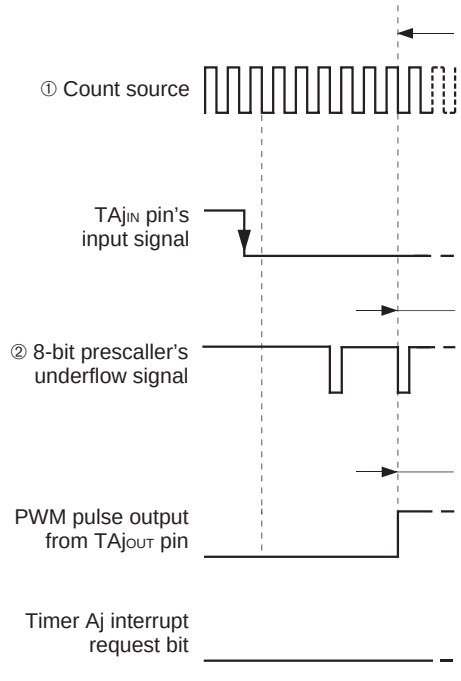
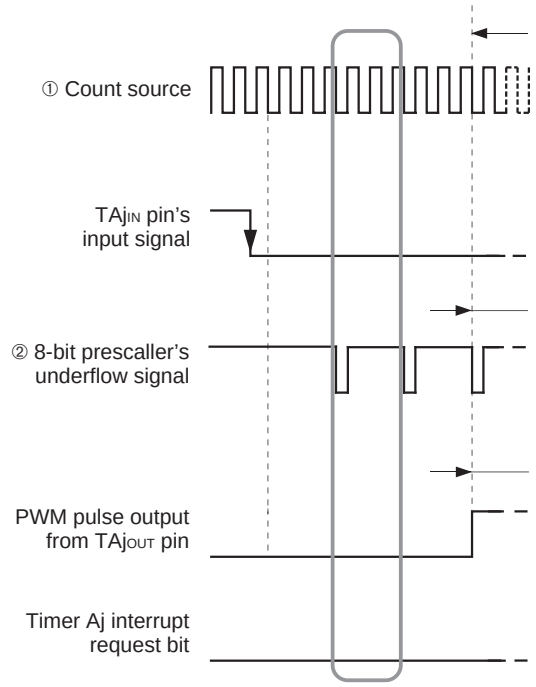
Please Visit Our Web Site.

- Mitsubishi MCU Technical Information (http://www.infomicom.mesc.co.jp/indexe.htm)
- Mitsubishi Microcomputer Development Support Tools
  (http://www.tool-spt.mesc.co.jp/index_e.htm)

❋ The printed version is also released.

Note: For products not included in the above web site, refer to "1996 MITSUBISHI SEMICONDUCTORS DATA BOOK ⟨SINGLE-CHIP 16-BIT MICROCOMPUTERS⟩ Vol. 1 to 2."

Corrections and Supplementary Explanation for “7721 Group User’s Manual” (REV. B) No. 1

	Page	Error	Correction
	P2-7 (2) Bit 1: Zero Flag	**Note**: This flag is invalid in the decimal mode addition (the **ADC** instruction).	**Note**: This flag is invalid in the decimal mode addition (the **ADC** instruction) and subtraction (the **SBC** instruction).
★	P5-6 Last 3 lines	in order of priority ••• MSB becomes “0.” For interrupts not to be accepted, •••	in order of priority ••• MSB becomes “0.” (When the level sense of an INT_i interrupt is used, an interrupt request is not retained. Therefore, if the level at the INT_i pin is invalid when the watchdog timer’s MSB becomes “0,” the interrupt request is not accepted.) For interrupts not to be accepted, •••
★	P7-12 Fig. 7.6.1	(1) Interrupt priotiry detection time select bits 	(1) Interrupt priotiry detection time select bits 
★	P8-39 Fig. 8.6.1, P17-22	<When operating as a 16-bit pulse width modulator> Bit: 15 to 0 Functions: These bits can be set to “0000_{16}” to “$FFFE_{16}$.” Assuming that the set value = n, the “ H” level width of the PWM pulse output from the TAj_{OUT} pin is expressed as follows: $\frac{n}{f_i}$ (PWM pulse period = $\frac{n^{16}-1}{f_i}$)	<When operating as a 16-bit pulse width modulator> Bit: 15 to 0 Functions: These bits can be set to “0000_{16}” to “$FFFE_{16}$.” Assuming that the set value = n, the “ H” level width of the PWM pulse output from the TAj_{OUT} pin is expressed as follows: $\frac{n}{f_i}$ (PWM pulse period = $\frac{2^{16}-1}{f_i}$)
★	P8-43 Last 2 lines	the TAj_{OUT} pin outputs “L” level which has the same width as “H” level width of the PWM pulse, which was set. •••	the TAj_{OUT} pin outputs “L” level for a period of (1/fi) × (m+1) × (n+1). •••
★	P8-45 Fig. 8.6.6		

Corrections and Supplementary Explanation for “7721 Group User’s Manual” (REV. B) No. 2

<table>
<tr><th>Page</th><th>Error</th><th>Correction</th></tr>
<tr><td>★ P11-21
Line 4,
P11-27
Lines 3 and 4,
P11-38
Lines 3 and 4</td><td>••• after 1 cycle of the transfer clock has passed. •••</td><td>••• after a maximum of 1 cycle of the transfer clock has passed. •••</td></tr>
<tr><td>P13-20
Table 13.3.3</td><td>
<table>
<tr><th colspan="2">Burst transfer mode
Level Sense</th><th>Cycle-steal transfer mode</th></tr>
<tr><td colspan="2">• “H”-level input to the DMAREQi pin
• Change of the TC pin’s input level from “H” to “L” (when the TC pin is valid)
•A write of “0” to the DMAi request bit
• A write of “0” to the DMAi enable bit</td><td>• Start of 1-unit transfer
• Change of the TC pin’s input level from “H” to “L” during DMA transfer (when the TC pin is valid)
• A write of “0” to the DMAi request bit
• A write of “0” to the DMAi enable bit</td></tr>
</table>
Note: While the DMAi enable bit is “0,”...
</td><td>
<table>
<tr><th colspan="2">Burst transfer mode
Level Sense</th><th>Cycle-steal transfer mode</th></tr>
<tr><td colspan="2">• “H”-level input to the DMAREQi pin
(Delete)</td><td>• Start of 1-unit transfer
• Change of the TC pin’s input level from “H” to “L” during DMA transfer (when the TC pin is valid)
• A write of “0” to the DMAi request bit
(Delete)</td></tr>
</table>
Note: (Delete)

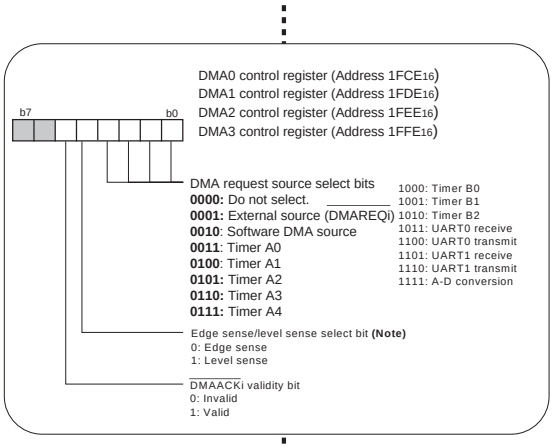
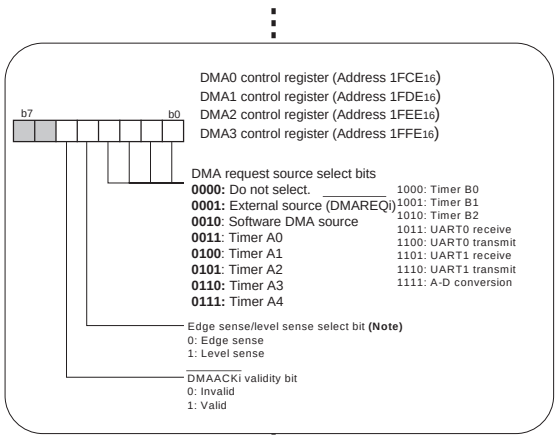
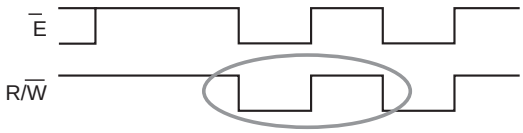
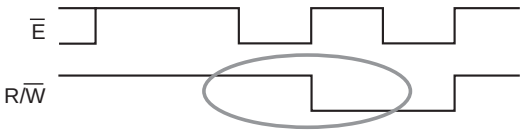
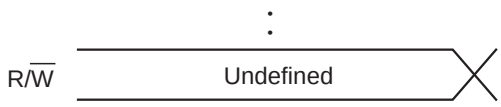
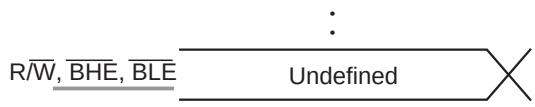
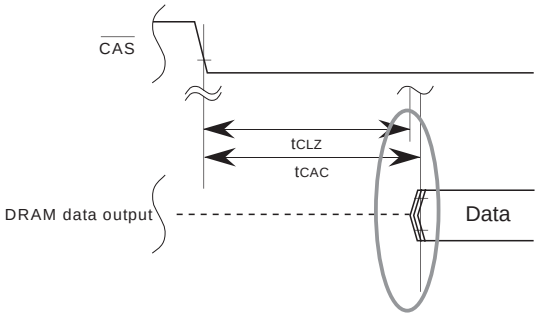
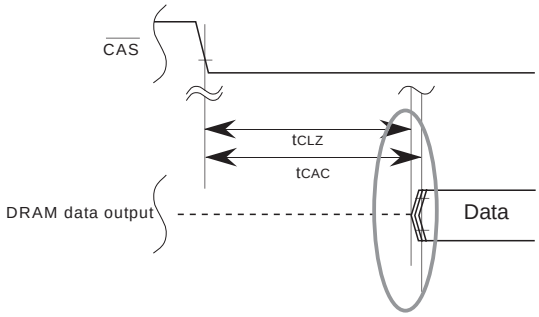
Supplement: Regardless of the DMAi enable bit’s contents, DMAi request bit is set to “1” when a DMA request is generated
</td></tr>
<tr><td>P13-27
Table 13.3.5</td><td>
<table>
<tr><td>DMAi request bit</td><td>0</td></tr>
</table>
</td><td>
<table>
<tr><td>DMAi request bit</td><td>When edge sense is selected in the burst transfer mode: o

When level sense is selected in the burst transfer mode: not changed

In the cycle-steal transfer mode: 0</td></tr>
</table>
</td></tr>
<tr><td>★ P13-28
13.3.6 (1)</td><td>(1) Restarting the same DMA ••• beginning
At normal and forced termination, the latches of SARi, DARi, and TCRi maintain their values written before the transfer start. (Refer to “Figure 13.3.4-a.”) ••• the following procedures:

● In single or repeat transfer mode
Set the DMAi enable bit to “1.” ••• (Refer to “Figure 13.3.4-b.”)
● In array chain ••• mode
① Re-set the values •••
② Set the DMAi •••</td><td>(1) Restarting the same DMA ••• beginning
● In single or repeat transfer mode
At normal and forced termination, the latches of SARi, DARi, and TCRi maintain their values written before the transfer start. (Refer to “Figure 13.3.4-a.”) ••• the following procedures:
Set the DMAi enable bit to “1.” ••• (Refer to “Figure 13.3.4-b.”)
● In array chain ••• mode
As values other than the initial values of SARi and TCRi have been set in their latches (refer to “Table 13.2.5”), it is necessary to re-set them.
① Re-set the values •••
② Set the DMAi •••</td></tr>
<tr><td>P13-48
Line 23</td><td>••• pin’s input level = “L,” the DMAi request bit is cleared to “0”; when this pin’s input level = “L,” the DMAi request bit is set to “1.”</td><td>••• pin’s input level = “L,” the DMAi request bit is set to “1”; when this pin’s input level = “H,” the DMAi request bit is cleared to “0.”</td></tr>
<tr><td>P13-51
Fig. 13.4.11</td><td> 
</td><td> 
</td></tr>
</table>

Corrections and Supplementary Explanation for “7721 Group User’s Manual” (REV. B) No. 3

Page	Error	Correction
P13-57 Fig. 13.5.3, P13-64 Fig. 13.6.3, P13-73 Fig. 13.7.4, P13-85 Fig. 13.8.4	 **Note**: When an external source (DMAREQi) is selected or when the cycle-steal transfer mode is selected, set this bit to “0” (Continue to the corresponding figure on the next page.)	 **Note**: When a source other than the external source (DMAREQi) is selected or when the cycle-steal transfer mode is selected, set this bit to “0” (Continue to the corresponding figure on the next page.)
P13-94 Fig.13.8.12, P13-95 Fig.13.8.13, P13-96 Fig.13.8.14		
★ P14-8 14.4.1 (3) Line 4	R/W is undefined.	R/W, BHE, and BLE are undefined.
★ P14-9 Fig. 14.4.1 (C) At refresh	(c) At refresh 	(c) At refresh 
P16-6 Fig.16.1.3		
★ P17-64 5. Setup for I/O ports	<Software protection> ● Read the data of ••• are equal. ● Since the output data may reverse because of noise, rewrite data ••• periodically. ● Rewrite data ••• periodically.	<Software protection> ● Read the data of ••• are equal. ● Since the output data may reverse because of noise, rewrite (**Note**) data ••• periodically. ● Rewrite (**Note**) data ••• periodically. **Note:** Be sure to use the **LDM** or **STA** instruction for the above rewriting.