GRADE A

MESC TECHNICAL NEWS

No. M7700-60-9912

Corrections and Supplementary Explanation for "7751 Series Software Manual" (REV.C)

This news includes a few corrections and supplementary explanation for "7751 Series Software Manual".

And also, this news includes the information previously announced by the MESC TECHNICAL NEWS (No. M7700-33-9803, Corrections and Supplementary Explanation for "7751 Series Software Manual" REV. B).

Notes 1: ★ represents the new information.

2: ☆ represents the information corrected only in the PDF version, not in the printed version (H-EF-436-A).

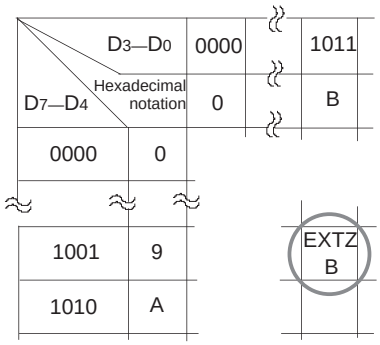
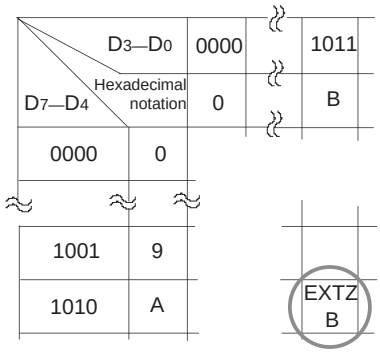
Please Visit Our Web Site.

- Mitsubishi MCU Technical Information (http://www.infomicom.mesc.co.jp/indexe.htm)
- Mitsubishi Microcomputer Development Support Tools (http://www.tool-spt.mesc.co.jp/index_e.htm)

Corrections and Supplementary Explanation for “7751 Series Software Manual” (REV.C) No.1

	Page	Error	Correction
	P2-8 (2) Bit 1: Zero flag	**Note:** This flag is invalid in the decimal mode addition (the **ADC** instruction).	**Note:** This flag is invalid in the decimal mode addition (the **ADC** instruction) and subtraction (the **SBC** instruction).
★	P4-24 **BRA** [Description]	••• The branch address is specified by a relative address.	••• The branch address is specified by a relative address. When using the **BRAL** (long relative) instruction, make sure that the low-order 16 bits of the branch address do not indicate address $FFFF_{16}$. If the low-order 16 bits of the branch address will indicate address $FFFF_{16}$, be sure to use the **JMPL** instruction.
☆	P4-35 **CPX**, P4-36 **CPY** **[Note]**	**Note:** The byte number increases by 1 when treating on 16-bit data in the condition of the data length flag = “0”.	**Note:** The byte number increases by 1 when treating a 16-bit data in the condition of the index register length flag = “0”.
☆	P4-44 **EOR** [Operation]	Acc ← Acc ∀ M When m = “0” Acc AccH M(n+1,n) □□ ← □□ ∀ □□	Acc ← Acc ∀ M When m = “0” Acc Acc M(n+1,n) □□ ← □□ ∀ □□
☆	P4-55 **LDX**, P4-56 **LDY** **[Note]**	**Note**: When treating a 16-bit data in the immediate addressing mode in the condition of the data length flag = “0”, the byte number increases by 1.	**Note**: When treating a 16-bit data in the immediate addressing mode in the condition of the index register length flag = “0”, the byte number increases by 1.
☆	P4-60 **MPYS** **[Status flags]**	C: Not affected.	C: Cleared to “0”.
★	P4-86 **PSH** [Operation]	M(S to S – i) ← A, B, X, Y, DPR, DT, PG, PS order to save ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ S ← S – i – 1	M(S to S –i + 1) ← A, B, X, Y, DPR, DT, PG, PS order to save ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ S ← S – i
	P4-100 **SBC**	Z: Set to “1“ when the operation result is “0”. Otherwise, cleared to “0”.	Z: Set to “1“ when the operation result is “0”. Otherwise, cleared to “0”. Meaningless for a decimal operation.
★	P4-133 (2)	(2) Do not set a value other than •••	(2) As for the products with the internal ROM area consisting of 60 Kbytes or less, do not set a value other than •••
	P4-133 (3)	(3) When performing a decimal operation, in the condition of the decimal mode flag = “1”: With **ADC** instruction Only the carry flag is valid. The zero, negative, and overflow flags are invalid. With **SBC** instruction Only the carry and zero flags are valid. The negative and overflow flags are invalid.	(3) When performing a decimal operation, in the condition of the decimal mode flag = “1”: With **ADC** and **SBC** instructions Only the carry flag is valid. The zero, negative, and overflow flags are invalid. (Delete)

Corrections and Supplementary Explanation for “7751 Series Software Manual” (REV.C) No.2

Page	Error	Correction
☆ P7-23		
P7-24