GRADE A

MESC TECHNICAL NEWS

No. M7700-56-9911

Corrections and Supplementary Explanation for "7902 Group User's Manual" (REV. A)

This news includes a few corrections and supplementary explanation for "7902 Group User's Manual" (PDF File, Rev.1.00).

The information about the product expansion, electrical characteristics, and develoment support tools will not be announced by the MESC TECHNICAL NEWS, even if the above information is updated.
So, for the product expansion, electrical characteristics, and development support tools, please refer to the latest version of the following documents in our web site:

- Product Expansion
  Mitsubishi Microcomputers General Catalog❋
- Electrical Characteristics
  Datasheets
- Development Support Tools
  Datasheets
  Microcomputers Development Support Tools Catalog❋
  Microcomputers Development Support Tools Accessory Guide

Please Visit Our Web Site.

- Mitsubishi MCU Technical Information (http://www.infomicom.mesc.co.jp/indexe.htm)
- Mitsubishi Microcompuet Development Support Tools
  (http://www.tool-spt.mesc.co.jp/index_e.htm)

❋ The printed version is also released.

Corrections and Supplementary Explanation for "7902 Group User's Manual" (REV.A) NO.1

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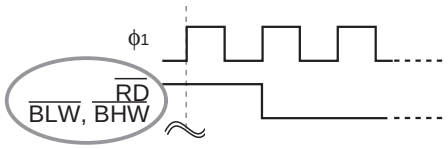
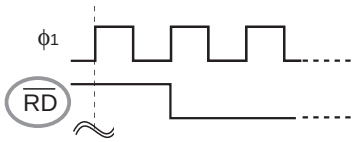
<table><tr><td>6</td><td>Recovery-cycle-insert number select bit (Note 6)</td><td></td></tr><tr><td>7</td><td>Internal ROM bus cycle select bit (Note 7)</td><td></td></tr></table></td></tr>
<tr><td></td><td>5: After reset, this bit can be set only once.
6: In the microprocessor mode, •••• reprogramming mode.”)</td><td>5: After reset, this bit can be set to “1” only once.
6: Make sure that a program to be used to change this bit's contents is allocated in the internal area.
7: In the microprocessor mode, •••• reprogramming mode.”)</td></tr>
<tr><td>P3-10
Last line</td><td>and bit 6 at addresses 8016, 8216, 8416, or 8616) must be set to “1.”</td><td>and bit 6 at address 8016, 8216, 8416, or 8616) must be set to “1.”
Make sure that a program to be used to change this bit's contents is allocated in the internal area.</td></tr>
<tr><td>P3-32
Figure 3.2.18</td><td>■ Burst ROM access
  </td><td>■ Burst ROM access
  </td></tr>
<tr><td>P5-6
First line</td><td>Figure 5.2.2 shows •••, and Figure 5.2.3 shows the procedure for setting or changing the PLL multiplication ratio.</td><td>Figure 5.2.2 shows •••, and Figure 5.2.3 shows the setting procedure for the clock control register when using the PLL frequency multiplier.</td></tr>
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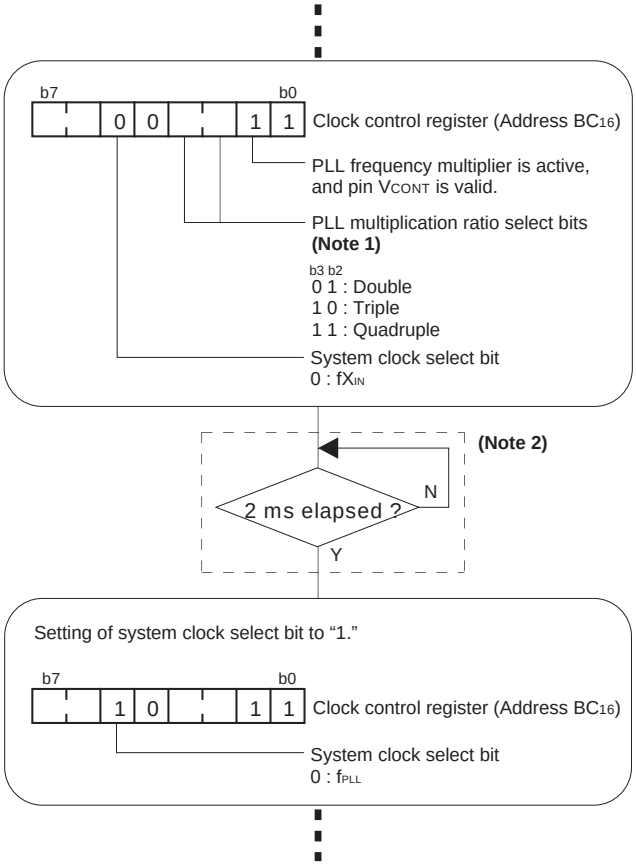
Figure 5.2.3</td><td>Fig. 5.2.3 Procedure for setting or changing PLL multiplication ratio</td><td>Fig. 5.2.3 Setting procedure for clock control register when using PLL frequency multiplier</td></tr>
</table>

Corrections and Supplementary Explanation for "7902 Group User's Manual" (REV.A) NO.2

Page: Correction

P5-8
Figure 5.2.3

(Revised figure)



Notes 1: After reset, these bits are allowed to be changed only once. If it is necessary to write a certain value to these bits, be sure to write the same value that has been written after the latest reset.
2: This decision is unnecessary if "double" is selected and the period of $\overline{\text{RESET}}$ = "L" is "the oscillation stabilizing time of an oscillator + 2 ms" or more.

Page	Error	Correction
P5-11 [Precautions for clock generating circuit] Last line	••• (bits 2, 3 at address BC16). (See Figure 5.2.3.)	••• (bits 2, 3 at address BC16). (See Figure 5.2.3.) After reset, the PLL multiplication ratio select bits are allowed to be changed only once. If it is necessary to write a certain value to these bits, be sure to write the same value that has been written after the latest reset.
P9-35 Figure 9.6.1, P21-20 (Addresses 5616 to 5A16)	Timer Ai mode register (i = 0 to 4) (Addresses 5616 to 5A16) 3, 4: Trigger select bits b4 b3 0 0 : 0 1 : } Writing "1" to one-shot start bit (•••) 1 0 : 1 1 :	Timer Ai mode register (i = 0 to 4) (Addresses 5616 to 5A16) 3, 4: Trigger select bits b4 b3 0 0 : 0 1 : } Writing "1" to count start bit (•••) 1 0 : 1 1 :
P12-6 Figure 12.2.3, P21-13 (Addresses 3416, 3C16)	**Notes 1:** Valid when the $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ enable bit (bit 4) is "0."	**Notes 1:** Valid when the $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ enable bit (bit 4) is "0" and $\overline{\text{CTS}}_i$/$\overline{\text{RTS}}_i$ separate select bit (bit 0 or 1 at address AC16) is "0."

Corrections and Supplementary Explanation for "7902 Group User's Manual" (REV.A) NO.3

P12-17 Figure 12.2.13, P21-42 (Address AC16)

Error

Serial I/O pin control register (Address AC_{16})

Bit	Bitname	Function
0	$\overline{CTS_0}/\overline{RTS_0}$ separate select bit	
1	$\overline{CTS_1}/\overline{RTS_1}$ separate select bit	
≈	≈	≈

Correction

Serial I/O pin control register (Address AC_{16})

Bit	Bitname	Function
0	$\overline{CTS_0}/\overline{RTS_0}$ separate select bit **(Note)**	
1	$\overline{CTS_1}/\overline{RTS_1}$ separate select bit **(Note)**	
≈	≈	≈

Note: Valid when the $\overline{CTS}/\overline{RTS}$ enable bit (bit 4 at addresses 34_{16} and $3C_{16}$) is "0."

P12-23 12.3.3 line 13, P12-28 12.3.5 line 12, P12-40 12.4.3 line 12, P12-47 12.4.5 line 6

Error

By connecting the $\overline{RTS}$ pin (receiver side) and $\overline{CTS}$ pin (transmitter side), •••

Correction

By connecting the $\overline{RTS_i}$ pin (receiver side) and $\overline{CTS_i}$ pin (transmitter side), •••

P14-3 Figure 14.2.2, P21-38 (Address 9616)

Error

D-A control register (Address 96_{16})

Bit	Bit name	Function
0	D-A_0 output enable bit	0 : Output is disabled. 1 : Output is enabled. **(Note)**
1	D-A_1 output enable bit	0 : Output is disabled. 1 : Output is enabled. **(Note)**
2	D-A_2 output enable bit	0 : Output is disabled. 1 : Output is enabled. **(Note)**
≈	≈	≈

Note: Pin DA_i is multiplexed ••••• (including programmable I/O port pin).

Correction

D-A control register (Address 96_{16})

Bit	Bit name	Function
0	D-A_0 output enable bit	0 : Output is disabled. 1 : Output is enabled. **(Notes 1, 2)**
1	D-A_1 output enable bit	0 : Output is disabled. 1 : Output is enabled. **(Notes 1, 2)**
2	D-A_2 output enable bit	0 : Output is disabled. 1 : Output is enabled. **(Notes 1, 2)**
≈	≈	≈

Notes 1: Pin DA_i is multiplexed ••••• (including programmable I/O port pin).

2: When not using the D-A converter, be sure to clear the contents of this bit to "0."

P14-3 Figure 14.2.3, P21-38 (Addresses 9816 to 9A16)

Error

D-A register i (i = 0 to 2) (Addresses 98_{16} to $9A_{16}$)

Bit	Function
7 to 0	Any value from 00_{16} through FF_{16} can be set, and this value is D-A converted and is output.

Correction

D-A register i (i = 0 to 2) (Addresses 98_{16} to $9A_{16}$)

Bit	Function
7 to 0	Any value from 00_{16} through FF_{16} can be set **(Note)**, and this value is D-A converted and is output.

Note: When not using the D-A converter, be sure to clear the contents of these bits to "00_{16}."

P14-7 [Precautions for D-A converter] Last line

Error

any other multiplexed input/output pin (including programmable I/O port pin).

Correction

any other multiplexed input/output pin (including programmable I/O port pin).

4. When not using the D-A converter, be sure to do as follows:
   - Clear the D-A_i (i = 0 to 2) output enable bit (bits 0 to 2 at address 96_{16}) to "0."
   - Clear the contents of the D-A register i (addresses 98_{16} to $9A_{16}$) to "00_{16}."

P16-2 Table 16.1.1

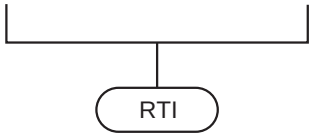
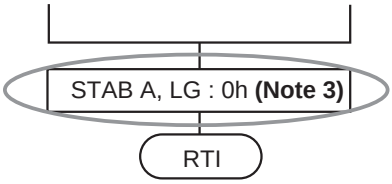
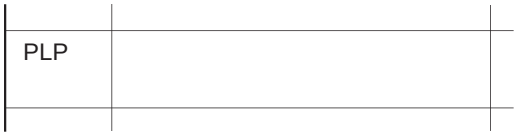
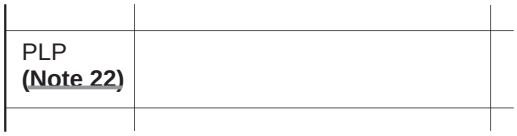
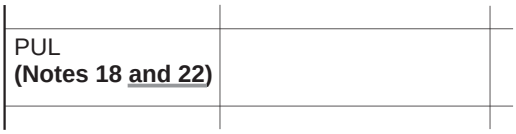
Error

Item	Stop mode
≈	≈
PLL frequency multiplier	Operates.
f_{CPU}, f_{BIU}	Inactive.

Correction

Item	Stop mode
≈	≈
PLL frequency multiplier	Stopped.
ϕ_{CPU}, ϕ_{BIU}	Inactive.

Corrections and Supplementary Explanation for “7902 Group User’s Manual” (REV.A) NO.4

Page	Error	Correction
P18-8 Figure 18.3.2, P18-9 Figure 18.3.3		 3. Make sure that this instruction is executed in the absolute long addressing mode. The above is just an example. In an actual programming, be sure to refer the format of the assembler description to be used.
P21-80 PLP		
P21-82 PUL		
P21-95 Last line	Note 21. Do not use the **SEP •••• SEI** instruction.)	Note 21. Do not use the **SEP •••• SEI** instruction.) Note 22. Be sure to keep flag I = “1” when executing the **PLP** or **PUL** instruction. Also, be sure to use the **SEI** instruction when setting flag I to “1.”